TEXAS INSTRUMENTS
TPS25830A-Q1, TPS25832A-Q1
ZHCSLL2 – MAY 2021

TPS2583xA-Q1 具有电缆补偿的 USB Type-C® 和 BC1.2 5V 3.5A 输出、36V 输入同步降压直流/直流稳压器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：–40°C 至 +125°C，T_A
  - HBM ESD 分类等级 H2
  - CDM ESD 分类等级 C5
- 同步降压直流/直流稳压器
  - 输入电压范围：4.5V 至 36V
  - 输出电流：3.5A
  - 5.1V 输出电压，精度为 ±1%
  - 电流模式控制
  - 频率可调节：300kHz 至 2.2MHz
  - 与外部时钟频率同步
  - 具有展频抖动功能的 FPWM
  - 内置补偿功能，便于使用
- 符合 USB-IF 标准
  - USB Type-C 1.3 版
    - CC 逻辑、V_{CONN} 拉电流和放电电流
    - USB 电缆极性保护 ($\overline{POL}$)
  - 符合 USB BC1.2 规范的 CDP/SDP 模式
  - 符合 MFI 过流限制
- 针对 USB 电源和通信进行了优化
  - 用户可编程的 USB 电流限制
  - 高达 1.5V 的电缆压降补偿
  - DP 和 DM 上的高带宽数据开关
  - 可用于进行 USB 固件更新的客户端模式
- 集成保护
  - V_{BUS} 对 V_{BAT} 短路保护
  - DP_IN、DM_IN、CCx 对 V_{BAT} 短路（仅 TPS25830A-Q1）
  - DP_IN、DM_IN、CCx 对 V_{BUS} 短路
  - 符合 IEC 61000-4-2 标准的 DP_IN、DM_IN 和 CCx
    - ±8kV 接触放电和 ±15kV 空气放电
- 故障标志报告
- 具有可湿性侧面的 32 引脚 QFN 封装

2 应用

- 汽车信息娱乐系统
- USB 媒体中心
- USB 充电器端口

3 说明

TPS2583xA-Q1 是一款包含一个同步直流/直流转换器的 USB Type-C 和 BC1.2 充电端口控制器。凭借电缆压降补偿，不管负载电流如何变化，V_{BUS} 电压都保持恒定，确保能以最佳电流和电压为连接的便携式设备充电。

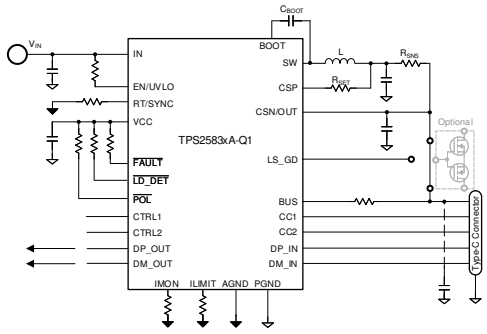
TPS2583xA-Q1 包含可实现 DP 和 DM 直通的高带宽模拟开关。

TPS25830A-Q1 还在 V_{BUS}、CC1、CC2、DM_IN 和 DP_IN 引脚上集成了对电池短路保护（支持高达 18V 的电压）。TPS25832A-Q1 不支持数据线（CC 和 Dx）对 VBAT 短路保护。

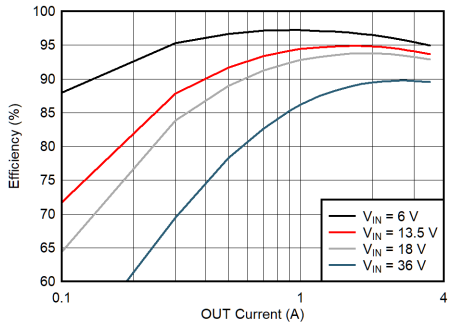
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS25830A-Q1	VQFN (32)	5.00mm × 5.00mm
TPS25832A-Q1	VQFN (32)	5.00mm × 5.00mm

(1) 如需了解所有可用选件的详细器件型号，请参阅数据表书末尾的可订购产品附录。



TPS2583xA-Q1 简化版原理图



降压效率与输出电流间的关系 (f_{sw} = 400kHz)

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

DATE	REVISION	NOTES
May 2021	*	Initial release.

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5 说明（续）

此同步降压稳压器具有电流模式控制并采用内部补偿，因此简化了设计。RT 引脚上有一个电阻器，可用于在 300kHz 和 2.2MHz 之间设置开关频率。在低于 400kHz 的频率下运行可实现更高的系统效率。在高于 2.1MHz 的频率下运行则可以避开 AM 无线电频带，并且能够使用较小的电感器。

TPS2583xA-Q1 集成了标准 USB Type-C 端口控制器功能，包括用于 3A 和 1.5A 电流广播的配置通道 (CC) 逻辑。电池充电（1.2 版）集成提供了利用 USB 数据线信号来确定 USB 端口拉电流能力的传统非 Type-C USB 设备所需的电气特性。

内含一个精密电流检测放大器，用于实现用户可编程电缆压降补偿和电流限制调整。电缆补偿可使降压稳压器输出电压随负载电流线性改变，以抵消由于汽车电缆布线中的导线电阻引起的压降，从而帮助便携式设备在重载下以最佳电流和电压充电。不管负载电流如何变化，在连接的便携式设备上测得的 V_{BUS} 电压都保持大致恒定，这使得便携式设备的电池充电器能够保持理想工作状态。

USB 规范要求 USB 充电端口满足电流限制，但也留下了合理的自由空间，允许系统设计人员基于系统要求选择过流保护级别。TPS2583xA-Q1 使用了一种新颖的双阈值电流限制电路，允许系统设计人员对降压稳压器的平均电流限制保护进行编程，或者在 CSN/OUT 和 BUS 引脚之间使用一个外部 NMOS 来对电流限制进行调整。由于实施了 NFET，TPS2583xA-Q1 降压稳压器可在 USB 端口上存在过流故障期间为其他负载提供 5V 输出。此外，TPS2583xA-Q1 使用的电流限制方法可以满足最新的 MFi 要求。

TPS2583xA-Q1 集成保护功能包括逐周期电流限制、断续短路保护、欠压锁定、V_{BUS} 过压和过流、CC 过压和过流、数据线 (D_x) 对 V_{BUS} 和 V_{BAT} 短路以及裸片过热保护。

TPS25830A-Q1 包括可实现 DP 和 DM 直通的高带宽模拟开关，支持数据线（Dx 和 CC）对 VBAT 短路保护。TPS25832A-Q1 不支持数据线（Dx 和 CC）对 VBAT 短路保护。

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6 Device Comparison Table

PART NUMBER	PACKAGE	MFI OC COMPLIANT	CLIENT MODE	DCP AUTO	DP/DM/CC SHORT TO BAT
TPS25830A-Q1	VQFN (32)	Yes	Yes	No	Yes
TPS25830-Q1	VQFN (32)	No	No	No	Yes
TPS25832A-Q1	VQFN (32)	Yes	Yes	No	No
TPS25832-Q1	VQFN(32)	No	No	No	No

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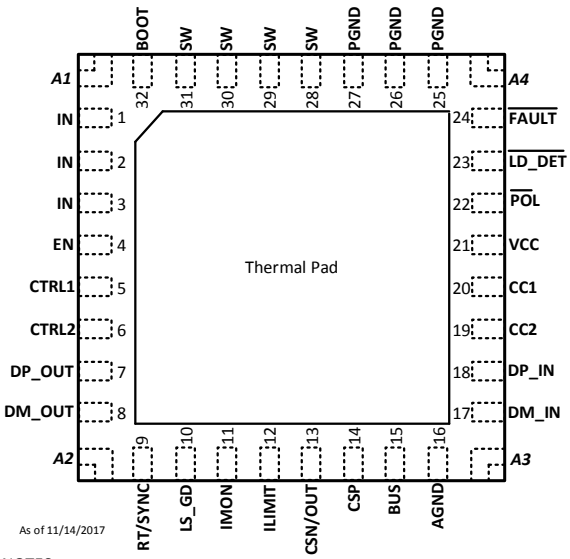
7 Pin Configuration and Functions



NOTES:
1) A1, A2, A3, and A4 are corner anchors for enhanced package stress performance.
2) A1, A2, A3, and A4 are electrically connected to the thermal pad.
3) A1, A2, A3, and A4 PCB lands should be electrically isolated or electrically connected to thermal pad and PGND.

图 7-1. TPS2583xA-Q1 RHB Package 32-Pin (VQFN) Top View

表 7-1. Pin Functions

PIN		TYPE (1)	I/O	DESCRIPTION
NAME	NO.			
AGND	16	G	–	Analog ground terminal. Ground reference for internal references and logic. All electrical parameters are measured with respect to this pin. Connect to system ground on PCB.
BOOT	32	P		Boot-strap capacitor connection for HS FET driver. Connect a high quality 100-nF capacitor from this pin to the SW pin.
BUS	15	A	I	VBUS discharge input. Connect to VBUS on USB Connector.
CC1	20	A	I/O	Analog input/output. Connect to Type-C CC1 pin.
CC2	19	A	I/O	Analog input/output. Connect to Type-C CC2 pin.
CSN/OUT	13	A	I	Negative input of current sense amplifier, also buck output for internal voltage regulation
CSP	14	A	I	Positive input of current sense amplifier.
CTRL1	5	A	I	Logic-level control inputs for device/system configuration (see Truth Table).
CTRL2	6	A	I	Logic-level control inputs for device/system configuration (see Truth Table).
DM_IN	17	A		DM data line. Connect to USB connector.
DM_OUT	8	A		DM data line. Connect to USB host controller.
DP_IN	18	A		DP data line. Connect to USB connector.
DP_OUT	7	A		DP data line. Connect to USB host controller.
EN/UVLO	4	A		Enable pin. Do not float. High = on, Low = off. Can be tied to VIN. Precision enable input allows adjustable UVLO by external resistor divider.
$\overline{\text{FAULT}}$	24	A	O	Active LOW open-drain output. Asserted during fault conditions (see 表 10-4).
ILIMIT	12	A		External resistor used to set the current-limit threshold (see 表 10-2).
IMON	11	A		External resistor used to set the max cable comp voltage at full load current.
IN	1, 2, 3	P	I	Input Supply to regulator. Connect a high-quality bypass capacitor(s) directly to this pin and PGND.

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表 7-1. Pin Functions (continued)

PIN		TYPE (1)	I/O	DESCRIPTION
NAME	NO.			
$\overline{\text{LD_DET}}$	23	A	O	Active LOW open-drain output. Asserted when a Type-C UFP is identified on the CC lines.
LS_GD	10	A		External NMOS gate driver.
PGND	25, 26, 27	G	–	Power ground terminal. Connect to system ground and AGND. Connect to bypass capacitor with short wide traces.
$\overline{\text{POL}}$	22	A	O	Active LOW open-drain output. Signals which Type-C CC pin is connected to the CC line. This gives cable orientation information needed to mux the super speed lines. Asserted when the CC2 pin is connected to the CC line in the cable.
RT/SYNC	9	A		Resistor Timing or External Clock input. An internal amplifier holds this terminal at a fixed voltage when using an external resistor to ground to set the switching frequency. If the terminal is pulled above the PLL upper threshold, a mode change occurs and the terminal becomes a synchronization input. The internal amplifier is disabled and the terminal is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the operating mode returns to resistor frequency programming.
SW	28, 29, 30, 31	P		Switching output of the regulator. Internally connected to source of the HS FET and drain of the LS FET. Connect to power inductor.
VCC	21	P		Output of internal bias supply. Used as supply to internal control circuits. Connect a high quality 2.2-µF capacitor from this pin to GND.

(1) A = Analog, P = Power, G = Ground.

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8 Specifications

8.1 Absolute Maximum Ratings

Voltages are with respect to GND (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
Input voltage	IN to PGND	–0.3	40	V
	OUT to PGND	–0.3	20	
	EN to AGND	–0.3	VIN + 0.3	
	CSP to AGND	–0.3	20	
	CSN to AGND	–0.3	20	
	BUS to AGND	–0.3	18	
	RT/SYNC to AGND	–0.3	6	
	CTRL1 or CTRL2 to AGND	–0.3	6	
	AGND to PGND	–0.3	0.3	
Output voltage	SW to PGND	–0.3	VIN + 0.3	V
	SW to PGND (less than 10 ns transients)	–3.5	40	
	BOOT to SW	–0.3	6	
	VCC to AGND	–0.3	6	
	LS_GD	–0.3	18	
Voltage range	**TPS25830A-Q1**: CC1 or CC2 to AGND	–0.3	18	V
	TPS25832A-Q1: CC1 or CC2 to AGND	–0.3	7	
	TPS25830A-Q1: DP_IN, DM_IN to AGND	–0.3	18	
	TPS25832A-Q1: DP_IN, DM_IN to AGND	–0.3	7	
	DP_OUT, DM_OUT to AGND	–0.3	6	
	$\overline{\text{FAULT}}$, $\overline{\text{POL}}$, $\overline{\text{LD_DET}}$ to AGND	–0.3	6	
	ILIMIT or IMON to AGND	–0.3	6	
Pin positive source current, I_{VCC}	VCC Source Current		5	mA
Pin positive source current, I_{SRC}	CC1, CC2		Internally Limited	A
Pin positive sink current, I_{SNK}	CC1, CC2 (while applying VCONN)		1	A
Pin positive sink current, I_{SNK}	$\overline{\text{FAULT}}$, $\overline{\text{POL}}$, $\overline{\text{LD_DET}}$		Internally Limited	A
I/O current	DP_IN to DP_OUT, or DM_IN to DM_OUT in SDP, CDP, or Client Mode	–100	100	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000(2)	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 8, 9, 17, 25 and 32)	±750(3)	
			Other pins	±750(3)	
		IEC 61000-4-2 contact discharge	DP_IN, DM_IN, CC1 and CC2 pins	±8000(4)	
		IEC 61000-4-2 air-gap discharge	DP_IN, DM_IN, CC1 and CC2 pins	±15000(4)	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) The passing level per AEC-Q100 Classification H2.
(3) The passing level per AEC-Q100 Classification C5.
(4) Surges per IEC61000-4-2, 1999 applied between DP_IN, DM_IN, CC1, CC2 and output ground of the TPS2583x-Q1 evaluation module. Addition 0.22u cap is needed on CCx pins.

8.3 Recommended Operating Conditions

Voltages are with respect to GND (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Input voltage	IN to PGND	4.5		36	V
		EN	0		VIN	
		VCC when driven from external regulator	0		5.5	
		DP_IN, DM_IN	0		3.6	
		DP_OUT, DM_OUT	0		3.6	
		CTRL1, CTRL2	0		VCC	
		RT/SYNC when driven by external clock	0		VCC	
V_{PU}	Pull up voltage	$\overline{FAULT}$, $\overline{LD_DET}$, $\overline{POL}$	0		VCC	
V_O	Output voltage	CSN/OUT	0		6.5	
I_O	Output current	Buck regulator output current	0		3.5	A
		DP_IN to DP_OUT or DM_IN to DM_OUT Continuous current in SDP, CDP or Client Mode	–30		30	mA
		DP_IN to DM_IN Continuous current in BC1.2 DCP Mode	–15		15	
I_{SRC}	Source current	CC1 or CC2 source current when supplying VCONN			250	
I_{SNK}	Sink current	$\overline{FAULT}$, $\overline{LD_DET}$, $\overline{POL}$			10	
I_I	Input current	Continuous current into the CSP pin			200	µA
R_{EXT}	External resistnace	R_{IMON}, R_{ILIMIT}	0		100	kΩ
T_J		Operating junction temperature	–40		125(1)	°C

(1) Operating at junction temperatures greater than 125°C is possible, however lifetime will be degraded.

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8.4 Thermal Information

THERMAL METRIC(1)		TPS2583xA-Q1 RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8.5 Electrical Characteristics

Limits apply over the junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400 kHz, C_{VCC} = 2.2 µF, R_{SNS} = 15 mΩ, R_{IMON} = 13 kΩ, R_{ILIMIT}= 13 kΩ, R_{SET}= 300 Ω unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (IN PIN)						
V_{IN}	Operating input voltage range		4.5		36	V
I_Q	Operating quiescent current (non switching)	$V_{EN/UVLO}$ = V_{IN}, CTRL1 = CTRL2 = V_{CC}, V_{CSN} = 8V, CC1 or CC2 = R_D, CC2 or CC1 = open		700	990	µA
I_{Q-SB}	Standby quiescent current	$V_{EN/UVLO}$ = V_{IN}, CTRL1 = CTRL2 = V_{CC}, CC1 and CC2 = open			290	µA
I_{SD}	Shutdown quiescent current; measured at IN pin.	EN= 0		10	16	µA
ENABLE and UVLO (EN/UVLO PIN)						
$V_{EN/UVLO_VCC_H}$	EN/UVLO input level required to turn on internal LDO	$V_{EN/UVLO}$ rising threshold			1.14	V
$V_{EN/UVLO_VCC_L}$	EN/UVLO input level required to turn off internal LDO	$V_{EN/UVLO}$ falling threshold	0.3			V
$V_{EN/UVLO_H}$	EN/UVLO input level required to turn on state machine	$V_{EN/UVLO}$ rising threshold	1.140	1.200	1.260	V
$V_{EN/UVLO_HYS}$	Hysteresis	$V_{EN/UVLO}$ falling threshold		90		mV
$I_{LKG_EN/UVLO}$	Enable input leakage current	$V_{EN/UVLO}$ = 3.3 V		0.5		uA
INTERNAL LDO						
V_{BOOT_UVLO}	Bootstrap voltage UVLO threshold			2.2		V
V_{CC}	Internal LDO output voltage appearing on VCC pin	6 V ≤ V_{IN} ≤ 36 V	4.75	5	5.25	V
$V_{CC_UVLO_R}$	Rising UVLO threshold		3.4	3.6	3.8	V
$V_{CC_UVLO_HYS}$	Hysteresis			600		mV
CURRENT LIMIT VOLTAGE (CSP - CSN/OUT PINS) TO ACTIVATE BUCK AVG CURRENT LIMITING						
(V_{CSP} – $V_{CSN/OUT}$)	Current limit voltage buck regulator control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 13 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 125°C	43.5	46	48.5	mV
(V_{CSP} – $V_{CSN/OUT}$)	Current limit voltage buck regulator control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 13 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 150°C	42.5	46	49.5	mV

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8.5 Electrical Characteristics (continued)

Limits apply over the junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400 kHz, C_{VCC} = 2.2 µF, R_{SNS} = 15 mΩ, R_{IMON} = 13 kΩ, R_{ILIMIT}= 13 kΩ, R_{SET}= 300 Ω unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
(V_{CSP} – $V_{CSN/OUT}$)	Current limit voltage buck regulator control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 26.1 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 125°C	20	22.5	25	mV
(V_{CSP} – $V_{CSN/OUT}$)	Current limit voltage buck regulator control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 26.1 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 150°C	19	22.5	26	mV
CURRENT LIMIT VOLTAGE (CSP - CSN/OUT PINS) TO ACTIVATE EXTERNAL NFET CURRENT LIMITING						
(V_{CSP} – $V_{CSN/OUT}$)	Current limit voltage NFET control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 6.8 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 125°C	41	44	47	mV
(V_{CSP} – $V_{CSN/OUT}$)	Current limit voltage NFET control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 6.8 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 150°C	39.5	44	48.5	mV
(V_{CSP} – $V_{CSN/OUT}$)	Current limit voltage NFET control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 13.7 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 125°C	19	22	25	mV
(V_{CSP} – $V_{CSN/OUT}$)	Current limit voltage NFET control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 13.7 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 150°C	18	22	26	mV
(V_{CSP} – $V_{CSN/OUT}$)	Secondary current limit voltage NFET control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 6.8 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 125°C	65.6	70.4	75.2	mV
(V_{CSP} – $V_{CSN/OUT}$)	Secondary current limit voltage NFET control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 6.8 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 150°C	63.2	70.4	77.6	mV
(V_{CSP} – $V_{CSN/OUT}$)	Secondary current limit voltage NFET control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 13.7 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 125°C	30.4	35.2	40	mV
(V_{CSP} – $V_{CSN/OUT}$)	Secondary current limit voltage NFET control loop	V_{CSN} = 5 V, R_{SET} = 300 Ω, R_{ILIMIT} = 13.7 kΩ, R_{IMON} = 13 kΩ, -40°C ≤ T_J ≤ 150°C	28.8	35.2	41.6	mV
CURRENT LIMIT - BUCK REGULATOR PEAK CURRENT LIMIT						
$I_{L-SC-HS}$	High-side current limit		6.2	7.1	8.0	A
$I_{L-SC-LS}$	Low-side current limit		4.6	5.4	6.2	A
$I_{L-NEG-LS}$	Low-side negative current limit		– 3.7	– 2.7	– 1.7	A
CABLE COMPENSATION VOLTAGE						
V_{IMON}	Cable compensation voltage	(V_{CSP} – V_{CSN}) = 46 mV, R_{SET} = 300 Ω, R_{ILIMIT} = 13 kΩ, R_{IMON} = 13 kΩ	0.935	1	1.065	V
V_{IMON}	Cable compensation voltage	(V_{CSP} – V_{CSN}) = 23 mV, R_{SET} = 300 Ω, R_{ILIMIT} = 13 kΩ, R_{IMON} = 13 kΩ	0.435	0.5	0.565	V
V_{IMON}	Cable compensation voltage (internal clamp)	(V_{CSP} – V_{CSN}) = 46 mV, R_{SET} = 300 Ω, R_{ILIMIT} = 13 kΩ, R_{IMON} = open		1.8		V
BUCK OUTPUT VOLTAGE (CSN/OUT PIN)						
$V_{CSN/OUT}$	Output voltage	CC1 or CC2 pulldown resistance = R_d, R_{IMON} = 0 Ω, R_{ILIMIT} = 0 Ω, – 40°C ≤ T_J ≤ 125°C	5.05	5.10	5.15	V
$V_{CSN/OUT}$	Output voltage accuracy	CC1 or CC2 pulldown resistance = R_d, R_{IMON} = 0 Ω, R_{ILIMIT} = 0 Ω	– 1		1	%

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8.5 Electrical Characteristics (continued)

Limits apply over the junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400 kHz, C_{VCC} = 2.2 µF, R_{SNS} = 15 mΩ, R_{IMON} = 13 kΩ, R_{ILIMIT}= 13 kΩ, R_{SET}= 300 Ω unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CSN/OUT_OV}	Overvoltage level on CSN/OUT pin which buck regulator stops switching	$V_{CSN/OUT}$ rising	7.1	7.5	7.9	V
V_{CSN/OUT_OV_HYS}	Hysteresis			500		mV
V_{HC}	CSN / OUT pin voltage required to trigger short circuit hiccup mode			2		V
V_{DROP}	Dropout voltage (V_{IN}-V_{OUT})	V_{IN} = V_{OUT} + V_{DROP}, V_{OUT} = 5.1V, I_{OUT} = 3A		150		mV
BUCK REGULATOR INTERNAL RESISTANCE						
$R_{DS-ON-HS}$	High-side MOSFET ON-resistance	Load = 3 A, T_J = 25°C		40	45	mΩ
$R_{DS-ON-HS}$	High-side MOSFET ON-resistance	Load = 3 A, -40°C ≤ T_J ≤ 125°C		40	68	mΩ
$R_{DS-ON-HS}$	High-side MOSFET ON-resistance	Load = 3 A, -40°C ≤ T_J ≤ 150°C		40	75	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET ON-resistance	Load = 3 A, T_J = 25C		35	41	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET ON-resistance	Load = 3 A, -40°C ≤ T_J ≤ 125°C		35	60	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET ON-resistance	Load = 3 A, -40°C ≤ T_J ≤ 150°C		35	68	mΩ
NFET GATE DRIVE (LS_GD PIN)						
V_{LS_GD}	NFET gate drive output voltage	$V_{CSN/OUT}$ = 5.1 V, C_G = 1000 pF	9.5	11	12.5	V
$I_{LS_DR_SRC}$	NFET gate drive output source current	$V_{CSN/OUT}$ = 5.1 V, C_G = 1000 pF	2	3	4	µA
$I_{LS_DR_SNK}$	NFET gate drive output sink current	$V_{CSN/OUT}$ = 5.1 V, C_G = 1000 pF	20	35	50	µA
$V_{LS_GD_UVLO_R}$	$V_{CSN/OUT}$ rising threshold for LS_GD operation	$V_{CSN/OUT}$ rising	2.85	3	3.18	V
$V_{LS_GD_UVLO_HYS}$	Hysteresis			80		mV
BUS DISCHARGE (BUS PIN)						
R_{BUS_DCHG}	BUS discharge resistance	V_{BUS} = 4 V	250	320	550	Ω
$V_{BUS_NO_DCHG}$	Falling threshold for VBUS not discharged				0.8	V
$R_{BUS_DCHG_BLEED}$	BUS bleed resistance	V_{BUS} = 4 V, No sink termination on CC lines, Time > $t_{W_BUS_DCHG}$	100	130	200	kΩ
V_{BUS_OV}	Rising threshold for BUS pin overvoltage protection	V_{BUS} rising	6.6	7	7.3	V
$V_{BUS_OV_HYS}$	Hysteresis			180		mV
$R_{BUS_DCHG_18V}$	Discharge resistance for BUS	V_{BUS} = 18V, measure leakage current		29		kΩ
$R_{BUS_DCHG_8V}$	Discharge resistance for BUS	V_{BUS} = 8V, measure leakage current		35		kΩ
CC1 AND CC2 - VCONN POWER SWITCH (CC1 AND CC2 PINS)						
R_{DS-ON}	On-state resistance	I_{CCn} = 250 mA, T_J = 25°C		500	540	mΩ
R_{DS-ON}	On-state resistance	I_{CCn} = 250 mA, –40°C ≤ T_J ≤ 125°C		500	830	mΩ
R_{DS-ON}	On-state resistance	I_{CCn} = 250 mA, –40°C ≤ T_J ≤ 150°C,		500	920	mΩ
I_{OS_CCn}	VCONN short circuit current limit	Short circuit current limit	350	430	550	mA
R_{VCONN_DCHG}	Discharge resistance	CC pin that was providing V_{CONN} before detach: V_{CCX} = 4V	650	850	1100	Ω
V_{TH}	Falling threshold for discharged	CC pin that was providing V_{CONN} before detach	570	600	630	mV
V_{TH}	Discharged threshold hysteresis			100		mV
V_{CCx_OV}	Rising threshold for CCn pin overvoltage protection	CC pin voltage V_{CCn} rising	5.8	6.1	6.4	V

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8.5 Electrical Characteristics (continued)

Limits apply over the junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400 kHz, C_{VCC} = 2.2 µF, R_{SNS} = 15 mΩ, R_{IMON} = 13 kΩ, R_{ILIMIT}= 13 kΩ, R_{SET}= 300 Ω unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CCx_OV_HYS}$	Hysteresis			150		mV
$R_{CCn_DCHG_18V}$	Discharge resistance for CCn	CC pin voltage V_{CCn} = 18V, measure leakage current		40		kΩ
$R_{CCn_DCHG_8V}$	Discharge resistance for CCn	CC pin voltage V_{CCn} = 8V, measure leakage current		86		kΩ
CC1/CC2 CONNECT MANAGEMENT: DANGLING ELECTRONICALLY MARKED CABLE MODE						
I_{SRC_CCn}	Sourcing current on the passthrough CC line	CC pin voltage 0 V ≤ V_{CCn} ≤ 1.5 V	64	80	96	µA
I_{SRC_CCn}	Sourcing current on the Ra CC line	CC pin voltage 0 V ≤ V_{CCn} ≤ 1.5 V	64	80	96	µA
CC1/CC2 CONNECT MANAGEMENT: UFP MODE						
I_{SRC_CCn}	Sourcing current	V_{CTRL1} = V_{CC} and V_{CTRL2} = V_{CC}, CC pin voltage: 0 V ≤ V_{CCn} ≤ 1.5 V (with CDP mode)	308	330	354	µA
I_{SRC_CCn}	Sourcing current	V_{CTRL1} = V_{CC} and V_{CTRL2} = GND, CC pin voltage: 0 V ≤ V_{CCn} ≤ 1.5 V (with SDP mode)	168	180	192	µA
I_{SRC_CCn}	Sourcing current	V_{CTRL1} = GND and V_{CTRL2} = V_{CC}, CC pin voltage: 0 V ≤ V_{CCn} ≤ 1.5 V (client mode)	168	180	192	µA
I_{SRC_CCn}	Sourcing current	V_{CTRL1} = GND and V_{CTRL2} = GND, CC pin voltage: 0 V ≤ V_{CCn} ≤ 1.5 V (client mode)	168	180	192	µA
I_{REV}	Reverse leakage current	CCx is the CC pin under test, CCy is the other CC pin. CC pin voltage VCCx = 5.5 V, CCy = 0V or floating, V_{EN} = 0 V, I_{REV} is current into CCx pin		0	5	µA
I_{REV}	Reverse leakage current	CCx is the CC pin under test, CCy is the other CC pin. CC pin voltage VCCx = 5.5 V, CCy = 0, V_{EN} = V_{IN}, I_{REV} is current into CCx pin under test		9	12	µA
$\overline{\text{FAULT}}$, LD_DET, POL						
V_{OL}	FAULT Output low voltage	I_{SNK_PIN} = 0.5 mA			250	mV
I_{OFF}	FAULT Off-state leakage	V_{PIN} = 5.5 V			1	µA
V_{OL}	LD_DET, POL Output low voltage	I_{SNK_PIN} = 0.5 mA			250	mV
I_{OFF}	LD_DET, POL Off-state leakage	V_{PIN} = 5.5 V			1	µA
CTRL1, CTRL2 - LOGIC INPUTS						
V_{IH}	Rising threshold voltage			1.48	2	V
V_{IL}	Falling threshold voltage		0.85	1.30		V
V_{HYS}	Hysteresis			180		mV
I_{IN}	Input current		–1		1	µA
DP_IN AND DM_IN OVERVOLTAGE PROTECTION						
$V_{Dx_IN_OV}$	Rising threshold for Dx_IN overvoltage protection	DP_IN or DM_IN rising	3.7	3.9	4.15	V
	Hysteresis			100		mV
$R_{Dx_IN_DCHG_18V}$	Discharge resistance for Dx_IN	VDx_IN = 18V, measure leakage current		94		kΩ
$R_{Dx_IN_DCHG_5V}$	Discharge resistance for Dx_IN	VDx_IN = 5V, measure leakage current		416		kΩ

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8.5 Electrical Characteristics (continued)

Limits apply over the junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400 kHz, C_{VCC} = 2.2 µF, R_{SNS} = 15 mΩ, R_{IMON} = 13 kΩ, R_{ILIMIT}= 13 kΩ, R_{SET}= 300 Ω unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-BANDWIDTH ANALOG SWITCH						
R_{DS_ON}	DP and DM switch on-resistance	V_{DP_OUT} = V_{DM_OUT} = 0 V, I_{DP_IN} = I_{DM_IN} = 30 mA		3.4	6.3	Ω
R_{DS_ON}	DP and DM switch on-resistance	V_{DP_OUT} = V_{DM_OUT} = 2.4 V, I_{DP_IN} = I_{DM_IN} = – 15 mA		4.3	7.7	Ω
$\lvert \Delta R_{DS_ON} \rvert$	Switch resistance mismatch between DP and DM channels	V_{DP_OUT} = V_{DM_OUT} = 0 V, I_{DP_IN} = I_{DM_IN} = 30 mA		0.05	0.15	Ω
$\lvert \Delta R_{DS_ON} \rvert$	Switch resistance mismatch between DP and DM channels	V_{DP_OUT} = V_{DM_OUT} = 2.4 V, I_{DP_IN} = I_{DM_IN} = – 15 mA		0.05	0.15	Ω
C_{IO_OFF}	DP/DM switch off-state capacitance	V_{EN} = 0 V, V_{DP_IN} = V_{DM_IN} = 0.3 V, Vac = 0.03 V_{PP}, f = 1 MHz		6.7		pF
C_{IO_ON}	DP/DM switch on-state capacitance	V_{DP_IN} = V_{DM_IN} = 0.3 V, Vac = 0.03 V_{PP}, f = 1 MHz		10		pF
O_{IRR}	Off-state isolation	V_{EN} = 0 V, f = 250 MHz		9		dB
X_{TALK}	On-state cross-channel isolation	f = 250 MHz		29		dB
$I_{lkg(OFF)}$	Off-state leakage current, DP_OUT and DM_OUT	V_{EN} = 0 V, V_{DP_IN} = V_{DM_IN} = 3.6 V, V_{DP_OUT} = V_{DM_OUT} = 0 V, measure I_{DP_OUT} and I_{DM_OUT}		0.1	1.5	µA
BW	Bandwidth (– 3 dB)	R_L = 50 Ω		800		MHz
CHARGING DOWNSTREAM PORT (CDP) DETECT						
V_{DM_SRC}	DM_IN CDP output voltage	V_{DP_IN} = 0.6 V, – 250 µA < I_{DM_IN} < 0 µA	0.5	0.6	0.7	V
V_{DAT_REF}	DP_IN rising lower window threshold for V_{DM_SRC} activation		0.36	0.38	0.4	V
V_{DAT_REF}	Hysteresis			50		mV
V_{LGC_SRC}	DP_IN rising upper window threshold for VDM_SRC deactivation		0.91	0.95	0.99	V
$V_{LGC_SRC_HYS}$	Hysteresis			100		mV
I_{DP_SINK}	DP_IN sink current	V_{DP_IN} = 0.6 V	40	70	100	µA
RT/SYNC THRESHOLD (RT/SYNC PIN)						
$V_{IH_RT/SYNC}$	RT/SYNC high threshold for external clock synchronization	Amplitude of SYNC clock AC signal (measured at SYNC pin)	2			V
$V_{IL_RT/SYNC}$	RT/SYNC low threshold for external clock synchronization	Amplitude of SYNC clock AC signal (measured at SYNC pin)			0.8	V
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown	Shutdown threshold		160		°C
		Recovery threshold		140		°C

8.6 Timing Requirements

Limits apply over the junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400 kHz, C_{VCC} = 2.2 µF, R_{SNS} = 15 mΩ, R_{IMON} = 13 kΩ, R_{ILIMIT}= 13 kΩ, R_{SET}= 300 Ω unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

		MIN	NOM	MAX	UNIT
SYNC (RT/SYNC PIN) WITH EXTERNAL CLOCK					

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8.6 Timing Requirements (continued)

Limits apply over the junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400 kHz, C_{VCC} = 2.2 µF, R_{SNS} = 15 mΩ, R_{IMON} = 13 kΩ, R_{ILIMIT}= 13 kΩ, R_{SET}= 300 Ω unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

			MIN	NOM	MAX	UNIT
f_{SYNC}	Switching frequency using external clock on RT/SYNC pin		300		2300	kHz
T_{SYNC_MIN}	Minimum SYNC input pulse width	f_{SYNC} = 400 kHz, $V_{RT/SYNC}$ > $V_{IH_RT/SYNC}$, $V_{RT/SYNC}$ < $V_{IL_RT/SYNC}$		100		ns
T_{LOCK_IN}	PLL lock time			100		µs

8.7 Switching Characteristics

Limits apply over the junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400 kHz, C_{VCC} = 2.2 µF, R_{SNS} = 15 mΩ, R_{IMON} = 13 kΩ, R_{ILIMIT}= 13 kΩ, R_{SET}= 300 Ω unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START						
T_{SS}	Internal soft-start time	The time of internal reference to increase from 0 V to 1.0 V	3	5	7	ms
HICCUP MODE						
N_{OC}	Number of cycles that LS current limit is tripped to enter Hiccup mode			128		Cycles
T_{OC}	Hiccup retry delay time			118		ms
SW (SW PIN)						
T_{ON_MIN}	Minimum turnon-time			105		ns
T_{ON_MAX}	Maximum turnon-time, HS timeout in dropout			7.5		µs
T_{OFF_MIN}	Minimum turnoff time			80		ns
D_{max}	Maximum switch duty cycle			98		%
TIMING RESISTOR AND INTERNAL CLOCK						
f_{SW_RANGE}	Switching frequency range using RT mode		300		2300	kHz
f_{SW}	Switching frequency	R_T = 49.9 kΩ	360	400	440	kHz
	Switching frequency	R_T = 8.66 kΩ	1953	2100	2247	kHz
FS_{SS}	Frequency span of spread spectrum operation			±6		%
BUS DISCHARGE						
$t_{DEGA_OUT_DCHG}$	Discharge asserting deglitch		5.0	12.5	23.4	ms
$t_{W_BUS_DCHG}$	V_{BUS} discharge time after sink termination removed from CC lines	V_{BUS} = 1 V, time I_{SNK_OUT} > 1 mA after sink termination removed from CC lines	150	266	400	ms
CC1/CC2 - VCONN POWER SWITCH 5.1 kΩ ON ONE CC PIN AND 1 kΩ ON THE OTHER						
t_r	Output voltage rise time	C_L = 1 µF, R_L = 100 Ω (measured from 10% to 90% of final value)	0.78	1.1	1.95	ms
t_f	Output voltage fall time		0.18	0.32	0.38	
t_{on}	Output voltage turnon-time	C_L = 1 µF, R_L = 100 Ω	4.1	6.2	8.5	ms
t_{off}	Output voltage turnoff time		0.5	1	1.6	
CC1/CC2 VCONN POWER SWITCH: CURRENT LIMIT						
t_{IOS}	Short circuit response time			15		µs
CC1/CC2 - CONNECT MANAGEMENT - ATTACH AND DETACH DEGLITCH						

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8.7 Switching Characteristics (continued)

Limits apply over the junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400 kHz, C_{VCC} = 2.2 µF, R_{SNS} = 15 mΩ, R_{IMON} = 13 kΩ, R_{ILIMIT}= 13 kΩ, R_{SET}= 300 Ω unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DEGA_CC_ATT}$	Attach asserting deglitch		1.1	2.08	3.29	ms
$t_{DEGD_CC_DET}$	Detach asserting deglitch for exiting UFP state		6.98	12.7	19.4	ms
CC1/CC2 - CONNECT MANAGEMENT - ATTACHED MODE 5.1-kΩ OR 1-kΩ TERMINATION ON AT LEAST ONE CC PIN						
$t_{DEGA_CC_SHORT}$	Detach, Rd and Ra asserting deglitch		78	195	366	µs
$t_{DEGA_CC_LONG}$	Long deglitch		87	150	217	ms
CC1/CC2 - CONNECT MANAGEMENT - VCONN DISCHARGED MODE						
$t_{W_CC_DCHG}$	Discharge wait time		37	66	99	ms
NFET DRIVER						
t_r	V_{LS_DR} rise time	VOUT = 5.1V, NFET = CSD87502Q2, time from LS_GD 10% to 90%		1000		µs
t_f	V_{LS_DR} fall time	VOUT = 5.1 V, NFET = CSD87502Q2, time from LS_GD time 90% to 10%		100		µs
CURRENT LIMIT - EXTERNAL NFET CONNECTED BETWEEN CSN/OUT AND BUS, LS_GD CONNECTED TO FET GATE						
$t_{OC_HIC_DEG}$	Deglitch time before hiccup mode			2		ms
$t_{OC_HIC_RST}$	Reset time for exiting hiccup mode			16		ms
$t_{OC_HIC_ON}$	ON-time during hiccup mode			2		ms
$t_{OC_HIC_OFF}$	OFF-time during hiccup mode			263		ms
$\overline{\text{FAULT}}$ DUE TO VBUS OC, VBUS OV, DP OV, DM OV, CC OV, CC OC						
t_{DEGLA}	Asserting deglitch time		5.5	8.2	11.5	ms
t_{DEGLD}	De-asserting deglitch time		5.5	8.2	11.5	ms
$\overline{\text{LD_DET}}$, $\overline{\text{POL}}$						
t_{DEGLA}	Asserting deglitch time		88	150	220	ms
t_{DEGLD}	De-asserting deglitch time		7.0	12.7	19.4	ms
HIGH-BANDWIDTH ANALOG SWITCH						
t_{pd}	Analog switch propagation delay			0.14		ns
t_{SK}	Analog switch skew between opposite transitions of the same port (t_{PHL} – t_{PLH})			0.02		ns
t_{OV_Dn}	DP_IN and DM_IN overvoltage protection response time			2		µs

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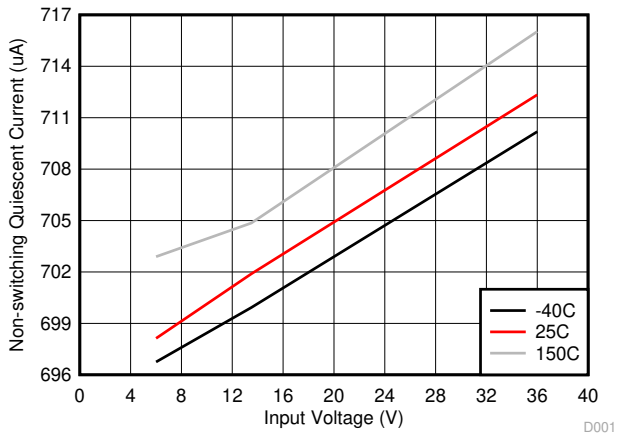
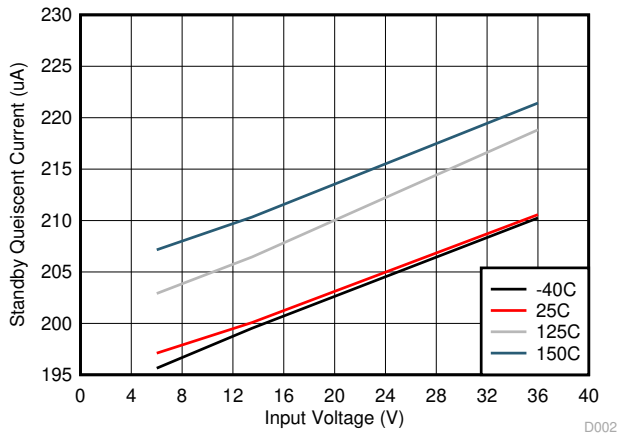
8.8 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 8.2 µH, C_{OUT_CSP} = 66 µF, C_{OUT_CSN} = 0.1 µF, C_{BUS} = 1 µF, T_A = 25 °C.



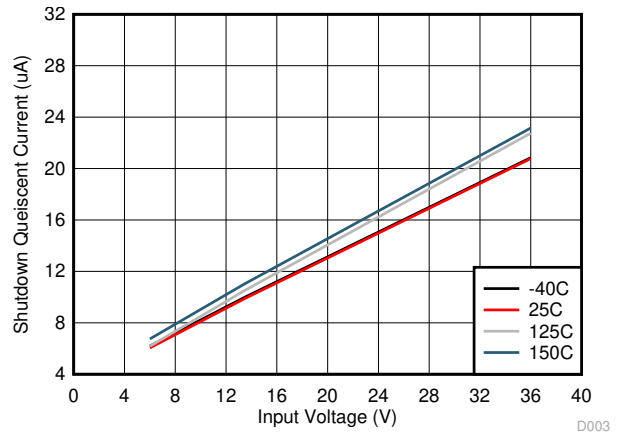
V_{CSN} = 8 V CC1= R_d

图 8-1. Non-Switching Quiescent Current



CC1 = OPEN CC2 = OPEN

图 8-2. Standby Quiescent Current



EN = 0 V

图 8-3. Shutdown Quiescent Current

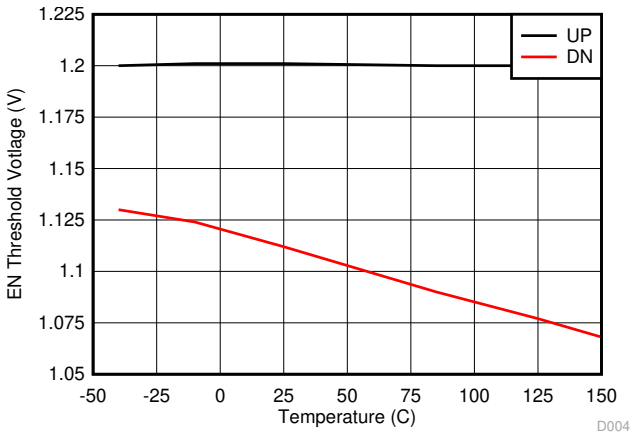


图 8-4. Precision Enable Threshold

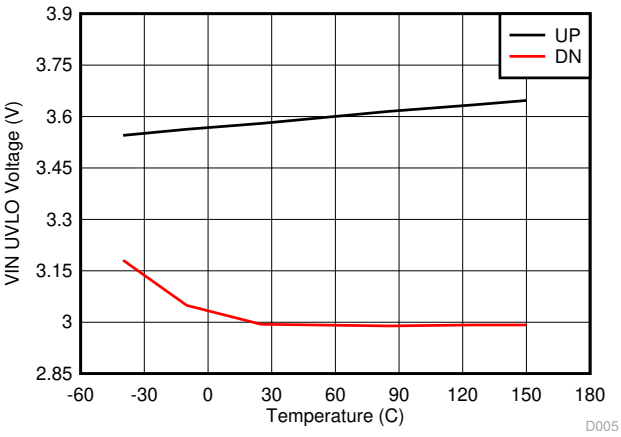


图 8-5. VIN UVLO Threshold

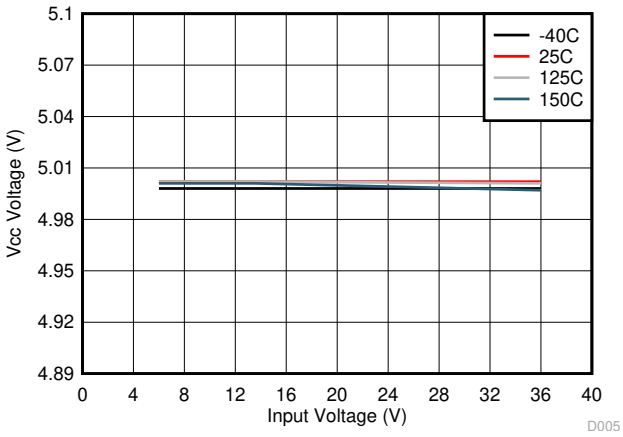


图 8-6. VCC vs Input Voltage

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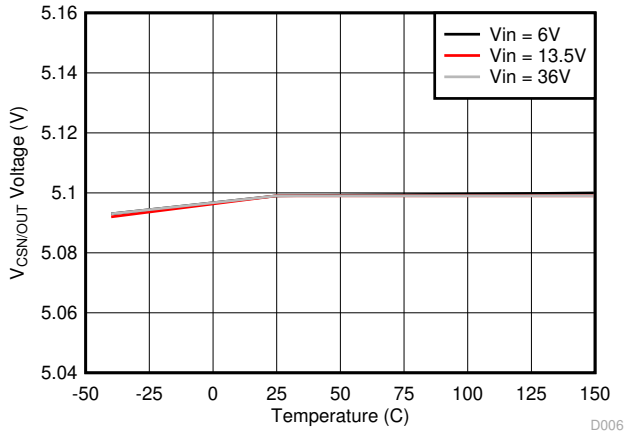
8.8 Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 8.2 µH, C_{OUT_CSP} = 66 µF, C_{OUT_CSN} = 0.1 µF, C_{BUS} = 1 µF, T_A = 25 °C.



R_{IMON} = 0 Ω

图 8-7. $V_{CSN/OUT}$ Voltage vs Junction Temperature

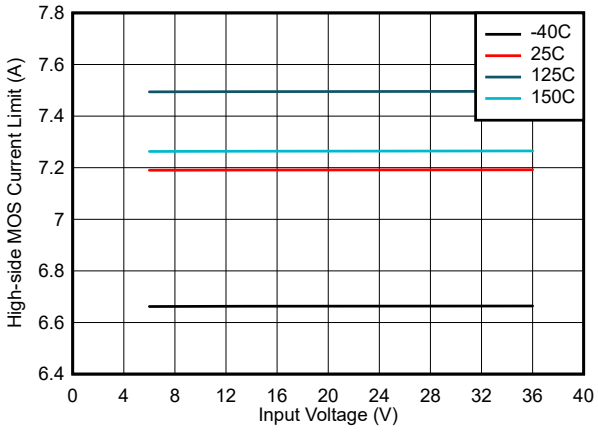


图 8-8. High-Side Current Limit vs Input Voltage

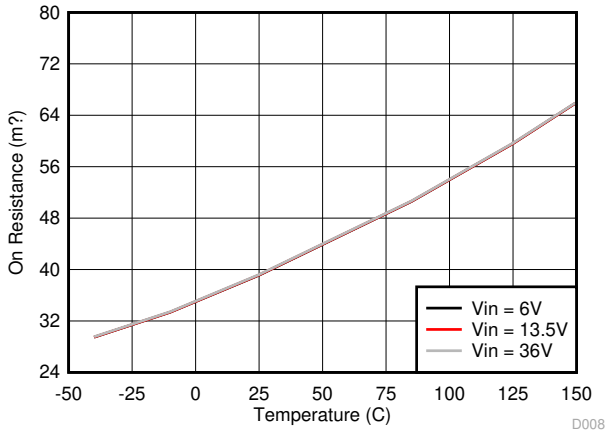


图 8-9. High-Side MOSFET on Resistance vs Junction Temperature

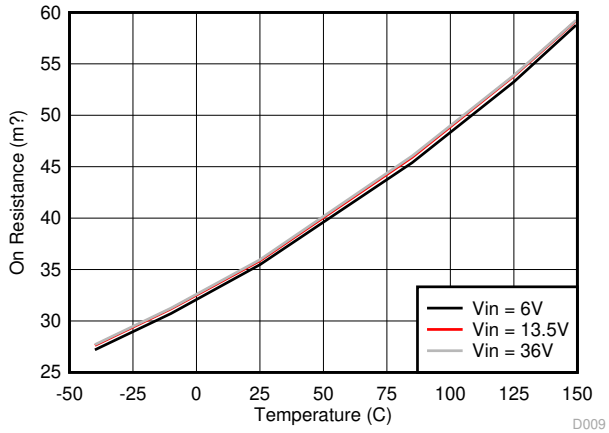
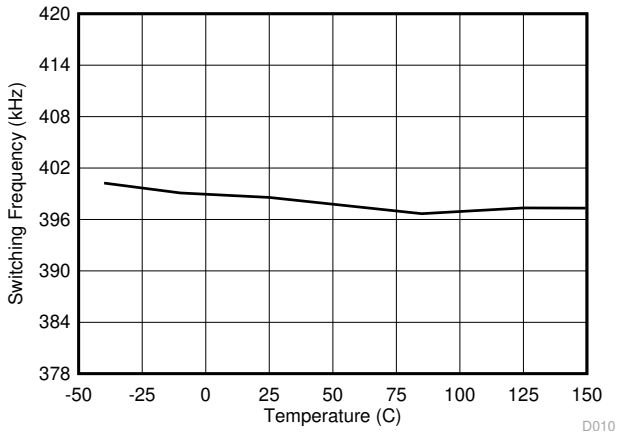
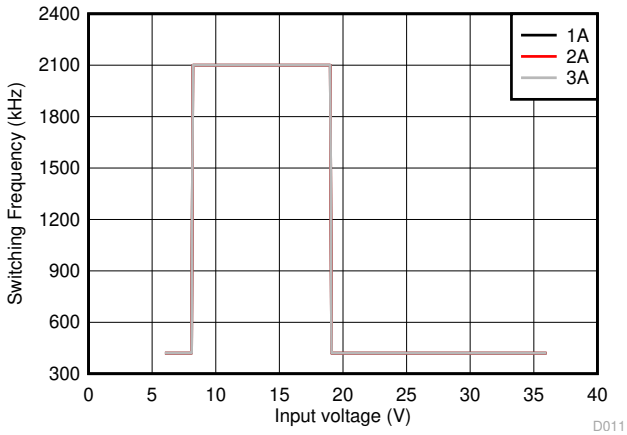


图 8-10. Low-Side MOSFET on Resistance vs Junction Temperature



R_T = 49.9 kΩ

图 8-11. Switching Frequency vs Junction Temperature



R_T = 8.66 kΩ

图 8-12. Switching Frequency vs VIN Voltage

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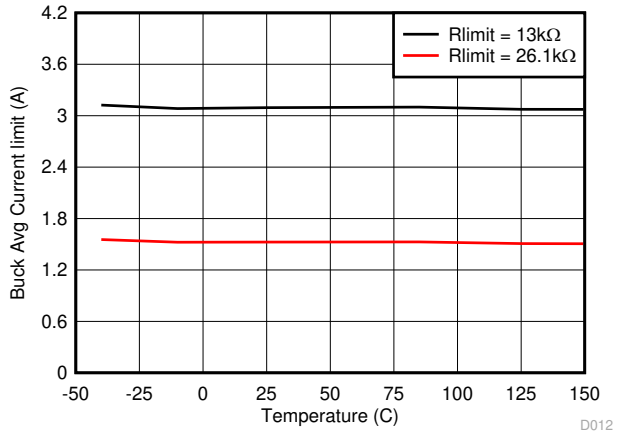
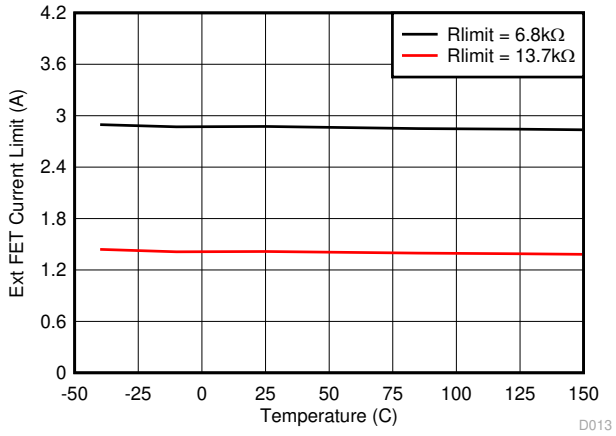
8.8 Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 8.2 µH, C_{OUT_CSP} = 66 µF, C_{OUT_CSN} = 0.1 µF, C_{BUS} = 1 µF, T_A = 25 °C.



R_{SNS} = 15 mΩ R_{SET} = 300 Ω

图 8-13. Buck Average Current Limit vs Junction Temperature



R_{SNS} = 15 mΩ R_{SET} = 300 Ω

图 8-14. External FET Current Limit vs Junction Temperature

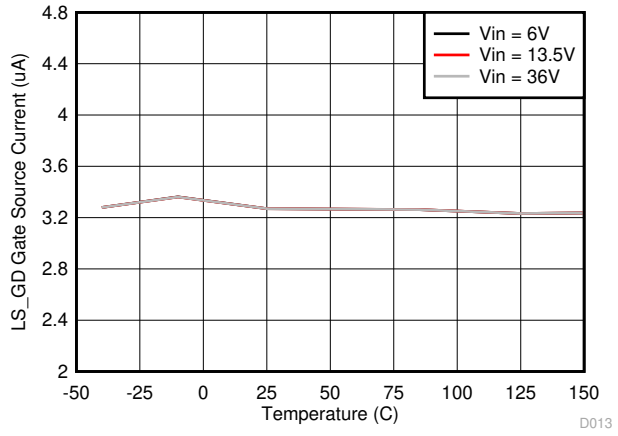
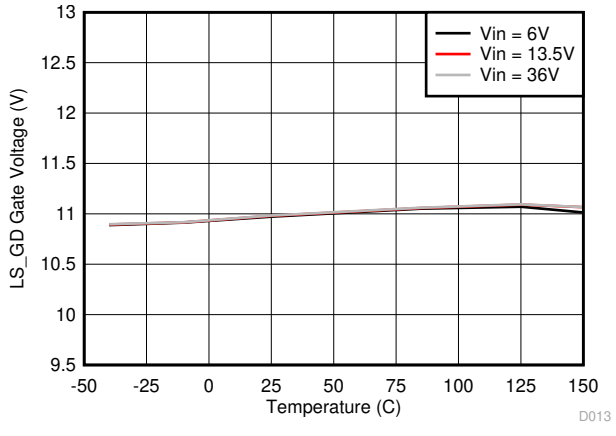
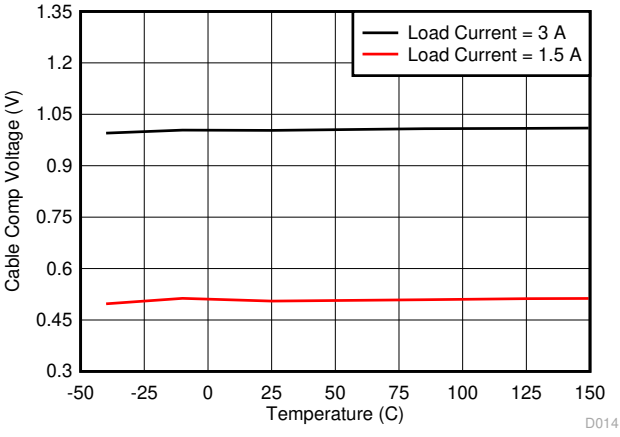


图 8-15. LS_GD Gate Source Current vs Junction Temperature



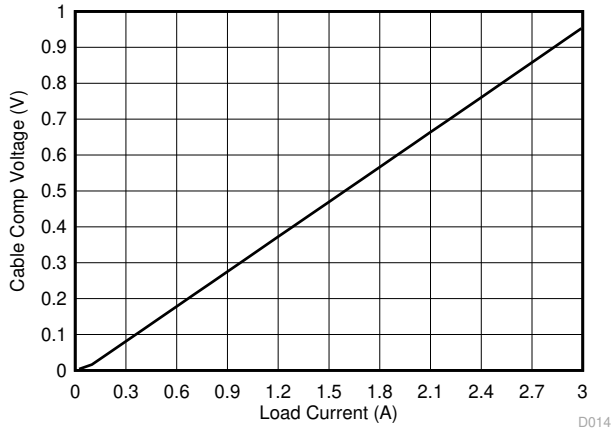
$V_{CSN/OUT}$ = 5.1 V R_{IMON} = 0 kΩ

图 8-16. LS_GD Gate Voltage vs Junction Temperature



R_{SNS} = 15 mΩ R_{SET} = 300 Ω R_{IMON} = 13 kΩ

图 8-17. Cable Compensation Voltage vs Junction Temperature



R_{SNS} = 15 mΩ R_{SET} = 300 Ω R_{IMON} = 13 kΩ

图 8-18. Cable Compensation Voltage vs Load Current

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8.8 Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 8.2 µH, C_{OUT_CSP} = 66 µF, C_{OUT_CSN} = 0.1 µF, C_{BUS} = 1 µF, T_A = 25 °C.

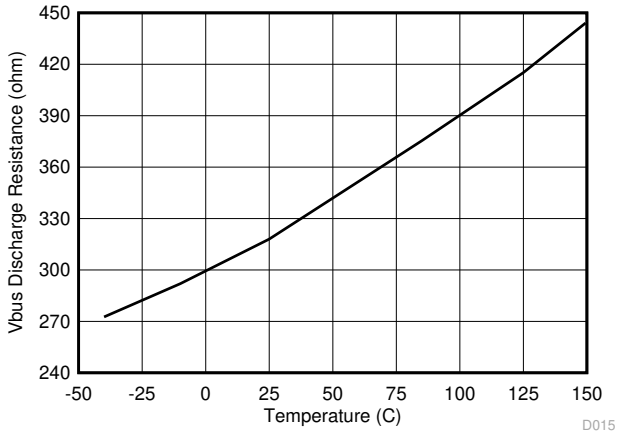


图 8-19. V_{BUS} Discharge Resistance vs Junction Temperature

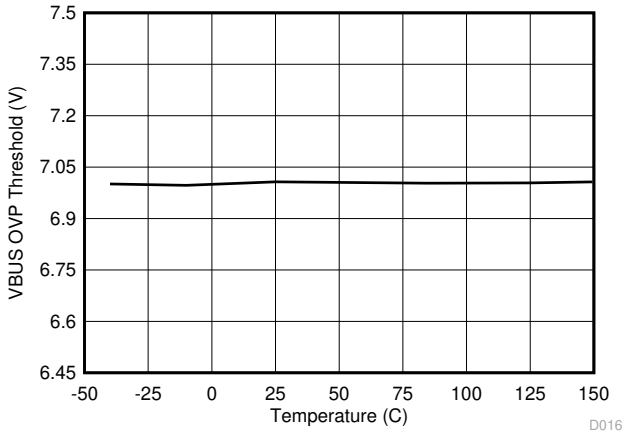


图 8-20. V_{BUS} Overvoltage Protection Threshold vs Junction Temperature

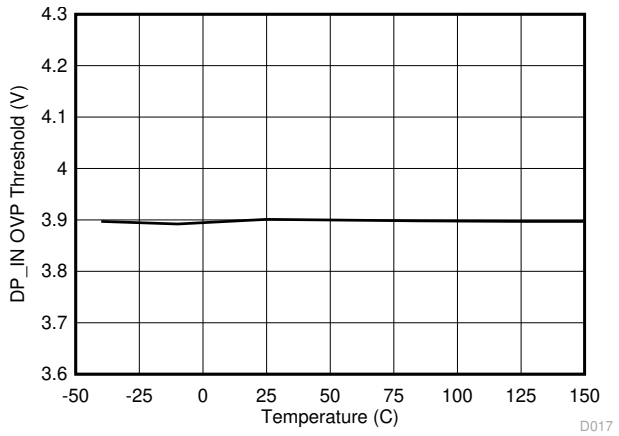


图 8-21. DP_IN Overvoltage Protection Threshold vs Junction Temperature

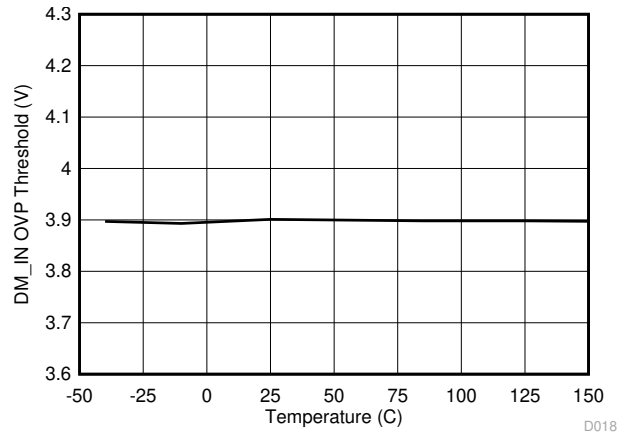
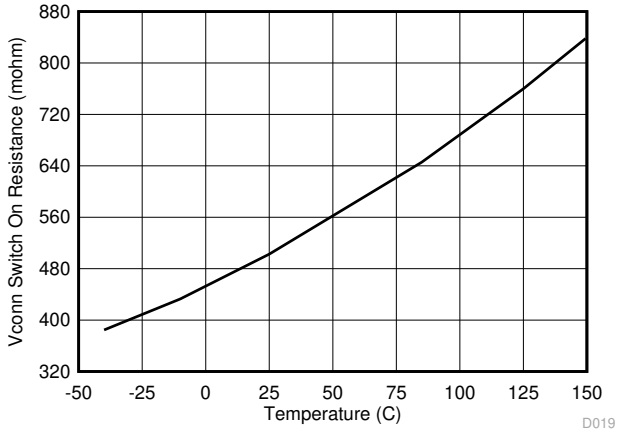
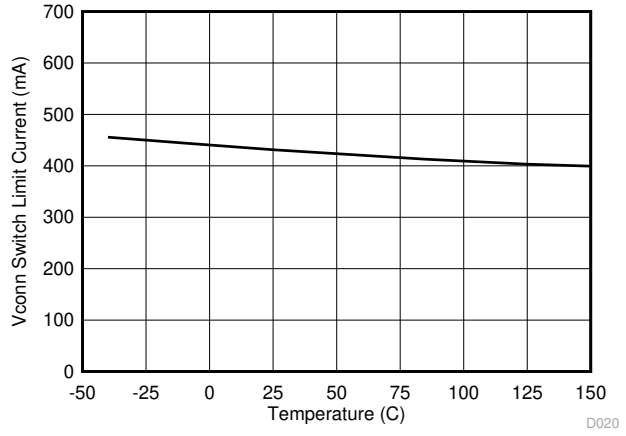


图 8-22. DM_IN Overvoltage Protection Threshold vs Junction Temperature



V_{CONN} = 5V

图 8-23. V_{CONN} Current Limiting Switch On Resistance vs Junction Temperature



V_{CONN} = 5 V

图 8-24. V_{CONN} Switch Current Limit vs Junction Temperature

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8.8 Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 8.2 µH, C_{OUT_CSP} = 66 µF, C_{OUT_CSN} = 0.1 µF, C_{BUS} = 1 µF, T_A = 25 °C.

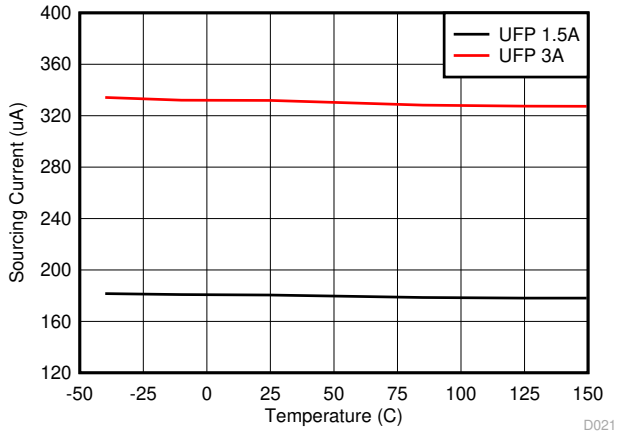


图 8-25. CC Sourcing Current vs Junction Temperature

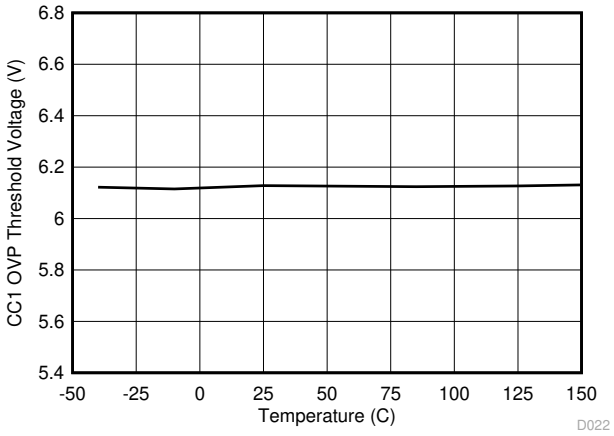
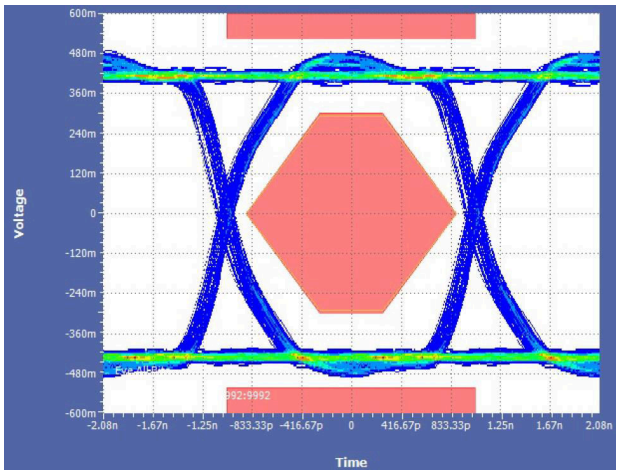
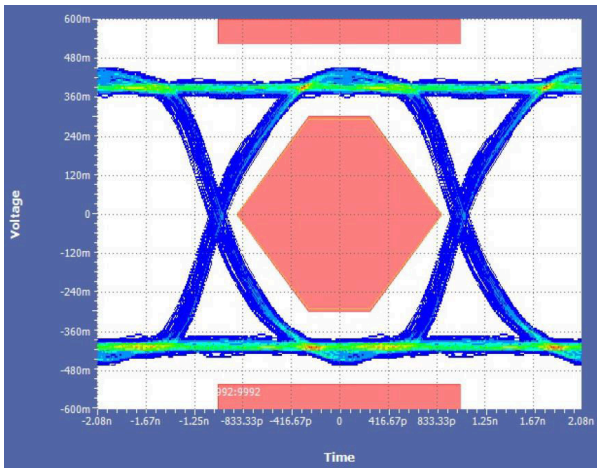


图 8-26. CC1 Overvoltage Protection Threshold vs Junction Temperature



Measured Source with 10-cm cable

图 8-27. Bypassing the TPS25830A-Q1 Data Switch



Measured on TPS25830-Q1 EVM with 10-cm cable

图 8-28. Through the TPS25830A-Q1 Data Switch



图 8-29. Data Transmission Characteristics vs Frequency (TPS25830A-Q1)



图 8-30. Off-State Data-Switch Isolation vs Frequency (TPS25830A-Q1)

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8.8 Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 8.2 µH, C_{OUT_CSP} = 66 µF, C_{OUT_CSN} = 0.1 µF, C_{BUS} = 1 µF, T_A = 25 °C.

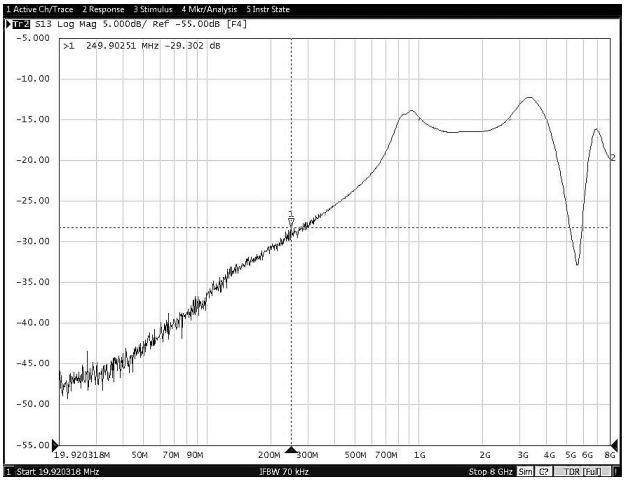

图 8-31. On-State Cross-Channel Isolation vs Frequency (TPS25830A-Q1)

9 Parameter Measurement Information

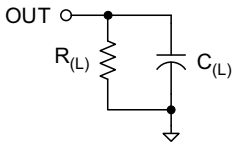

图 9-1. V_{CONN} Switch Rise-Fall Test Load Figure

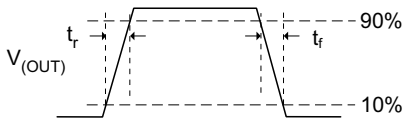

图 9-2. V_{CONN} Switch Rise-Fall Timing

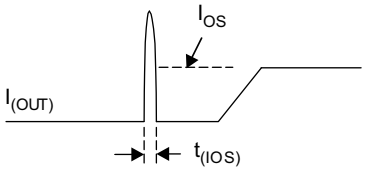

图 9-3. Short-Circuit Parameters

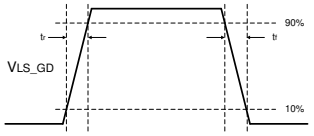

图 9-4. NFET Gate Drive Rise and Fall Time

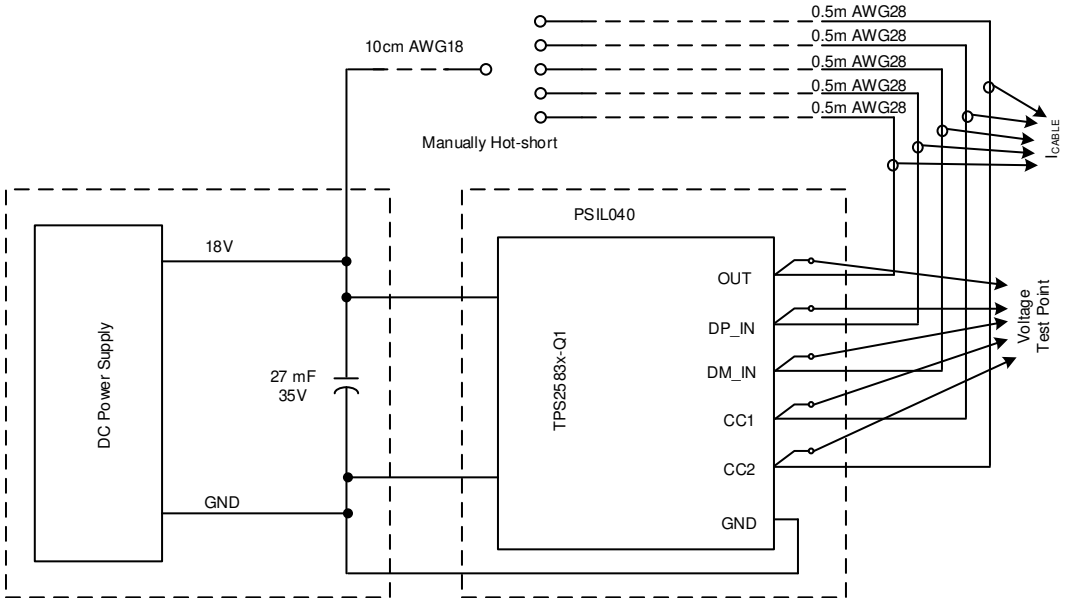

图 9-5. Short-to-Battery System Test Setup

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10 Detailed Description

10.1 Overview

The TPS2583xA-Q1 are full-featured solutions for implementing a compact USB charging port with support for both Type-C and BC1.2 standards. Both devices contain an efficient 36-V buck regulator power source capable of providing up to 3.5 A of output current at 5.10 V (nominal). System designers can optimize efficiency or solution size through careful selection of switching frequency over the range of 300 to 2200 kHz with sufficient margin to operate above or below the AM radio frequency band. In devices, the buck regulator operates in forced PWM mode ensuring fixed switching frequency regardless of load current. Spread-spectrum frequency dithering reduces harmonic peaks of the switching frequency potentially simplifying EMI filter design and easing compliance.

Current sensing with a precision high-side current sense amplifier enables an accurate, user programmable overcurrent limit setting; and programmable linear cable compensation to overcome IR losses when powering remote USB ports.

The CTRL1 and CTRL2 pins set the operating mode for the TPS2583xA-Q1 device. The device can support CDP, SDP or Client configurations.

The TPS25830A-Q1 integrates high band-width (800 MHz) USB switches, includes short to V_{BAT} and short to V_{BUS} protection as well as IEC61000-4-2 electrostatic discharge clamps to protect the host from potentially damaging overvoltage conditions.

The TPS25832A-Q1 integrates high band-width (800 MHz) USB switches, includes short to V_{BUS} protection as well as IEC61000-4-2 electrostatic discharge clamps, but does not support short to V_{BAT} protection.

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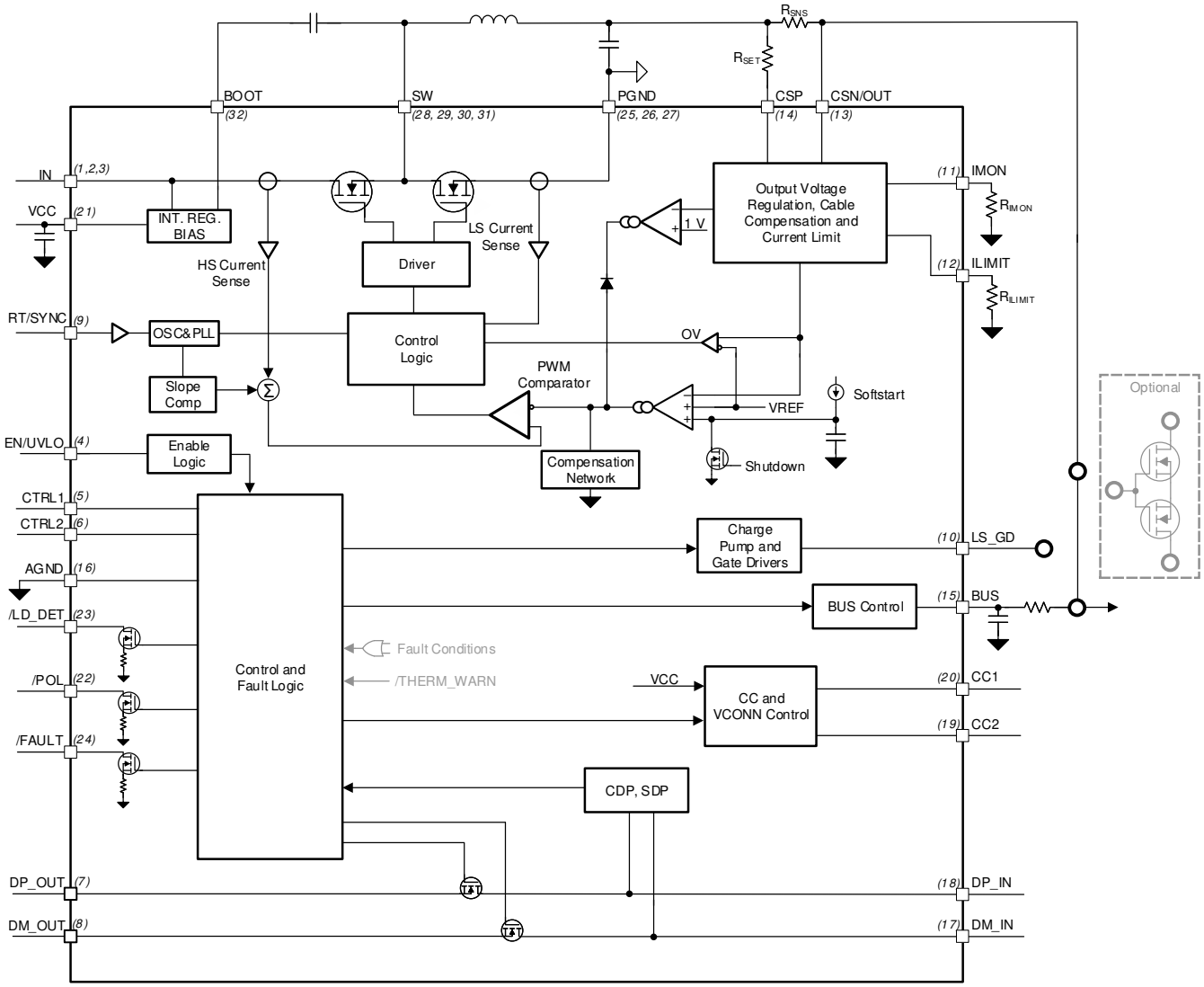
10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Buck Regulator

The following operating description of the TPS2583xA-Q1 will refer to the *Functional Block Diagram* and to the waveforms in 图 10-1. TPS2583xA-Q1 is a step-down synchronous buck regulator with integrated high-side (HS) and low-side (LS) switches (synchronous rectifier). The TPS2583xA-Q1 supplies a regulated output voltage by turning on the HS and LS NMOS switches with controlled duty cycle. During high-side switch ON time, the SW pin voltage swings up to approximately V_{IN}, and the inductor current i_L increase with linear slope (V_{IN} – V_{OUT}) / L. When the HS switch is turned off by the control logic, the LS switch is turned on after an anti-shoot-through dead time. Inductor current discharges through the LS switch with a slope of – V_{OUT} / L. The control parameter of a buck converter is defined as Duty Cycle D = t_{ON} / T_{SW}, where t_{ON} is the high-side switch ON time and T_{SW} is the switching period. The regulator control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = V_{OUT} / V_{IN}.

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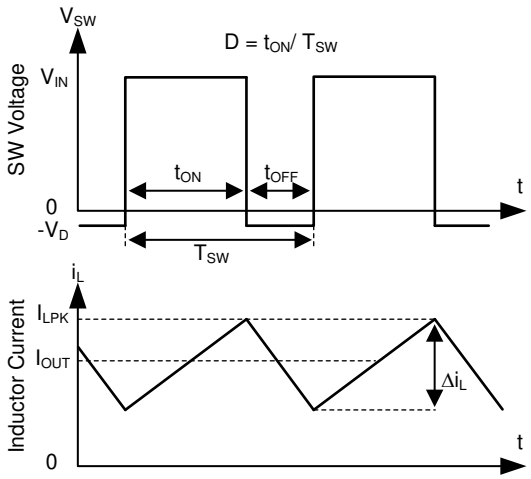

图 10-1. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The TPS2583xA-Q1 employs fixed frequency peak current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current threshold to control the ON time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, makes it easy to design, and provides stable operation with a reasonable combination of output capacitors. TPS2583xA-Q1 operates in FPWM mode for low output voltage ripple, tight output voltage regulation, and constant switching frequency.

10.3.2 Enable/UVLO and Start-Up

The voltage on the EN/UVLO pin controls the ON or OFF operation of TPS2583xA-Q1. An EN/UVLO pin voltage higher than $V_{EN/UVLO-H}$ is required to start the internal regulator and begin monitoring the CCn lines for a valid Type-C connection. The internal USB monitoring circuitry is on when V_{IN} is within the operation range and the EN/UVLO threshold is cleared; however, the buck regulator does not begin operation until a valid USB Type-C detection has been made. This feature ensures the "cold socket" (0 V) USB Type-C V_{BUS} requirement is met. The EN/UVLO pin is an input and can not be left open or floating. The simplest way to enable the operation of the TPS2583xA-Q1 is to connect the EN to V_{IN}. This allows self-start-up of the TPS2583xA-Q1 when V_{IN} is within the operation range.

DP and DM data switch will also be turned on after the EN/UVLO pin set high.

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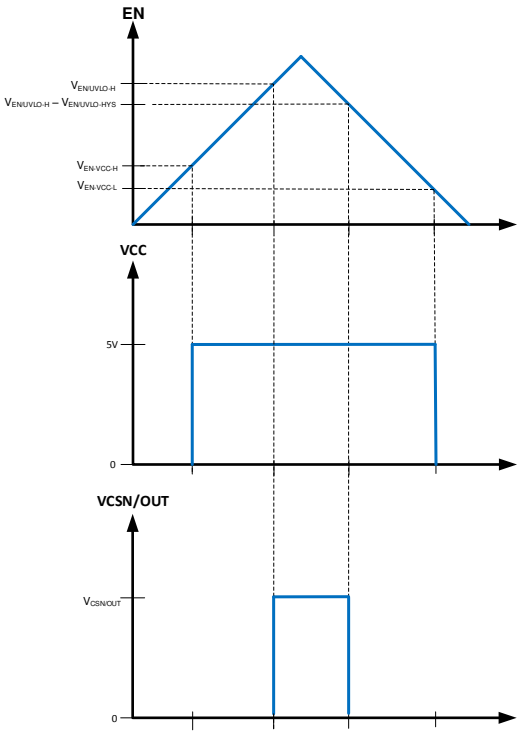

图 10-2. Precision Enable Behavior

Many applications will benefit from the employment of an enable divider R_{ENT} and R_{ENB} (图 10-3) to establish a precision system UVLO level for the TPS2583xA. The system UVLO can be used for sequencing, ensuring reliable operation, or supply protection, such as a battery discharge level. To ensure the USB port V_{BUS} is within the 5-V operating range as required for USB compliance (refer to *USB.org* for the latest USB specifications and requirements), it is suggested that the R_{ENT} and R_{ENB} resistors be chosen so that the TPS2583xA-Q1 enables when V_{IN} is approximately 6 V. Considering the drop out voltage of the buck regulator and IR loses in the system, 6 V provides adequate margin to maintain V_{BUS} within USB specifications. If system requirements such as a warm crank (start) automotive scenario require operation with V_{IN} < 6 V, the values of R_{ENT} and R_{ENB} can be calculated assuming a lower V_{IN}. An external logic signal can also be used to drive EN/UVLO input when a microcontroller is present and it is desirable to enable or disable the USB port remotely for other reasons.

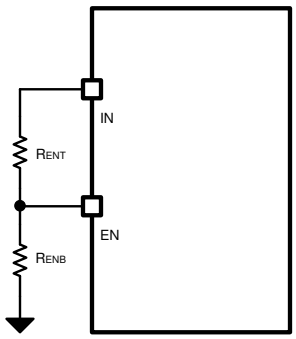

图 10-3. System UVLO by Enable Divider

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UVLO configuration using external resistors is governed by the following equations:

$$R_{ENT} = (\frac{V_{IN(ON)}}{V_{EN/UVLO_H}} - 1) \times R_{ENB} \quad (1)$$

$$V_{IN(OFF)} = V_{IN(ON)} \times (1 - \frac{V_{EN/UVLO_HYS}}{V_{EN/UVLO_H}}) \quad (2)$$

Example:

$V_{IN(ON)}$ = 6 V (user choice)

R_{ENB} = 5 kΩ (user choice)

R_{ENT} = [($V_{IN(ON)}$ / $V_{EN/UVLO_H}$) - 1] × R_{ENB}= 19.6 kΩ. Choose standard 20 kΩ.

Therefore $V_{IN(OFF)}$ = 6 V × [1 - (0.09 V / 1.2 V)] = 5.55 V

A typical start-up waveform is shown in 图 10-4, indicating typical timings when R_d connected to CC line. The rise time of DCDC VBUS voltage is about 5 ms.

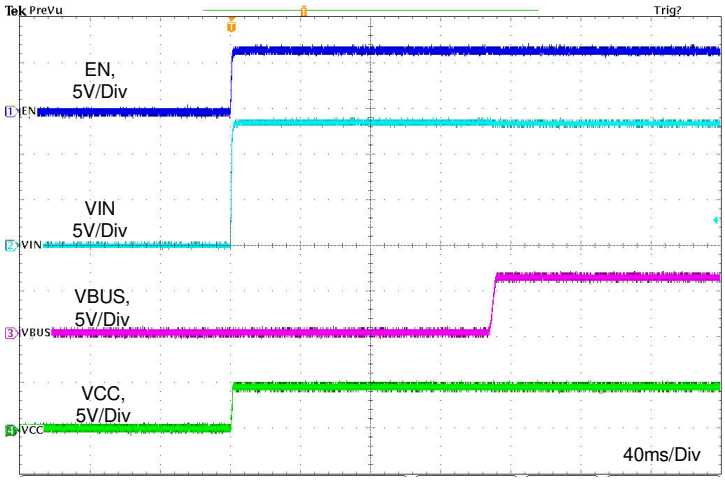

图 10-4. Typical Start-Up Behavior, V_{IN} = 13.5 V, CC1 = R_d, R_{IMON} = 12.6 kΩ

For TPS2583xA-Q1, the pin voltage must meet the requirement below during 150 ms (typical) Rd assert deglitch time, see 图 10-5:

- V_{BUS} < 0.8 V (typical), per Type-C requirement;
- V_{Dx_OUT} < 2.2 V (typical);
- V_{Dx_IN} < 1.5 V (typical);

After the TPS2583xA-Q1 Rd assert deglitch time, there is no additional requirement on these pins. In a real application, $\overline{LD_DET}$ pin can be used to configure the timing sequence.

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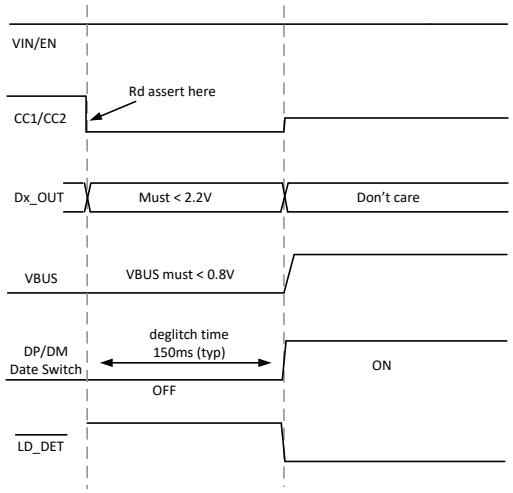

图 10-5. TPS2583xA-Q1 Pin Voltage Requirement Under CDP/SDP Mode

10.3.3 Switching Frequency and Synchronization (RT/SYNC)

The switching frequency of the TPS2583xA-Q1 can be programmed by the resistor R_T from the RT/SYNC pin and GND pin. To determine the RT resistance, for a given switching frequency, use Equation 3:

$$R_{RT}(k\Omega) = 27767 \times f_{sw}^{-1.0551}(kHz) \quad (3)$$

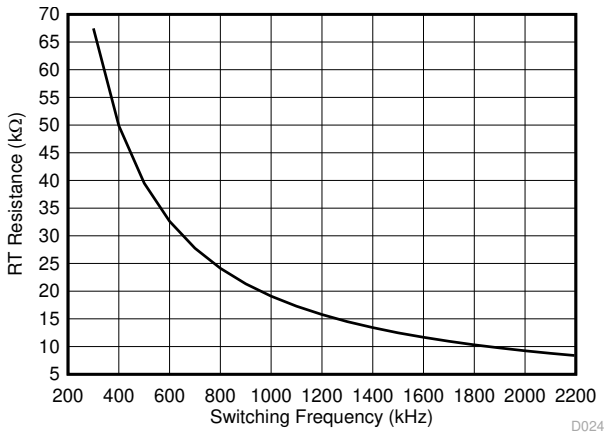

图 10-6. RT Set Resistor vs Switching Frequency

Typical RT resistors values are listed in 表 10-1.

表 10-1. Setting the Switching Frequency with RT

RT (kΩ)	SWITCHING FREQUENCY (kHz)
68.1	300
49.9	400
39.2	500
19.1	1000
12.4	1500
9.09	2000
8.66	2100
8.25	2200

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TPS2583xA-Q1 switching action can be synchronized to an external clock from 300 kHz to 2.3 MHz.
The RT/SYNC pin can be used to synchronize the internal oscillator to an external clock. The internal oscillator can be synchronized by AC coupling a positive edge into the RT/SYNC pin. The AC coupled peak-to-peak voltage at the RT/SYNC pin must exceed the SYNC amplitude threshold of 2.0 V (min) to trip the internal synchronization pulse detector, and the minimum SYNC clock ON and OFF time must be longer than 100 ns (typical). When using a low impedance signal source, the frequency setting resistor R_T is connected in parallel with an AC coupling capacitor C_{COUP} to a termination resistor R_{TERM} (for example, 50 Ω). The two resistors in series provide the default frequency setting resistance when the signal source is turned off. A 10-pF ceramic capacitor can be used for C_{COUP}. 图 10-7 shows the device synchronized to an external clock.

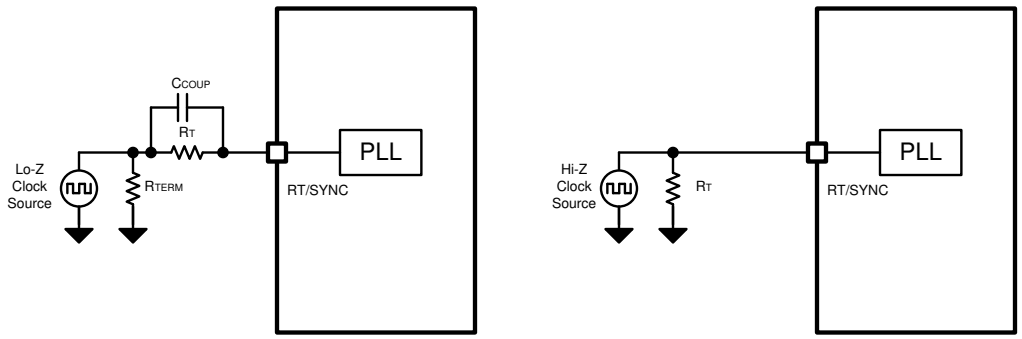

图 10-7. Synchronize to External Clock

In order to avoid AM radio frequency band and maintain proper regulation when minimum ON-time or minimum OFF-time is reached, the TPS2583xA-Q1 implements a frequency foldback scheme depending on VIN voltage, refer to 图 8-11.

- When 8 V < VIN ⩽ 19 V, the switching frequency of TPS2583xA-Q1 is determined by R_T resistor or external sync clock.
- When VIN ⩽ 8 V, the switching frequency of TPS2583xA-Q1 is set to default 420 kHz, regardless of R_T resistor setting or external sync clock.
- When VIN > 19 V, the switching frequency of TPS2583xA-Q1 is set to default 420 kHz, regardless of R_T resistor setting or external sync clock.

图 10-8, 图 10-9 and 图 10-10 show the device switching frequency and behavior under different VIN voltage and R_T = 8.66 kΩ.

图 10-11, 图 10-12 and 图 10-13 show the device switching frequency and behavior under different VIN voltage and synchronized to an external 2.1-M system clock.

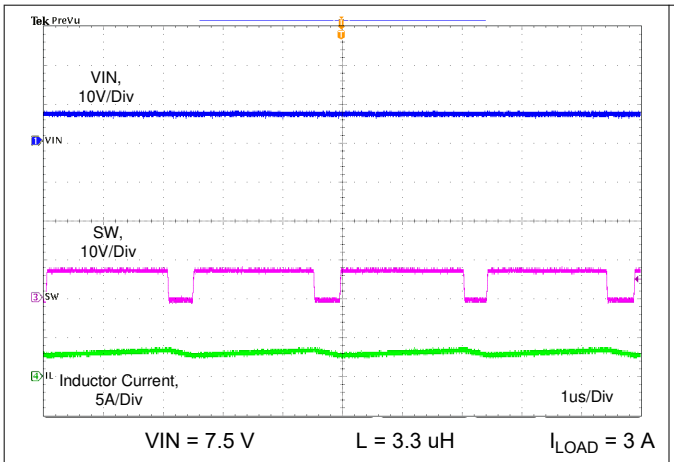

图 10-8. Switching Frequency When R_T = 8.66 kΩ

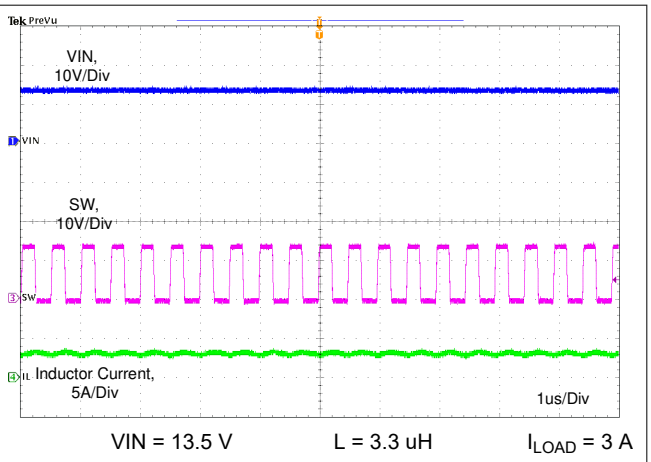

图 10-9. Switching Frequency When R_T = 8.66 kΩ

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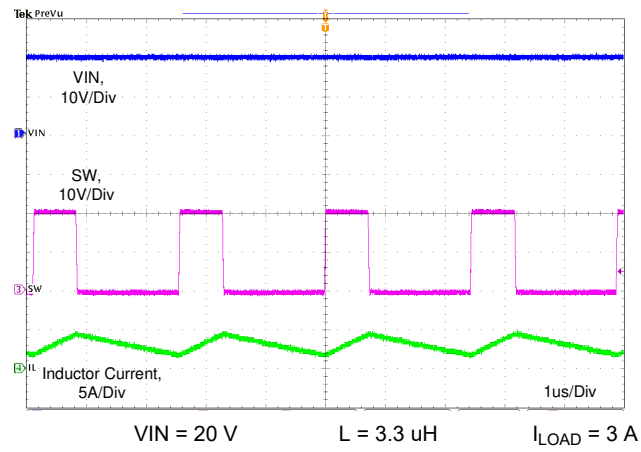

图 10-10. Switching Frequency When R_T = 8.66 kΩ

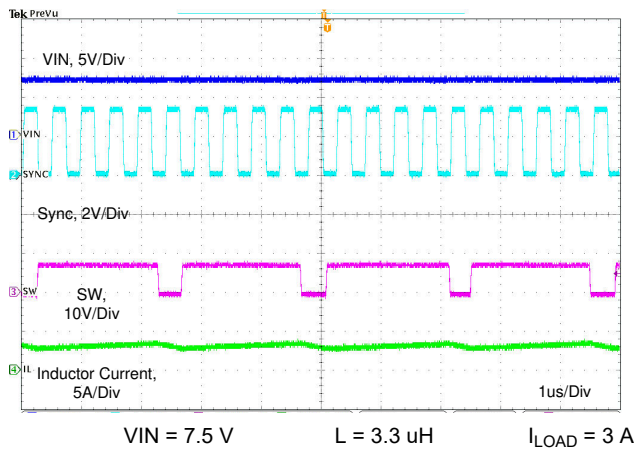

图 10-11. Synchronizing to External 2.1-MHz Clock

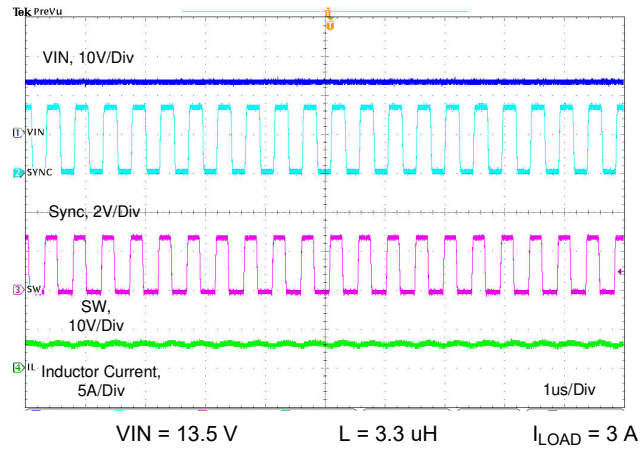

图 10-12. Synchronizing to External 2.1-MHz Clock

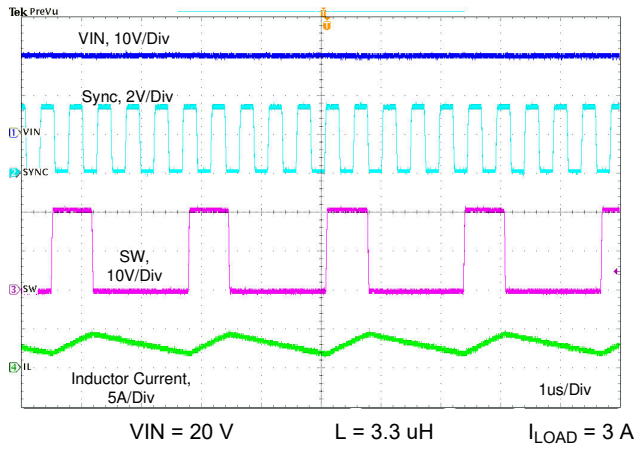

图 10-13. Synchronizing to External 2.1-MHz Clock

10.3.4 Spread-Spectrum Operation

In order to reduce EMI, the TPS2583xA-Q1 introduces frequency spread spectrum. The spread spectrum is used to eliminate peak emissions at specific frequencies by spreading emissions across a wider range of frequencies than a part with fixed frequency operation. In most systems, low frequency conducted emissions from the first few harmonics of the switching frequency can be easily filtered. A more difficult design criterion is reduction of emissions at higher harmonics which fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node. The TPS2583xA-Q1 devices use ±6% spread of switching frequencies with 1/256 swing frequency.

The spread spectrum function is only available when using the TPS2583xA-Q1 internal oscillator. If the RT/SYNC pin is synchronized to an external clock, the spread spectrum function will be turned off.

10.3.5 VCC, VCC_UVLO

The TPS2583xA-Q1 integrates an internal LDO to generate V_{CC} for control circuitry and MOSFET drivers. The nominal voltage for V_{CC} is 5 V. The V_{CC} pin is the output of an LDO and must be properly bypassed. A high quality ceramic capacitor with a value of 2.2 µF to 4.7 µF, 10 V or higher rated voltage should be placed as close as possible to VCC and grounded to the PGND ground pin. The V_{CC} output pin should not be loaded with more than 5 mA, or shorted to ground during operation.

In applications where V_{CONN} support is required, the V_{CC} pin can be over-driven with an external 5-V LDO capable of sourcing at least 300 mA. In this operating mode the external LDO is the source for the buck low-side switch gate drive as well as power to the internal V_{CONN} mux.

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Note if using external 5-V LDO for V_{CONN} power, the timing sequence below must be required. External V_{CONN} power can not be enabled before the TPS2583xA-Q1 is enabled, external V_{CONN} must be disabled before the TPS2583xA-Q1 is disabled. In a real application, customer can tie the EN of external 5-V LDO and EN of TPS2583xA-Q1 together to meet the timing requirement.

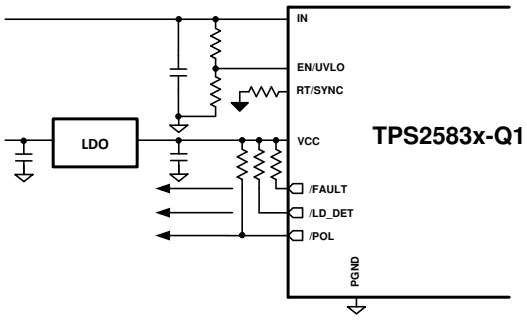

图 10-14. V_{CONN} Source Using External LDO

10.3.6 Minimum ON-Time, Minimum OFF-Time

Minimum ON-time, T_{ON_MIN}, is the smallest duration of time that the HS switch can be on. T_{ON_MIN} is typically 105 ns in the TPS2583xA. Minimum OFF-time, T_{OFF_MIN}, is the smallest duration that the HS switch can be off. T_{OFF_MIN} is typically 80 ns in the TPS2583xA-Q1. In CCM (FPWM) operation, T_{ON_MIN} and T_{OFF_MIN} limit the voltage conversion range given a selected switching frequency.

The minimum duty cycle allowed is:

$$D_{MIN} = T_{ON_MIN} \times f_{sw} \tag{4}$$

And the maximum duty cycle allowed is:

$$D_{MAX} = 1 - T_{OFF_MIN} \times f_{sw} \tag{5}$$

Given fixed T_{ON_MIN} and T_{OFF_MIN}, the higher the switching frequency the narrower the range of the allowed duty cycle.

10.3.7 Internal Compensation

The TPS2583xA-Q1 is internally compensated as shown in 图 10-1. The internal compensation is designed such that the loop response is stable over the specified operating frequency and output voltage range. The TPS2583x-Q1 is optimized for transient response over the range 300 kHz ⩽ fsw ⩽ 2300 kHz.

10.3.8 Bootstrap Voltage (BOOT)

The TPS2583xA-Q1 provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW pins provides the gate drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET is off and the low-side switch conducts. The recommended value of the BOOT capacitor is 0.1 μF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended for stable performance over temperature and voltage.

10.3.9 R_{SNS}, R_{SET}, R_{ILIMIT} and R_{IMON}

The programmable current limit threshold and full-scale cable compensation voltage are determined by the values of the R_{SNS}, R_{SET}, R_{ILIMIT}, and R_{IMON} resistors. Refer to 图 10-15.

- R_{SNS} is the current sense resistor. The recommended voltage across R_{SNS} under current limit should be approximately 50 mV as a compromise between accuracy and power dissipation. For example, if current

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limiting is desired for $I_{OUT(MAX)} \geqslant 3.3$ A, then R_{SNS} = 0.05 V / 3.3 A = 0.01515 Ω. Choose a standard value of 15 mΩ.

- R_{SET} determines the input current to the transconductance amplifier and current mirror. The amplifier balances the voltage to be equal to that across R_{SNS}. Choose a R_{SET} value to produce an I_{SET} current between 75 – 180 µA at the desired $I_{OUT(MAX)}$. Considering 50 mV across R_{SET}, a value of 300 Ω will provide approximately 166 µA of I_{SET} current to the amplifier and mirror circuit. Care should be taken to limit the I_{SET} current below 200 µA to avoid saturating the internal amplifier circuit.
- R_{ILIMIT} in conjunction with the 0.5 × I_{SET} current produces a voltage on the ILIMIT pin which is proportional to the load current flowing in R_{SNS}. See *Current Limit Setting using R_{ILIMIT}* for details on setting the current limit.
- R_{IMON} in conjunction with the 0.5 × I_{SET} current produces a voltage on the IMON pin which is proportional to the load current flowing in R_{SNS}. See *Cable Compensation* for details on setting the current limit.

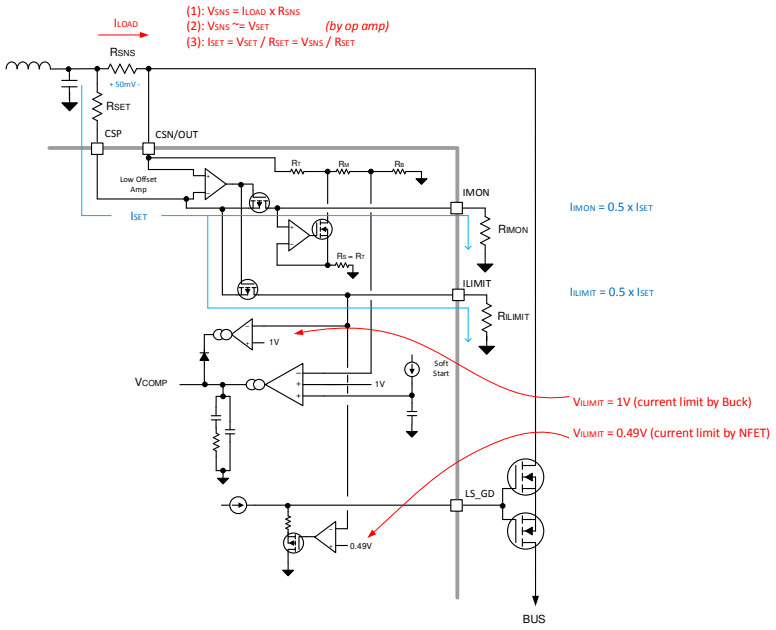

图 10-15. Current Limit and Cable Compensation Circuit

10.3.10 Overcurrent and Short Circuit Protection

For maximum versatility, TPS2583xA-Q1 includes both a precision, programmable current limit and cycle-by-cycle current limit to protect the USB port from extreme overload conditions. In most applications the R_{ILIMIT} resistor in conjunction with the selection of R_{SNS} and R_{SET} will determine the overload threshold. The cycle-by-cycle current limit will serve as a backup means of protection in the event R_{ILIMIT} is shorted to ground disabling the programmable current limit function.

TPS2583xA-Q1 also implements a internal circuit to meet MFi over-current requirement.

10.3.10.1 Current Limit Setting using R_{ILIMIT}

Refer to 图 10-15. The TPS2583xA-Q1 can establish current limit by two methods.

- Using external a single or back-to-back N-Channel MOFETs between CSN/OUT and BUS: A voltage of 0.49 V on the ILIMIT pin initiates current limiting using the external MOSFET by decreasing the LS_GD voltage causing the FET to operate in the saturation region. To protect the MOSFETs from damage a hiccup timer limits the duty cycle to prevent thermal runaway. Refer to the *Switching Characteristics* for MOSFET hiccup timing.
- Buck average current limit: No MOSFET, CSN/OUT connected to BUS. In this configuration a voltage of 1 V across R_{ILIMIT} on the ILIMIT pin initiates average current limiting of the buck regulator.

The detailed current limit is described below:

- With external MOSFET 图 10-16:

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- Isolating a fault on the USB port from other loads connected to the CSP output of the TPS2583xA-Q1. In some applications, it may be useful to power additional circuitry (example USB HUB) from the output of the TPS2583xA-Q1 and maintain operation of these circuits in the event of a short circuit downstream of the BUS pin. To prevent triggering the MOSFET current limit below the programmed ILIMIT threshold, external circuits should be supplied after the inductor and before the current sense resistor, R_{SNS}.
- After R_{SNS} and R_{SET} are determined and the full load I_{SET} current is known, the resistor value R_{ILIMIT} can be determined by:

$$R_{ILIMIT} = \frac{0.49 \times R_{SET}}{0.5 \times (I_{LIMIT} \times R_{SNS} + 0.0007)} \quad (6)$$

- In most case, the recommended voltage across R_{SNS} under current limit should be approximately 50 mV as a compromise between accuracy and power dissipation. While in some application, R_{ILIMIT} is the only resistor that can be changed to achieve different current limit. Typical R_{ILIMIT} resistors value are listed in 表 10-2 given the condition R_{SNS}= 15 mΩ and R_{SET}= 300 Ω

表 10-2. Setting the Current Limit with R_{ILIMIT}

CURRENT-LIMIT THRESHOLD (mA)	R_{ILIMIT} (kΩ)	
	WITH EXTERNAL MOSFET	BUCK AVERAGE
700	26.1	53.6
1500	12.7	26.1
1700	11.3	22.6
2700	7.15	14.7
3000	6.49	13
3400	5.62	11.5
3800	5.11	10.5

- Buck Average Current Limit 图 10-17:
  1. CSN/OUT connected directly to BUS. The TPS2583xA-Q1 can operate as a stand-alone USB charging port. In this configuration, the internal buck regulator operates with average current limiting as programmed by the ILIMIT pin, potentially producing less heat compared to N-channel MOSFET current limiting.
  2. After R_{SNS} and R_{SET} are determined and the full load I_{SET} current is known, the resistor value R_{ILIMIT} can be determined by:

$$R_{ILIMIT} = \frac{1 \times R_{SET}}{0.5 \times (I_{LIMIT} \times R_{SNS} + 0.0007)} \quad (7)$$

  3. Typical R_{ILIMIT} resistors value are listed in 图 10-16, given the condition R_{SNS}= 15 mΩ and R_{SET} = 300 Ω.

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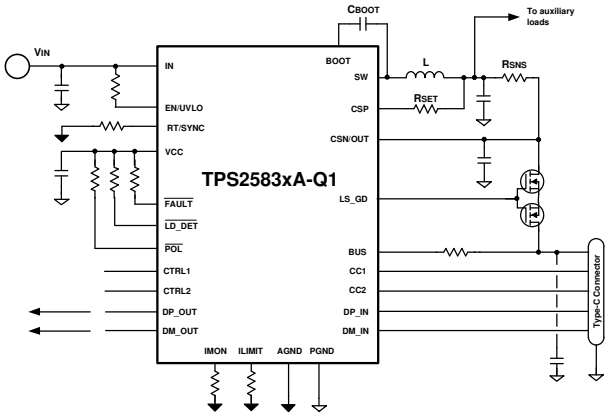

图 10-16. TPS2583xA-Q1 Current Limit with External MOSFET

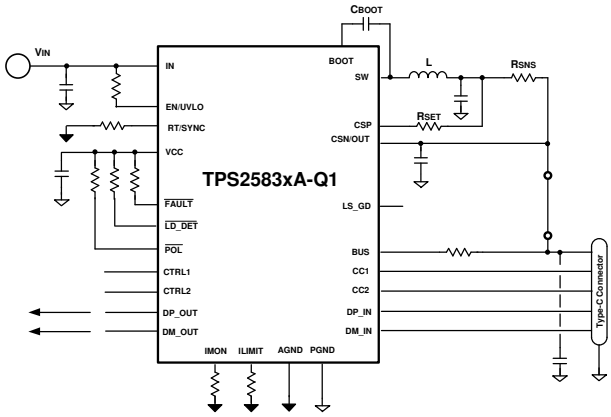

图 10-17. TPS2583xA-Q1 Buck Average Current Limit

10.3.10.2 Current Limit Setting for MFI OCP

Apple has defined new overcurrent protection requirements in its latest MFI spec. TPS2583xA-Q1 also implements a novel current limit inside to meet the MFI OC requirement.

The settings are described below:

- With external MOSFET: When TPS2583xA-Q1 uses an external FET for current limit, it actually has two current limit threshold. The 1st threshold I_{LIMIT1} is determined by R_{LIMIT} according to equation 6. The 2nd threshold I_{LIMIT2} equals to 1.6 times of I_{LIMIT1}.
  - Case 1: If the load current I_{BUS} is in the range $I_{LIMIT2} > I_{BUS} > I_{LIMIT1}$, and the duration < $t_{OC_HIC_DEG}$, the external MOSFET will remain on and V_{BUS} will stay unchanged, as shown in 图 10-18.

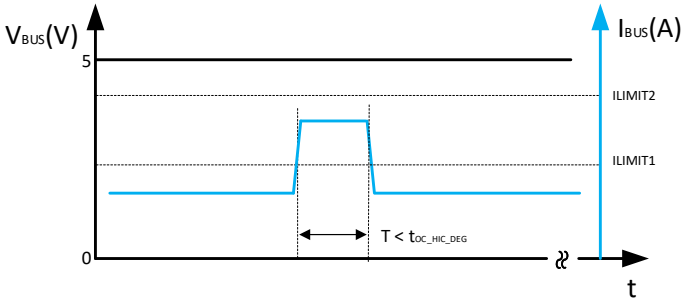

图 10-18. Two level Current Limit Methodology with ext MOSFET Case 1

  - Case 2: If the load current I_{BUS} is in the range $I_{LIMIT2} > I_{BUS} > I_{LIMIT1}$ and the duration > $t_{OC_HIC_DEG}$, the external MOSFET will current limit to I_{LIMIT1}, then enter hiccup mode with 2 ms of on-time and 263 ms of off-time, as shown in 图 10-19. When the load current decreases below I_{LIMIT1} and continues > $t_{OC_HIC_RST}$, the external MOSFET will resume always on.

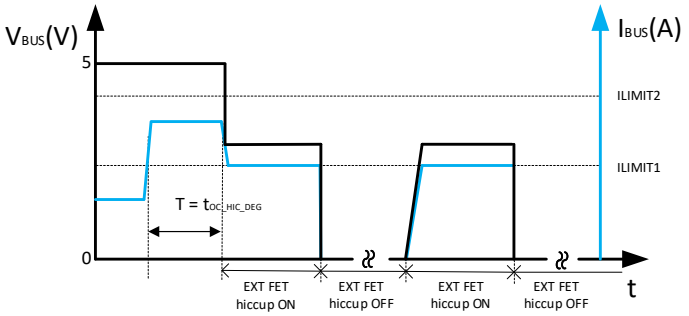

图 10-19. Two Level Current Limit Methodology with ext MOSFET Case 2

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- Case 3: If the load current I_{BUS} > I_{LIMIT2}, the external MOSFET will current limit to I_{LIMIT1} immediately, then enter hiccup mode with 2 ms of on-time and 263 ms of off-time, as shown in 图 10-20. When the load current I_{BUS} < I_{LIMIT1} for $t_{OC_HIC_RST}$, the external MOSFET will resume always on.

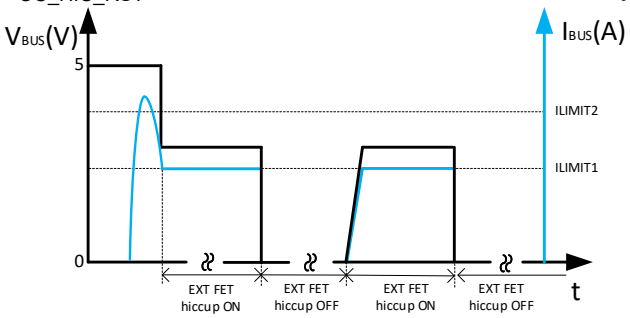

图 10-20. Two Level Current Limit Methodology with ext MOSFET Case 3

- Buck average current limit
  - When TPS2583xA-Q1 uses Buck average current limit, it has only one current limit threshold determined by R_{LIMIT} according to 方程式 6.
  - In order to meet the MFI OC requirement, an RC network is needed in parallel with R_{limit} resistor as shown in 图 10-21. Suggest selecting R_{para} = R_{limit}, C_{para} = 100 nF.

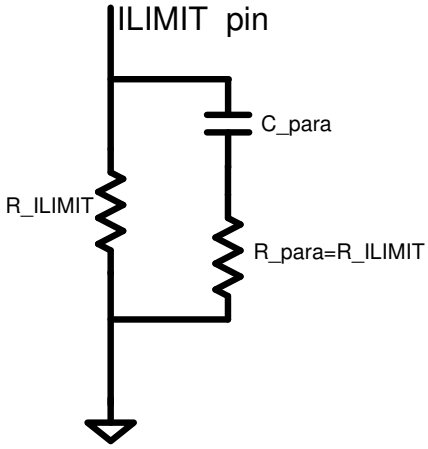

图 10-21. RC Network in Parallel with R_{limit}

10.3.10.3 Buck Average Current Limit Design Example

To start the procedure, the $I_{LOAD(MAX)}$, R_{SNS}, R_{SET}, must be known.

1. Determine I_{LIMIT}, usually choose I_{LIMIT}= $I_{LOAD(MAX)}$ / (1 - 10%).
2. Determine R_{SNS} to achieve 50 mV at current limit. For 3-A Type-C load current, choose I_{LIMIT} = 3.3 A. R_{SNS} = (0.05 V / 3.3 A) = 15 mΩ.
3. Choose R_{SET} = 300 Ω
4. According to 方程式 6, R_{LIMIT} = 300 / (0.5 × (3.3 × 0.015 + 0.0007)) = 11.95 kΩ.
5. Choose standard 11.8 kΩ.

10.3.10.4 External MOSFET Gate Drivers

The TPS2583xA-Q1 has integrated NFET gate drivers and can support current limit with external NFET. Refer to 图 10-16.

The LS_GD pin of TPS2583xA-Q1 can source 3-uA (typical) current to enhance the external MOSFET. A 6.2-V clamp between LS_GD and CSN/OUT pin limits the gate-to-source voltage. During DCDC start up, the LS_GD gate drivers begin to source current after $V_{CSN/OUT}$ reach 3 V. If the $V_{CSN/OUT}$ > 7.5 V or V_{BUS} > 7 V under overvoltage condition, the LS_GD will turn off immediately with 35-uA (typical) sink current.

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If load current above NFET current limit threshold, LS_GD will also turn off the NFET after 2 ms (typical) and enter hiccup mode to protect NFET from thermal issue. Refer to 图 11-26 for application waveform.

In real application, if V_{BUS} short to V_{BAT} function is needed, 20-V back-to-back NFET is suggested in circuit design.

10.3.10.5 Cycle-by-Cycle Buck Current Limit

The buck regulator cycle-by-cycle current limit on both the peak and valley of the inductor current. Hiccup mode will be activated if a fault condition persists to prevent over-heating.

High-side MOSFET overcurrent protection is implemented by the nature of the Peak Current Mode control. The HS switch current is sensed when the HS is turned on after a set blanking time. The HS switch current is compared to the output of the Error Amplifier (EA) minus slope compensation every switching cycle. Refer to *Functional Block Diagram* for more details. The peak current of HS switch is limited by a clamped maximum peak current threshold I_{HS_LIMIT} which is constant. So the peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

The current going through LS MOSFET is also sensed and monitored. When the LS switch turns on, the inductor current begins to ramp down. The LS switch will not be turned OFF at the end of a switching cycle if its current is above the LS current limit I_{LS_LIMIT}. The LS switch will be kept ON so that inductor current keeps ramping down, until the inductor current ramps below the LS current limit I_{LS_LIMIT}. Then the LS switch will be turned OFF and the HS switch will be turned on after a dead time. This is somewhat different than the more typical peak current limit, and results in Equation 8 for the maximum load current.

$$I_{OUT_MAX} = 0.5 \times (I_{LS_LIMIT} + I_{HS_LIMIT}) \tag{8}$$

If $V_{CSN/OUT}$ < 2-V typical due to a short circuit for 128 consecutive cycles, hiccup current protection mode will be activated. In hiccup mode, the regulator will be shut down and kept off for 118 ms typically, then TPS2583xA-Q1 will go through a normal re-start with soft start again. If the short-circuit condition remains, hiccup will repeat until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, prevents over-heating and potential damage to the device, and serves as a backup to the programmable current limit, see the *Current Limit Setting using R_{ILIMIT}* section. Once the output short is removed, the hiccup delay is passed, the output voltage recovers normally as shown in 图 11-23.

10.3.11 Overvoltage, IEC and Short to Battery Protection

The TPS25830A-Q1 integrates OVP and short to battery protection on VBUS, CC1, CC2, DM_IN and DP_IN pins. These pins can withstand voltage up to 18 V, and can protect upstream processor or Hub data line when overvoltage or short to battery condition occurs. Refer to 图 9-5 for short to battery test setup.

For more detailed TPS2583x-Q1 Short to Battery consideration and test report, please refer to TPS2583x-Q1 and TPS2584x-Q1 Short-to- Battery Application.

The TPS2583xA-Q1 also integrates IEC ESD cell on CC1, CC2, DP_IN and DM_IN pins.

10.3.11.1 V_{BUS} and $V_{CSN/OUT}$ Overvoltage Protection

The TPS2583xA-Q1 integrates overvoltage protection on both BUS and CSN/OUT pin to meet different application requirement.

BUS pin can withstand up to 18 V, and the OVP threshold is 7-V typical. Once overvoltage is detected on BUS pin, the LS_GD will turn off immediately, also $\overline{\text{FAULT}}$ asserts after 8-ms deglitch time. Once the excessive voltage is removed, the LS_GD will turn on again and $\overline{\text{FAULT}}$ deasserts.

CSN/OUT pin can withstand up to 20 V, and the OVP threshold is 7.5-V typical. Once overvoltage is detected on CSN/OUT pin, the buck converter will stop regulation, also LS_GD will turn off immediately. Once the excessive voltage is removed, the buck converter will resume and LS_GD turn on again.

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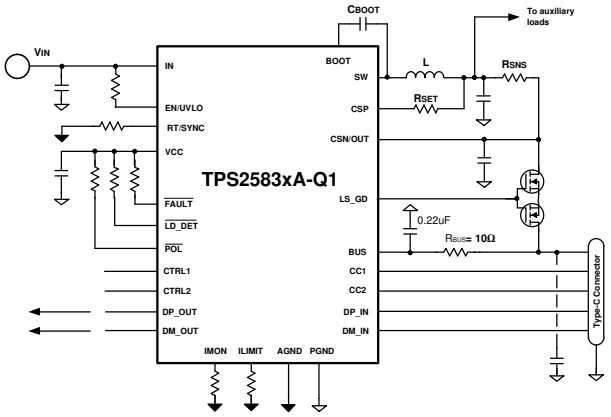

图 10-22. Current Limit with External MOSFET

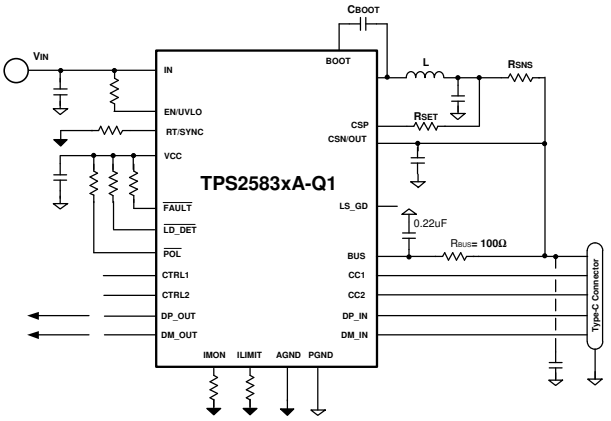

图 10-23. Buck Average Current Limit

TPS2583xA-Q1 is configured in external FET current limit mode as shown in 图 10-22. When short to battery occurs on BUS_Connector, the external MOSFET will be turn off immediately after BUS pin detect overvoltage. The $\overline{\text{FAULT}}$ signal will assert after 8ms deglitch time, see 图 11-35. With Back-to-back FET, the TPS2583xA-Q1 can withstand short to battery event even when Vin is off. A 10-Ω 0805 resistor is recommended between BUS pin and BUS_Connector.

TPS2583xA-Q1 is configured in buck average current limit mode as shown in 图 10-23. When short to battery occurs on BUS_Connector, the buck regulator will stop switching after CSN/OUT pin detect overvoltage. The $\overline{\text{FAULT}}$ signal will also assert after 8-ms deglitch time. A 100-Ω 0805 resistor is recommended between BUS pin and BUS_Connector in buck average current limit mode.

10.3.11.2 DP_IN and DM_IN Protection

DP_IN and DM_IN protection consists of IEC ESD and overvoltage protection.

The DP_IN and DM_IN pins integrate an IEC ESD cell to provide ESD protection up to ±15-kV air discharge and ±8-kV contact discharge per IEC 61000-4-2 (See the *ESD Ratings* section for test conditions). The IEC ESD performance of the TPS2583xA-Q1 device depends on the capacitance connected from BUS pin to GND. A 0.22-µF capacitor placed close to the BUS pin is recommended.

The ESD stress seen at DP_IN and DM_IN is impacted by many external factors like the parasitic resistance and inductance between ESD test points and the DP_IN and DM_IN pins. For air discharge, the temperature and humidity of the environment can cause some difference, so the IEC performance should always be verified in the end-application circuit.

Overvoltage protection (OVP) is provided for short-to-V_{BUS} or short-to-battery conditions in the vehicle harness, preventing damage to the upstream USB transceiver or hub. When the voltage on DP_IN or DM_IN exceeds 3.9 V (typical), the TPS25830A-Q1 device immediately turn off DP/DM switch, and responds to block the high-voltage reverse connection to DP_OUT and DM_OUT. $\overline{\text{FAULT}}$ signal will assert after 8-ms deglitch time (see 图 11-39).

For DP_IN and DM_IN, when OVP is triggered, the device turns on an internal discharge path with 416-kΩ resistance to ground. On removal of the overvoltage condition, the pin automatically turns off this discharge path and returns to normal operation by turning on the previously affected analog switch.

10.3.11.3 CC IEC and OVP Protection

CCx protection consists of IEC ESD and overvoltage protection.

The CC pins integrate an IEC ESD cell to provide ESD protection up to ±15-kV air discharge and ±8-kV contact discharge per IEC 61000-4-2 (see the *ESD Ratings* section for test conditions). Additional 0.22-uF capacitor placed close to the CC pin is recommended in real application.

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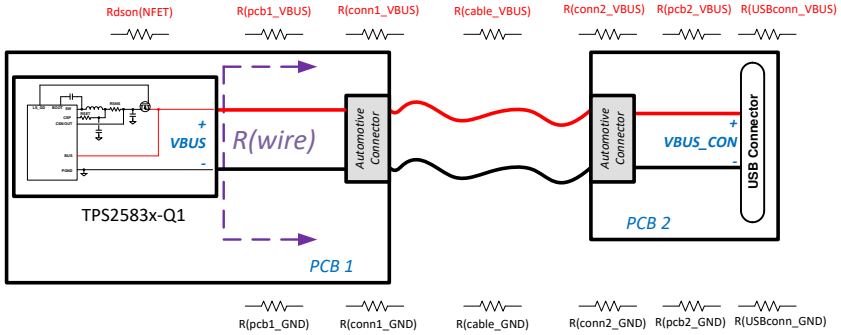
Overvoltage protection (OVP) is provided for short-to-V_{BUS} or short-to-battery conditions in the vehicle harness. When the voltage on CC1 or CC2 exceeds 6.1 V (typical), the TPS25830A-Q1 device immediately shuts off CC line. $\overline{FAULT}$ signal will assert after 8-ms deglitch time (see 图 11-37).

For CC1 and CC2, when OVP is triggered, the device turns on an internal discharge path with 55-kΩ resistance to ground. On removal of the overvoltage condition, the pin automatically turns off this discharge path and returns to normal operation.

10.3.12 Cable Compensation

When a load draws current through a long or thin wire, there is an IR drop that reduces the voltage delivered to the load. Cable droop compensation linearly increases the voltage at the CSN/OUT pin of TPS2583xA-Q1 as load current increases with the objective of maintaining V_{BUS_CON} (the bus voltage at the USB connector) at 5 V, regardless of load conditions. Most portable devices charge at maximum current when 5 V is present at the USB connector. 图 10-24 provides an example of resistor drops encountered when designing an automotive USB system with a remote USB connector location.



R(wire) = R(pcb1_VBUS) + R(conn1_VBUS) + R(cable_VBUS) + R(conn2_VBUS) + R(pcb2_VBUS) + R(USBconn_VBUS) + R(USBconn_GND) + R(pcb2_GND) + R(conn2_GND) + R(cable_GND) + R(conn1_GND) + R(pcb1_GND)

图 10-24. Automotive USB Resistances

The TPS2583xA-Q1 detects the load current and increases the voltage at the CSN/OUT pin to compensate the IR drop in the charging path according to the gain set by the R_{SNS}, R_{SET}, and R_{IMON} resistors as described in *R_{SNS}, R_{SET}, R_{ILIMIT}, and R_{IMON}*.

The amount of cable droop compensation required can be estimated by the following equation: $\Delta V_{OUT} = (R_{SNS} + R_{DSON_NFET} + R_{WIRE}) \times I_{BUS}$. R_{IMON} is then chosen by $R_{IMON} = (\Delta V_{OUT} \times R_{SET} \times 2) / (I_{BUS} \times R_{SNS})$, where ΔV_{OUT} is the desired cable droop compensation voltage at full load.

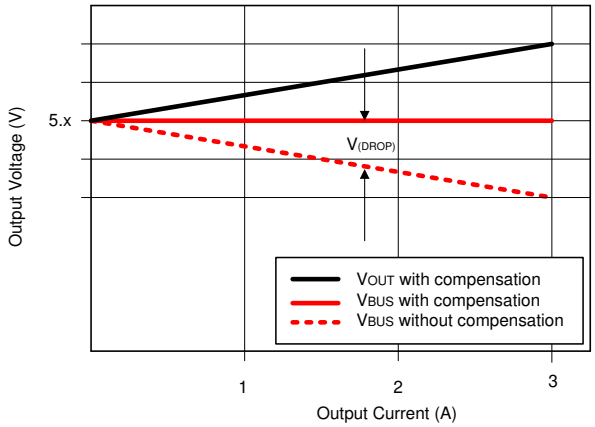


图 10-25. Voltage Drop

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Per *R_{SNS}, R_{SET}, R_{ILIMIT}, and R_{IMON}*, in most cases, the recommended voltage across R_{SNS} should be 50 mV. In Type-C application, typical R_{IMON} resistors value are listed in 表 10-3 given the condition full load current = 3 A, R_{SNS} = 15 mΩ and R_{SET} = 300 Ω.

表 10-3. Setting the Cable Compensation Voltage with R_{IMON}

CABLE COMPENSATION VOLTAGE AT 3-A FULL LOAD (V)	R_{IMON} (kΩ)
0.3	4.02
0.6	8.06
0.9	12.1
1.2	16.2
1.5	20

Pls note that the max cable compensation voltage in TPS2583xA-Q1 is 1.5 V.

10.3.12.1 Cable Compensation Design Example

To start the procedure, the R_{SNS}, R_{DSON_NFET} and wire resistance R_{WIRE}, must be known.

1. Determine R_{SNS} to achieve 50 mV at full current. For 3.3 A (3-A Type-C load current plus approximately 10% for overcurrent threshold). R_{SNS} = (0.05 V / 3.3 A) = 15 mΩ.
2. R_{DSON_NFET} = 50 mΩ
3. R_{WIRE} = 200 mΩ
4. $\Delta V_{OUT} = (R_{SNS} + R_{DSON_NFET} + R_{WIRE}) \times I_{BUS}$ = (0.015 + 0.05 + 0.2) × 3 = 0.795 V
5. Choose R_{SET} = 300 Ω
6. $R_{IMON} = (\Delta V_{OUT} * R_{SET} \times 2) / (I_{BUS} \times R_{SNS})$ = (0.795 × 300 × 2) / (3 × 0.015) = 10.6 kΩ

10.3.13 USB Port Control

The TPS2583xA-Q1include DP_IN, DM_IN, CC1 and CC2 pins for automatic or host facilitated USB port power management of either a Type-A or Type-C downstream facing connector. See the *Device Functional Modes* section for details on configuring the TPS2583xA-Q1.

10.3.14 FAULT Response

The device features an active-low, open-drain fault output. Connect a 100-kΩ pullup resistor from $\overline{FAULT}$ to VCC or other suitable I/O voltage. $\overline{FAULT}$ can be left open or tied to GND when not used.

表 10-4 summarizes the conditions that generate a fault and actions taken by the device.

表 10-4. Fault and Warning Conditions

EVENT	CONDITION	ACTION
Overcurrent on OUT	NFET or Buck average current limit implemented per *Current Limit Setting using R_{ILIMIT}*. $I_{CSN/OUT}$ > programmed I_{SNS}.	The device regulates current at I_{SNS} either by external NFET or by the buck regulator control loop. When current limiting by external NFET, there is NO fault indicator assertion under minor overload conditions. When current limiting by buck average current, there is NO fault indicator assertion under minor overload conditions. Hard shorts during average buck current limiting may trigger buck hiccup operation. The $\overline{FAULT}$ indicator asserts immediately after N_{OC} cycles in and persists for T_{OC} as specified in the *Cycle-by-Cycle Buck Current Limit* section.
Overvoltage on BUS	V_{BUS} > V_{BUS_OV}	The device turns on the BUS discharge path in the event of an overvoltage conditions, and turn off the LS_GD immediately. The $\overline{FAULT}$ indicator asserts and de-asserts with a 8-ms deglitch.
Overvoltage on the data lines	DP_IN or DM_IN > $V_{Dx_IN_OV}$	The device immediately shuts off the USB data switches. The $\overline{FAULT}$ indicator asserts and de-asserts with a 8-ms deglitch.
Overvoltage on CC lines	CC1 or CC2 > V_{CCx_OV}	The device immediately shuts off the CC lines. The $\overline{FAULT}$ indicator asserts and de-asserts with a 8-ms deglitch.

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表 10-4. Fault and Warning Conditions (continued)

EVENT	CONDITION	ACTION
Overcurrent on CC lines when supplying VCONN	$I_{LOAD_CCn} > I_{OS_CCn}$	The $\overline{FAULT}$ indicator asserts and de-asserts with a 8-ms deglitch. The $\overline{FAULT}$ indicator remains asserted during the VCONN overload condition and the VCONN path is not disabled.

10.3.15 USB Specification Overview

Universal Serial Bus specifications provide critical physical and electrical requirements to electronics manufacturers of USB capable equipment. Adherence to these specifications during product development coupled with standardized compliance testing assures very high degrees of interoperability amongst USB products in the market. Since its inception in the mid 1990s, USB has undergone a number of revisions to enhance utility and extend functionality. For the most up to date standards, please consult the USB Implementers Forum (USB-IF).

All USB ports are capable of providing a 5-V output making them a convenient power source for operating and charging portable devices. USB specification documents outline specific power requirements to ensure interoperability. In general, a USB 2.0 port host port is required to provide up to 500 mA; a USB 3.0 or USB 3.1 port is required to provide up to 900 mA; ports adhering to the USB Battery Charging 1.2 Specification provide up to 1500 mA; and newer Type-C ports can provide up to 3000 mA. Though USB standards governing power requirements exist, some manufacturers of popular portable devices created their own proprietary mechanisms to extend allowed available current beyond the 1500-mA maximum per BC 1.2. While not officially part of the standards maintained by the USB-IF, these proprietary mechanisms are recognized and implemented by manufacturers of USB charging ports.

The TPS2583xA-Q1 device supports five of the most-common USB-charging schemes found in popular hand-held media and cellular devices.

- USB Type-C (1.5-A and 3-A advertisement)
- USB Battery Charging Specification BC1.2
- Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider 3 mode
- 1.2-V mode

The BC1.2 specification includes three different port types:

- Standard Downstream Port (SDP)
- Charging Downstream Port (CDP)
- Dedicated Charging Port (DCP)

BC1.2 defines a charging port as a downstream-facing USB port that provides power for charging portable equipment. Under this definition, CDP and DCP are defined as charging ports.

表 10-5 lists the difference between these port types.

表 10-5. USB Operating Modes Table

PORT TYPE	SUPPORTS USB2.0 COMMUNICATION	MAXIMUM ALLOWABLE CURRENT DRAWN BY PORTABLE EQUIPMENT (A)
SDP (USB 2.0)	YES	0.5
SDP (USB 3.0 and 3.1)	YES	0.9
CDP	YES	1.5
DCP	NO	1.5
TYPE-C	YES	3.0

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10.3.16 USB Type-C® Basics

For a detailed description of the Type-C specifications refer to the USB-IF website to download the latest information. Understanding the basic concepts of the USB Type-C specification will aid in understanding the operation of the TPS2583xA-Q1 (a DFP device).

USB Type-C removes the need for different plug and receptacle types for host and device functionality. The Type-C receptacle replaces both Type-A and Type-B receptacle since the Type-C cable is plug-able in either direction between host and device. A host-to-device logical relationship is maintained via the configuration channel (CC). Optionally hosts and devices can be either providers or consumers of power when USB Power Delivery (PD) communication is used to swap roles.

All USB Type-C ports operate in one of below three data modes:

- Host mode: the port can only be host (provider of power)
- Device mode: the port can only be device (consumer of power)
- Dual-Role mode: the port can be either host or device

Port types:

- DFP (Downstream Facing Port): Host
- UFP (Upstream Facing Port): Device
- DRP (Dual-Role Port): Host or Device

Valid DFP-to-UFP connections:

- 表 10-6 describes valid DFP-to-UFP connections
- Host to Host or Device to Device have no functions

表 10-6. DFP-to-UFP Connections

	HOST-MODE PORT	DEVICE-MODE PORT	DUAL-ROLE PORT
Host-Mode Port	No Function	Works	Works
Device-Mode Port	Works	No Function	Works
Dual-Role Port	Works	Works	Works(1)

(1) This may be automatic or manually driven.

10.3.16.1 Configuration Channel

The function of the configuration channel is to detect connections and configure the interface across the USB Type-C cables and connectors.

Functionally the Configuration Channel (CC) is used to serve the following purposes:

- Detect connect to the USB ports
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish DFP and UFP roles between two connected ports
- Discover and configure power: USB Type-C current modes or USB Power Delivery
- Discovery and configure optional Alternate and Accessory modes
- Enhances flexibility and ease of use

Typical flow of DFP to UFP configuration is shown in 图 10-26:

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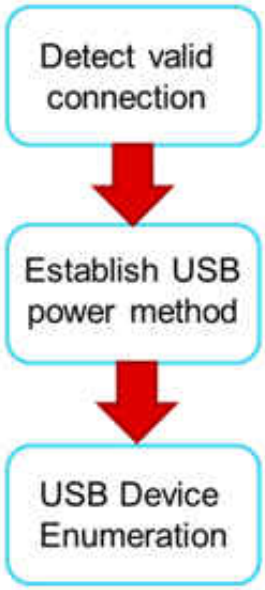

图 10-26. Flow of DFP to UFP Configuration

10.3.16.2 Detecting a Connection

DFPs and DRPs fulfill the role of detecting a valid connection over USB Type-C. 图 10-27 shows a DFP to UFP connection made with Type C cable. As shown in 图 10-27, the detection concept is based on being able to detect terminations in the product which has been attached. A pull-up and pull-down termination model is used. A pull-up termination can be replaced by a current source. TPS2583xA-Q1 devices use current sources in lieu of R_P as allowed by the Type-C specification.

- In the DFP-UFP connection the DFP monitors both CC pins for a voltage lower than the unterminated voltage.
- A UFP advertises Rd on both its CC pins (CC1 and CC2).
- A powered cable advertises Ra on only one of CC pins of the plug. Ra is used to inform the source to apply VCONN.
- An analog audio device advertises Ra on both CC pins of the plug, which identifies it as an analog audio device. VCONN is not applied on either CC pin in this case.

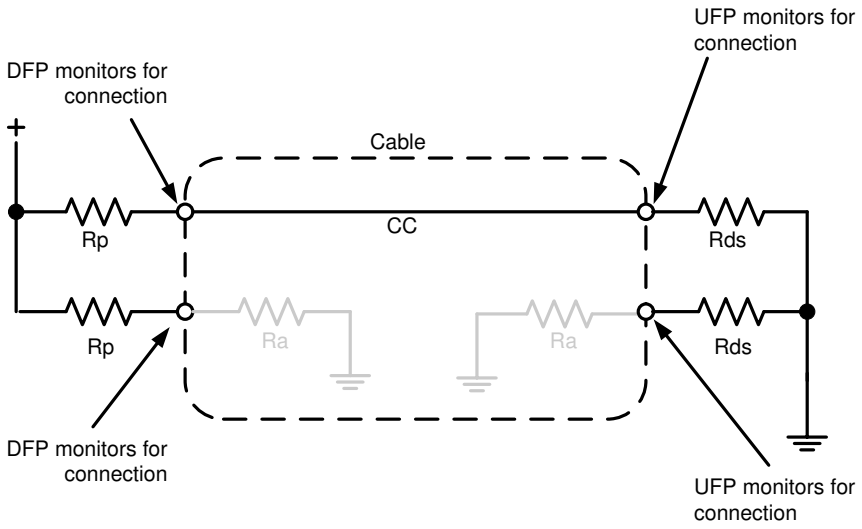

图 10-27. DFP-UFP Connection

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10.3.16.3 Configuration Channel Pins CC1 and CC2

The TPS2583xA-Q1 has two pins, CC1 and CC2 that serve to detect an attachment to the port and resolve cable orientation. These pins are also used to establish current broadcast to a valid UFP and configure VCONN.

表 10-7 lists TPS2583xA-Q1 response to various attachments to its port.

表 10-7. TPS2583xA-Q1 Response

TPS2583xA-Q1 TYPE C PORT	CC1	CC2	TPS2583xA-Q1 RESPONSE(1)				
			BUCK REGULATOR	LS_GD	V_{CONN} On CC1 or CC2(2)	$\overline{POL}$	$\overline{LD_DET}$
Nothing Attached	OPEN	OPEN	OFF	OFF	NO	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	ON	ON	NO	Hi-Z	LOW
UFP Connected	OPEN	Rd	ON	ON	NO	LOW	LOW
Powered Cable/No UFP Connected	OPEN	Ra	OFF	OFF	NO	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OFF	OFF	NO	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	ON	ON	CC2	Hi-Z	LOW
Powered Cable/UFP Connected	Ra	Rd	ON	ON	CC1	LOW	LOW
Debug Accessory Connected(3)	Rd	Rd	OFF	OFF	NO	Hi-Z	Hi-Z
Audio Adapter Accessory Connected(3)	Ra	Ra	OFF	OFF	NO	Hi-Z	Hi-Z

(1) $\overline{POL}$ and $\overline{LD_DET}$ are open drain outputs; pull high with 100 kΩ to VCC when used. Tie to GND or leave open when not used.
(2) To supply V_{CONN} a 5 V external LDO with at least 500-mA output current should be connected to the V_{CC} pin.
(3) The TPS2583xA-Q1 don't support debug mode or audio mode.

10.3.16.4 Current Capability Advertisement and VCONN Overload Protection

The TPS2583xA-Q1 supports all three Type-C current advertisements as defined by the USB Type C standard. Current broadcast to a connected UFP is controlled by the CTRL1 and CTRL2 pins. For each broadcast level the device protects itself from a UFP that draws current in excess of the port’s USB Type-C Current advertisement by setting the current limit as shown in 表 10-8.

表 10-8. USB Type-C® Current Advertisement

DEVICE	CTRL1	CTRL2	CC CAPABILITY BROADCAST	MODE	SUPPORT USB 2.0 COMMUNICATION	CURRENT LIMIT (typ)
'83xA-Q1	0	0	1.5 A	Client mode	YES: DP_IN to DP_OUT and DM_IN to DM_OUT	VBUS power is off
	0	1	1.5 A			
	1	0	1.5 A	SDP	YES: DP_IN to DP_OUT and DM_IN to DM_OUT	BY R_{SNS}, R_{SET}, R_{ILIMIT}
	1	1	3 A	CDP	YES: DP_IN to DP_OUT and DM_IN to DM_OUT	

Under overload conditions, a precision current-limit circuit limits the VCONN output current. When a VCONN overload condition is present, the TPS2583xA-Q1 maintains a constant output current, with the output voltage determined by (i_{OS_CCn} x R_{LOAD}). VCONN functionality is supported only with an external 5-V supply connected to VCC. Failure to connect an external supply may cause TPS2583xA-Q1 Vcc reset. The device turns off when the junction temperature exceeds the thermal shutdown threshold, T_{SD}, and remains off until the junction temperature cools approximately 20°C and then restarts. The TPS2583xA-Q1 current limit profile is shown in 图 10-28.

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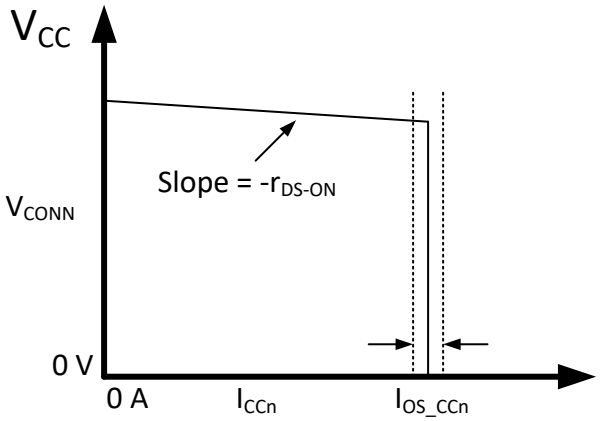

图 10-28. VCONN Current Limit Profile

10.3.16.5 Plug Polarity Detection

Reversible Type-C plug orientation is reported by the $\overline{POL}$ pin when a UFP is connected. However when no UFP is attached, $\overline{POL}$ remains de-asserted irrespective of cable plug orientation. 表 10-9 describes the $\overline{POL}$ state based on which device CC pin detects V_{RD} from an attached UFP pull-down.

表 10-9. Plug Polarity Detection

CC1	CC2	$\overline{POL}$	STATE
Rd	Open	Hi-Z	UFP connected
Open	Rd	Asserted (pulled low)	UFP connected with reverse plug orientation

图 10-29 shows an example implementation that uses the $\overline{POL}$ terminal to control the SEL terminal on the HD3SS3212. The HD3SS3212 provides switching on the differential channels between Port B and Port C to Port A depending on cable orientation.

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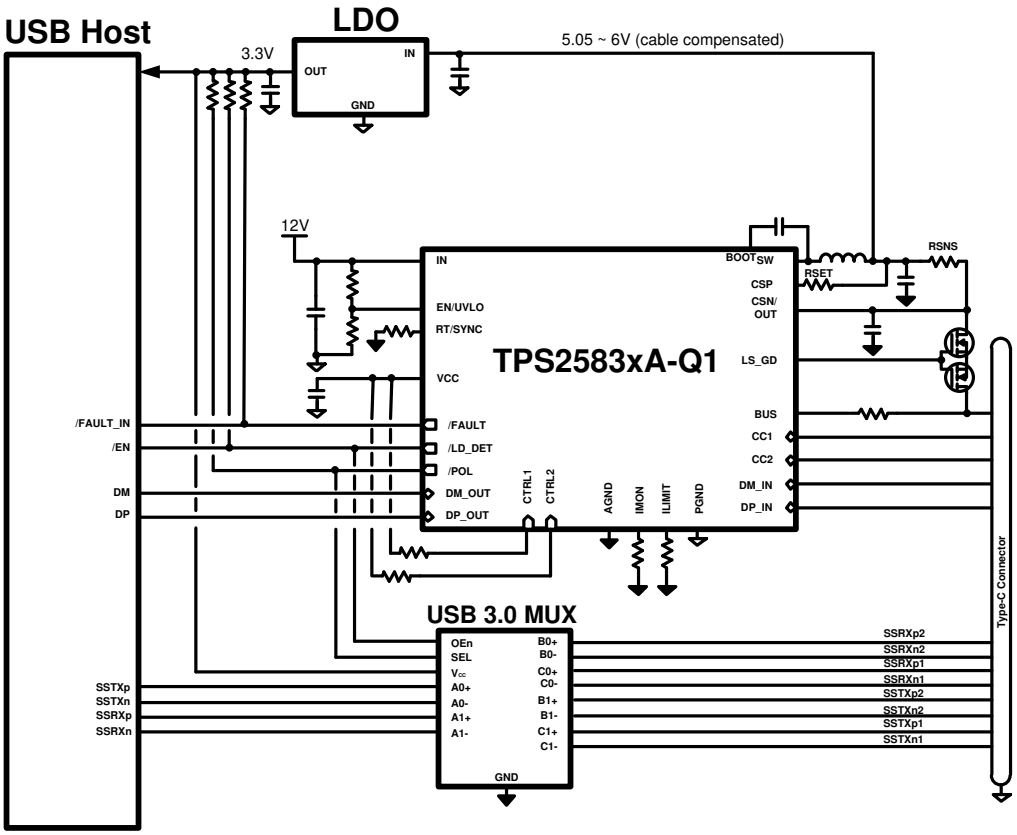

图 10-29. Example Implementation

10.3.17 Device Power Pins (IN, CSN/OUT, and PGND)

The IN pins are the input power path to the TPS2583xA-Q1 devices. The internal LDO and buck regulator high side switch are supplied from the IN pins. The CSN/OUT pin connects to the negative terminal of the current sense amplifier and the internal voltage feedback network. This pin must be connected to the output LC filter for proper operation. PGND is the power ground return. For optimum performance, ensure the IN pin is properly bypassed to PGND with adequate bulk and high-frequency bypass capacitance located as close to these pins as possible.

10.3.18 Thermal Shutdown

The device has an internal overtemperature shutdown threshold, T_{SD}, to protect the device from damage and overall safety of the system. When device temperature exceeds T_{SD}, the LD_GD pin is pulled low, and the buck regulator stops switching. The device attempts to power-up when die temperature decreases by approximately 20°C.

10.3.19 Power Wake

Legacy Type-A ports source 5 V on VBUS regardless of a load connection or not. In contrast, Type-C ports are "cold," 0 V, until a UFP connection has been detected with the CC lines. This fundamental change in VBUS operation enables a Type-C port to save power when no load is connected. The TPS2583xA-Q1 devices monitor the CC lines for a UFP connection and enable the internal buck regulator to source VBUS after a UFP is detected. As a result idle port power consumption is reduced compared to Type-A port systems where the buck regulator operates continuously to supply VBUS, even when no load is connected.

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10.4 Device Functional Modes

10.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control for the TPS2583xA. When V_{EN} is below 1.2 V (typical), the device is in shutdown mode. The TPS2583xA-Q1 also employs V_{IN} and V_{CC} undervoltage lock out protection. If V_{IN} or V_{CC} voltage is below their respective UVLO level, the regulator will be turned off.

10.4.2 Standby Mode

If the EN pin is pulled above the EN threshold, and there is no active connection on the CC lines, TPS2583xA-Q1 remains in a low-power state with the buck converter off until a valid UFP (sink) is detected with a valid R_D on either CC1 or CC2. This mode ensures the Type-C 0-V V_{BUS} requirement is met and saves system power when no device is connected.

10.4.3 Active Mode

The TPS2583xA-Q1 is in Active Mode when V_{EN} is above the precision enable threshold, V_{IN} and V_{CC} are above their respective UVLO levels ***and*** a valid detection has been made on the CC lines. The simplest way to enable the TPS2583xA-Q1 is to connect the EN pin to VIN pin. This allows self startup when the input voltage is in the operating range: 3.8 V to 36 V and a UFP detection is made. Refer to *VCC, VCC_UVLO* and *Enable/UVLO and Start-up* for details on setting these operating levels.

In Active Mode, the TPS2583xA-Q1 buck regulator operates with forced pulse width modulation (FPWM), also referred to as forced continuous conduction mode (FCCM). This ensures the buck regulator switching frequency remains constant under all load conditions. FPWM operation provides low output voltage ripple, tight output voltage regulation, and constant switching frequency. Built-in spread-spectrum modulation aids in distributing spectral energy across a narrow band around the switching frequency programmed by the RT/SYNC pin. Under light load conditions the inductor current is allowed to go negative. A negative current limit of I_{L_NEG} is imposed to prevent damage to the regulator's low side FET. During operation the TPS2583xA-Q1 will synchronize to any valid clock signal on the RT/SYNC input.

10.4.4 Device Truth Table (TT)

The device truth table (表 10-10) lists all valid combinations for the two control pins (CTRL1 and CTRL2). The TPS2583xA-Q1 devices monitor the CTRL inputs and transitions to whichever charging mode is commanded.

The data line switches are NOT OFF during mode changes once Rd asserts. VBUS voltage is depending on new mode the device transitions to. If the device change from CDP mode to Client mode, the VBUS will be turned OFF; If the device change from CDP mode to SDP mode, the VBUS will be always on during mode transition.

表 10-10. Truth Table

DEVICE	CTRL1	CTRL2	CURRENT LIMIT SETTING	USB MODES	BUCK REGULATOR	LS_GD
TPS25830xA-Q1	0	0	VBUS is off	Client mode	OFF	OFF
	0	1				
	1	0	See *Current Limit Setting using R_{ILIMIT}*	Type-C (1.5A) + SDP Mode	ON	ON
	1	1		Type-C (3A) + CDP Mode	ON	ON

10.4.5 USB Port Operating Modes

10.4.5.1 USB Type-C Mode

The TPS2583xA-Q1 is a Type-C controller that supports all Type-C functions in a downstream facing port. It is also used to manage current advertisement and protection to a connected UFP and active cable. When VIN exceeds the undervoltage lockout threshold, the device samples the EN pin. A high level on this pin enables the device and normal operation begins. Having successfully completed its start-up sequence, the device now actively monitors its CC1 and CC2 pins for attachment to a UFP. When a UFP is detected on either the CC1 or CC2 pin the buck regulator turn-ons after the required de-bounce time is met. If connected, the LS_GD pin sources current into the external MOSFET allowing current to flow from CSN/OUT to BUS. If Ra is detected on

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the other CC pin (not connected to UFP), VCONN is applied to allow current to flow from VCC to the CC pin connected to Ra. For a complete listing of various device operational modes refer to 表 10-7.

The TPS2583xA-Q1 always starts in Type-C mode, then transitions to Client, CDP, or SDP as determined by the CTRL1 and CTRL2 pins and signaling by the connected portable device on the DP_IN and DM_IN pins.

10.4.5.2 Standard Downstream Port (SDP) Mode — USB 2.0, USB 3.0, and USB 3.1

A SDP is a traditional USB port that follows USB 2.0, USB 3.0 or USB 3.1 protocol. A USB 2.0 SDP supplies a minimum of 500 mA per port and supports USB 2.0 communications. A USB 3.x SDP supplies a minimum of 900 mA per port and supports USB 3.0 or USB 3.1 communications. For both types, the host controller must be active to allow charging.

10.4.5.3 Charging Downstream Port (CDP) Mode

A CDP is a USB port that follows USB BC1.2 and supplies a minimum of 1.5 A per port. A CDP provides power and meets the USB 2.0 requirements for device enumeration. USB-2.0 communication is supported, and the host controller must be active to allow charging. The difference between CDP and SDP is the host-charge handshaking logic that identifies this port as a CDP. A CDP is identifiable by a compliant BC1.2 client device and allows for additional current draw by the client device.

The CDP handshaking process occurs in two steps. During step one, the portable equipment outputs a nominal 0.6-V output on the DP line and reads the voltage input on the DM line. The portable device detects the connection to an SDP if the voltage is less than the nominal data-detect voltage of 0.3 V. The portable device detects the connection to a CDP if the DM voltage is greater than the nominal data detect voltage of 0.3 V and optionally less than 0.8 V.

The second step is necessary for portable equipment to determine whether the equipment is connected to a CDP or a DCP. The portable device outputs a nominal 0.6-V output on the DM line and reads the voltage input on the DP line. The portable device concludes the equipment is connected to a CDP if the data line being read remains less than the nominal data detects voltage of 0.3 V. The portable device concludes it is connected to a DCP if the data line being read is greater than the nominal data detect voltage of 0.3 V.

10.4.5.4 Client Mode

The TPS2583xA-Q1 device integrates client mode as shown in 图 10-30. Both the buck converter and the external MOSFET power switch are OFF and only the data analog switch is ON. This mode can be used by automotive USB system manufacturers and OEMs for factory-only software programming via the USB port.

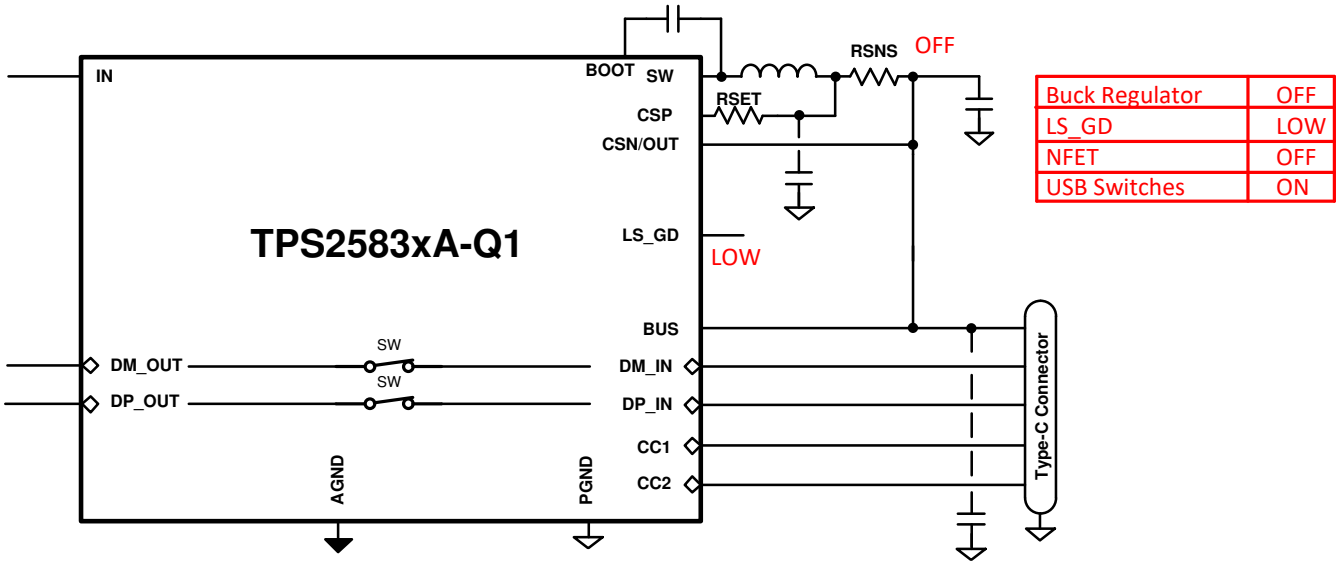

图 10-30. Client-Mode Equivalent Circuit

If the TPS2583xA-Q1 configured in Client mode during start up, the data line switches are always on regardless the voltage on VBUS and DP/DM pin.

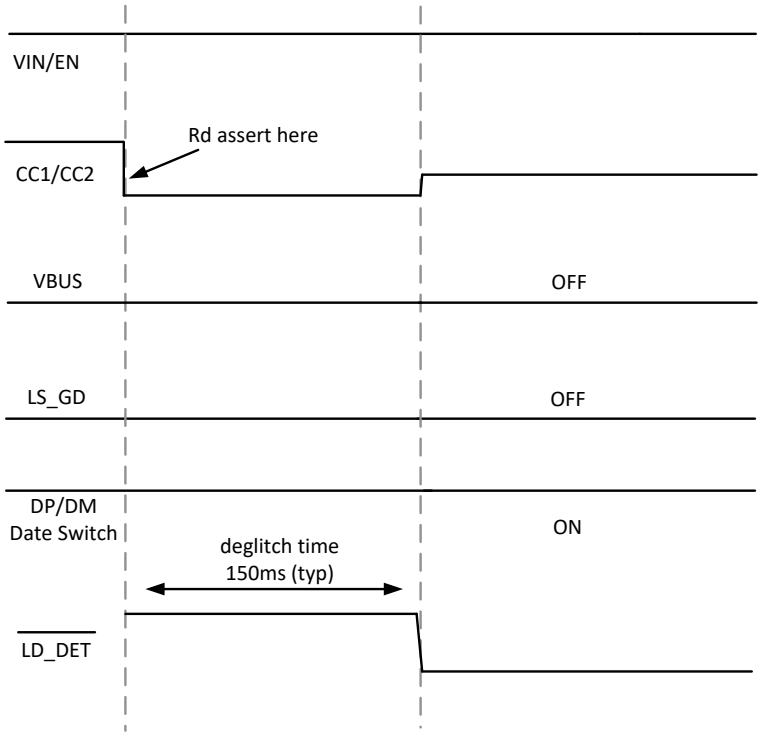

图 10-31. TPS2583xA-Q1 Startup Behavior Under Client Mode

10.4.6 High-Bandwidth Data-Line Switches

The TPS2583xA-Q1 device passes the DP and DM data lines through the device to enable monitoring and handshaking while supporting the charging operation. A wide-bandwidth signal switch allows data to pass through the device without corrupting signal integrity. The data-line switches are turned on in any of the CDP, SDP or client modes. Under client mode, once the EN/UVLO input is at logic high, the data line switches are turn on. Under CDP/SDP mode, the data line switches are only turn on after Rd assert.

For more detailed USB2.0 data line consideration and eye diagram test report, please refer to How to improve USB2.0 Eye Diagram using long USB cable.

Note

- While in CDP mode, the data switches are ON, even during CDP handshaking.
- The data line switches are OFF if EN/UVLO is low.
- The data line switches are OFF if OVP is deteced on data line.
- The data switches are only for a USB-2.0 differential pair. In the case of a USB-3.0 or 3.1 host, the super-speed differential pairs must be routed directly to the USB connector without passing through the TPS2583xA-Q1 device.

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11 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

11.1 Application Information

The TPS2583xA-Q1 is a step down DC-to-DC regulator and USB charge port controller. It is typically used in automotive systems to convert a DC voltage from the vehicle battery to 5-V DC with a maximum output current of 3.5 A. The following design procedure can be used to select components for the TPS2583xA-Q1.

11.2 Typical Application

The TPS2583xA-Q1 only requires a few external components to convert from a wide voltage range supply to a 5-V output for powering USB devices. 图 11-1 shows a basic schematic.

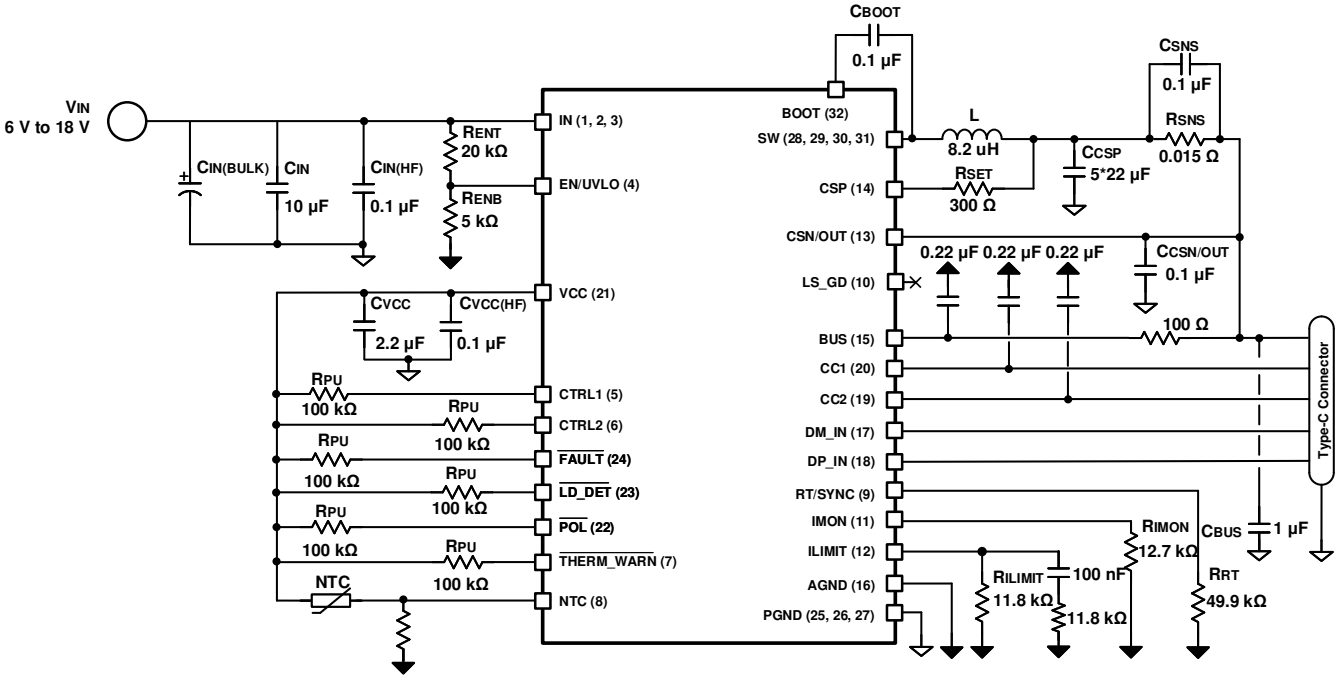

图 11-1. Application Circuit

The integrated buck regulator of TPS2583xA-Q1 is internally compensated and optimized for a reasonable selection of external inductance and capacitance. The external components have to fulfill the needs of the application, but also the stability criteria of the device's control loop. 表 11-2 can be used to simplify the output filter component selection.

11.2.1 Design Requirements

To begin the design process, a few parameters must be known:

- Cable compensation: total resistance including cable resistance, contact resistance of connectors, TPS2583xA-Q1 current sense resistor and external NFET $r_{DS(on)}$ (if used). Refer to 图 10-24 for examples of resistances in an automotive application.
- The maximum continuous output current for the charging port. The minimum current-limit setting of TPS2583xA-Q1 device must be higher than this current.

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For this example, use the parameters listed in 表 11-1 as the input parameters.

表 11-1. Design Example Parameters

PARAMETER	VALUE
Input Voltage, V_{IN}	13.5-V typical, range from 6 V to 18 V
Output Voltage, V_{OUT}	5.1 V
Maximum Output Current $I_{OUT(MAX)}$	3.0 A
Transient Response 0.3 A to 3 A	5%
Output Voltage Ripple	50 mV
Input Voltage Ripple	400 mV
Switching Frequency f_{SW}	400 kHz
Cable Resistance for Cable Compensation	300 mΩ
Current Limit by Buck Average	3.3 A

表 11-2. L and C_{OUT} Typical Values

f_{SW}	V_{OUT} WITHOUT CABLE COMPENSATION	C_{IN} + C_{HF}	L	CURRENT LIMIT	C_{CSP}	$C_{CSN/OUT}$	C_{BUS}
400 kHz	5.10 V	1 × 10 µF + 1 × 100 nF	8.2 µH	Buck Avg	5 × 22 µF	100 nF	1 to 4.7 µF
400 kHz	5.10 V	1 × 10 µF + 1 × 100 nF	8.2 µH	Ext. NFET	5 × 22 µF	100 nF	1 to 4.7 µF
2100 kHz	5.10 V	1 × 10 µF + 1 × 100 nF	3.3 µH	Buck Avg	2 × 22 µF	100 nF	1 to 4.7 µF

1. Inductance value is calculated based on V_{IN} = 18 V.
2. All the C_{OUT} values are after de-rating.

11.2.2 Detailed Design Procedure

11.2.2.1 Output Voltage

The output voltage of TPS2583xA-Q1 is internally fixed at 5.10 V. Cable compensation can be used to increase the voltage on the CSN/OUT pin linearly with increasing load current. Refer to the *Cable Compensation* section for more details on output voltage variation versus load current. If cable compensation is not desired, use a 0-Ω R_{IMON} resistor.

11.2.2.2 Switching Frequency

The recommended switching frequency of the TPS2583xA-Q1 is in the range of 300 to 400 kHz for best efficiency. Choose R_{RT} = 49.9 kΩ for 400-kHz operation. To choose a different switching frequency, refer to 表 10-1.

11.2.2.3 Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current and the rated current. The inductance is based on the desired peak-to-peak ripple current Δi_L. Since the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use Equation 10 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device. A reasonable value of K_{IND} should be 20% to 40%. During an instantaneous short or overcurrent operation event, the RMS and peak inductor current can be high. The inductor current rating should be higher than the current limit of the device.

$$\Delta i_L = \frac{V_{OUT} \times \left(V_{IN_MAX} - V_{OUT}\right)}{V_{IN_MAX} \times L \times f_{SW}} \tag{9}$$

$$L_{MIN} = \frac{V_{IN_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN_MAX} \times f_{SW}} \tag{10}$$

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In general, it is preferable to choose lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. But too low of an inductance can generate too large of an inductor current ripple such that overcurrent protection at the full load could be falsely triggered. Larger inductor current ripple also implies larger output voltage ripple with same output capacitors. With peak current mode control, it is not recommended to have too small of an inductor current ripple. A larger peak current ripple improves the comparator signal to noise ratio.

For this design example, choose K_{IND} = 0.3, the minimum inductor value is calculated to be 8.7 µH. Choose the nearest standard 8.2- µ H ferrite inductor with a capability of 5-A RMS current and 8-A saturation current.

11.2.2.4 Output Capacitor Selection

The value of the output capacitor, and its ESR, determine the output voltage ripple and load transient performance. The output capacitor bank is usually limited by the load transient requirements, rather than the output voltage ripple. Equation 11 can be used to estimate a lower bound on the total output capacitance, and an upper bound on the ESR, required to meet a specified load transient.

$$C_{OUT} \geq \frac{\Delta I_{OUT}}{f_{SW} \cdot \Delta V_{OUT} \cdot K} \cdot \left[(1-D) \cdot (1+K) + \frac{K^2}{12} \cdot (2-D) \right]$$

$$ESR \leq \frac{(2+K) \cdot \Delta V_{OUT}}{2 \cdot \Delta I_{OUT} \left[1+K+\frac{K^2}{12} \cdot \left(1+\frac{1}{(1-D)} \right) \right]}$$

$$D = \frac{V_{OUT}}{V_{IN}} \tag{11}$$

where

- ΔV_{OUT} = output voltage transient
- ΔI_{OUT} = output current transient
- K = Ripple factor from *Inductor Selection*

Once the output capacitor and ESR have been calculated, Equation 12 can be used to check the peak-to-peak output voltage ripple; V_r.

$$V_r \cong \Delta I_L \cdot \sqrt{ESR^2 + \frac{1}{(8 \cdot f_{SW} \cdot C_{OUT})^2}} \tag{12}$$

The output capacitor and ESR can then be adjusted to meet both the load transient and output ripple requirements.

For this example we require a ΔV_{OUT} of $\leqslant$ 250 mV for an output current step of ΔI_{OUT} = 2.7 A. Equation 11 gives a minimum value of 86 µF and a maximum ESR of 0.08 Ω. Assuming a 20% tolerance and a 10% bias de-rating, we arrive at a minimum capacitance of 110 µF. This can be achieved with a bank of 5 × 22-µF, 10-V, ceramic capacitors in the 1210 case size. More output capacitance can be used to improve the load transient response. Ceramic capacitors can easily meet the minimum ESR requirements. In some cases an aluminum electrolytic capacitor can be placed in parallel with the ceramics to help build up the required value of capacitance.

In practice the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and Bode plots are the best way to validate any given design and should always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can help to reduce high frequency noise. Small case size ceramic capacitors in the range

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of 1 nF to 100 nF can be very helpful in reducing voltage spikes on the output caused by inductor and board parasitics.

The maximum value of total output capacitance should be limited to about 10 times the design value, or 1000 µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

11.2.2.5 Input Capacitor Selection

The TPS2583xA-Q1 device requires high frequency input decoupling capacitor(s) and a bulk input capacitor, depending on the application. A high-quality ceramic capacitor type X5R or X7R with sufficient voltage ratings are recommended. To compensate the derating of ceramic capacitors, a voltage rating of twice the maximum input voltage is recommended. The bulk capacitance selection depends upon a number of factors: long leads from the automotive battery to the IN pin of TPS2583xA-Q1, cold or warm engine crank requirements, etc. The bulk capacitor is used to dampen voltage spike due to the lead inductance of the cable or the trace. For this design, one 10 µF, 50 V, X7R ceramic capacitors are used. A 0.1 µF for high-frequency filtering and place it as close as possible to the device pins. Consider adding additional bulk capacitance for operation through low V_{IN} warm-crank profiles is required by the vehicle OEM.

11.2.2.6 Bootstrap Capacitor Selection

Every TPS2583xA-Q1 design requires a bootstrap capacitor (C_{BOOT}). The recommended capacitor is 0.1 µF and rated 10 V or higher. The bootstrap capacitor is located between the SW pin and the BOOT pin. The bootstrap capacitor must be a high-quality ceramic type with an X7R or X5R grade dielectric for temperature stability.

11.2.2.7 VCC Capacitor Selection

The VCC pin is the output of an internal LDO for TPS2583x. The LDO supplies gate charge to the LS buck switch and is the supply to the digital state-machine and analog USB circuitry. To insure stability of the device, place a minimum of 2.2 µF, 10 V, X7R capacitor from this pin to ground. In addition a 0.1-µF high frequency decoupling capacitor is highly recommended.

11.2.2.8 Enable and Undervoltage Lockout Set-Point

The system enable and undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The EN/UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. The following equations can be used to determine the $V_{IN(ON)}$ and $V_{IN(OFF)}$ levels.

$$R_{ENT} = \left(\frac{V_{IN(ON)}}{V_{EN/UVLO_H}} - 1\right) \times R_{ENB} \tag{13}$$

$$V_{IN(OFF)} = V_{IN(ON)} \times \left(1 - \frac{V_{EN/UVLO_HYS}}{V_{EN/UVLO_H}}\right) \tag{14}$$

$V_{IN(ON)}$ = 6 V (user choice)

R_{ENB} = 5 kΩ (user choice)

R_{ENT} = [($V_{IN(ON)}$ / $V_{EN/UVLO_H}$) - 1] × R_{ENB}

R_{ENT} = [(6 V / 1.2 V) - 1] × 5 kΩ = 20 kΩ. Choose standard 20 kΩ.

Therefore $V_{IN(OFF)}$ = 6 V × [1 - (0.09 V / 1.2 V)] = 5.55 V

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11.2.2.9 Current Limit Set-Point

The TPS2583xA-Q1 can provide an accurate current limit to protect the USB port from overload based upon the values of R_{SNS}, R_{SET} and R_{ILIMIT}. The design process is the same regardless of whether buck average current limiting or external NFET current limiting is chosen. The only difference is the current limit threshold voltage on the ILIMIT pin.

- R_{SNS} is the current sense resistor. The recommended voltage across the R_{SNS} undercurrent limit should be approximately 50 mV as a compromise between accuracy and power dissipation. For example, if current limiting is desired for $I_{OUT(MAX)} \geqslant$ 3.3 A, then R_{SNS} = 0.05 V / 3.3 A = 0.01515 Ω. Choose a standard value of 15 mΩ.
- R_{SET} determines the input current to the transconductance amplifier and current mirror. The amplifier balances the voltage to be equal to that across R_{SNS}. Choose a R_{SET} value to produce an I_{SET} current between 75 - 180 µA at the desired $I_{OUT(MAX)}$. Considering 50 mV across R_{SET}, a value of 300 Ω will provide approximately 166 µA of I_{SET} current to the amplifier and mirror circuit. Care should be taken to limit the I_{SET} current below 200 µA to avoid saturating the internal amplifier circuit.
- Buck average current limiting occurs when V_{ILIMIT} = 1 V. R_{ILIMIT} is calculated as 1 V × 300 Ω / [0.5 × (3.3 A × 15 mΩ + 0.7 mV)] = 11.95 kΩ. A standard 11.8-kΩ value is chosen.

11.2.2.10 Cable Compensation Set-Point

From 表 11-1 the total cable resistance to be accounted for is 300 mΩ.

1. From *Current Limit Set-Point* R_{SNS} and R_{SET} have been determined as 15 mΩ and 300 Ω, respectively.
2. R_{WIRE} = 300 mΩ
3. $\Delta V_{OUT} = (R_{SNS} + R_{WIRE}) \times I_{BUS} = (0.015 + 0.3) \times 3 = 1.0395$ V
4. $R_{IMON} = (\Delta V_{OUT} \times R_{SET} \times 2) / (I_{BUS} \times R_{SNS}) = (1.0395 \times 300 \times 2) / (3.3 \times 0.015) = 12.6$ kΩ. A standard value of 12.7 kΩ is selected.

11.2.2.11 $\overline{\text{LD_DET}}$, $\overline{\text{POL}}$, and $\overline{\text{FAULT}}$ Resistor Selection

The $\overline{\text{LD_DET}}$, $\overline{\text{POL}}$, and $\overline{\text{FAULT}}$ pins are open-drain output flags. They can be connected to the TPS2583xA-Q1 VCC pin with 100-kΩ resistors, or connected to another suitable I/O voltage supply if actively monitored by a USB HUB or MCU. They can be left floating if unused.

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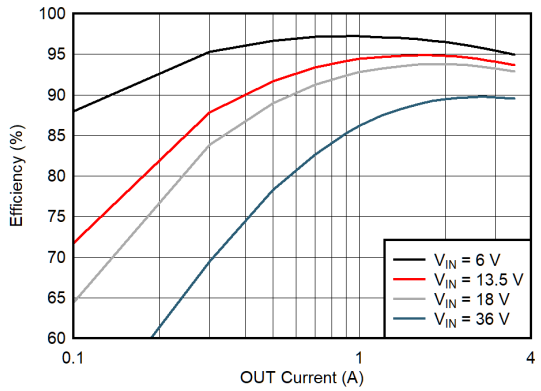
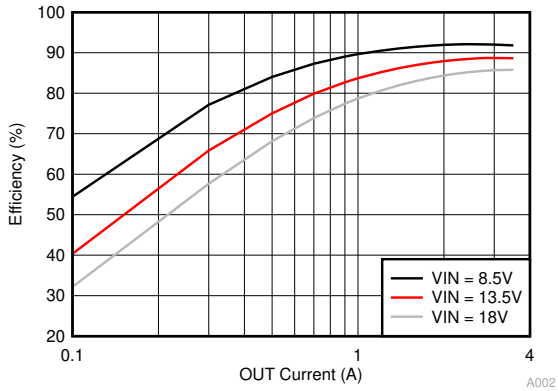
11.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 8.2 µH, C_{OUT_CSP} = 66 µF, C_{OUT_CSN} = 0.1 µF, C_{BUS} = 1 µF, T_A = 25 °C.



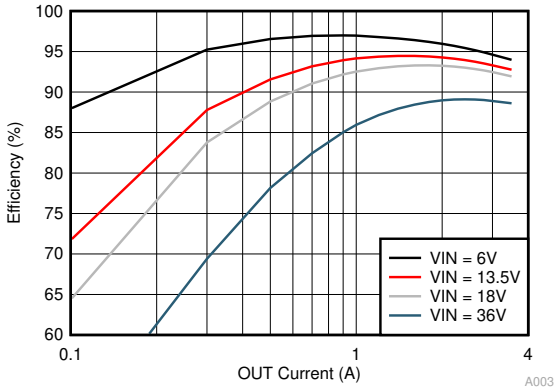
V_{OUT} = 5.1 V f_{SW} = 400 kHz

图 11-2. Buck Only Efficiency



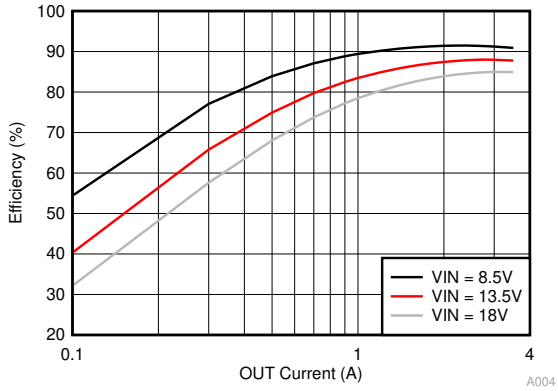
V_{OUT} = 5.1 V f_{SW} = 2100 kHz L = 3.3 uH

图 11-3. Buck Only Efficiency



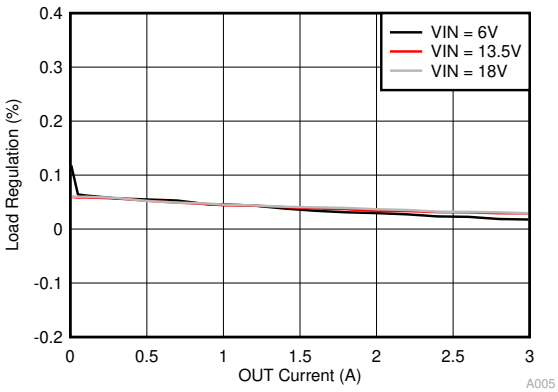
R_{SENS} = 15 mΩ f_{SW} = 400 kHz

图 11-4. Efficiency With Sense Resistor



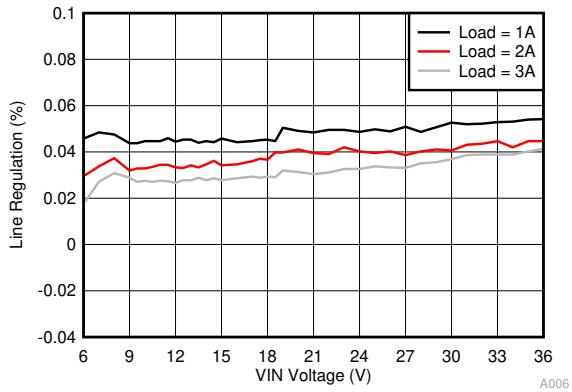
R_{SENS} = 15 mΩ f_{SW} = 2100 kHz L = 3.3uH

图 11-5. Efficiency With Sense Resistor



V_{OUT} = 5.1 V f_{SW} = 400 kHz

图 11-6. Load Regulation



V_{OUT} = 5.1 V f_{SW} = 400 kHz

图 11-7. Line Regulation

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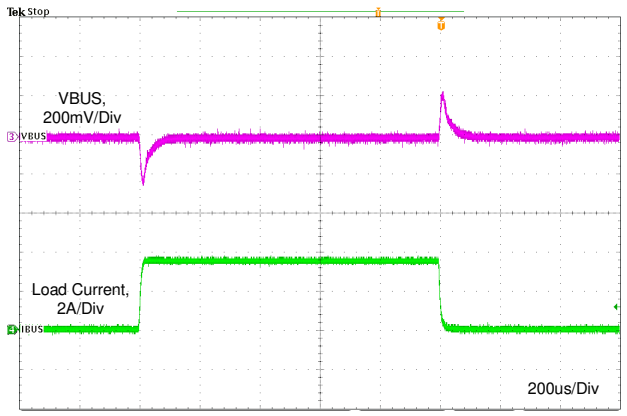
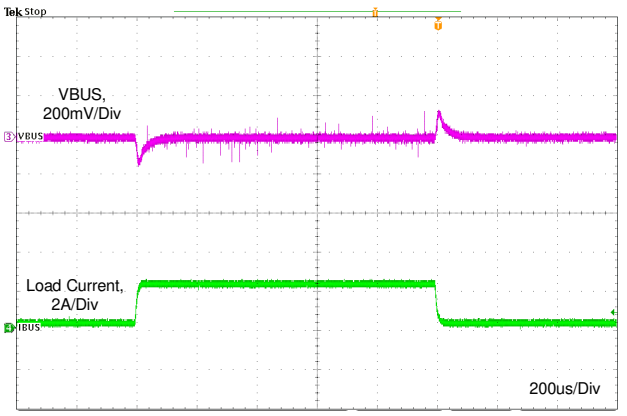


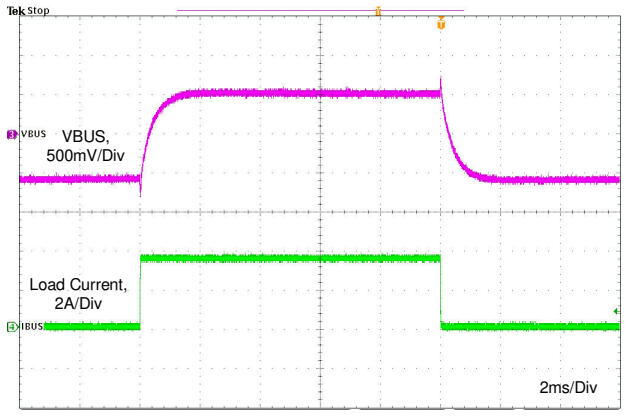
I_{LOAD} = 0 A to 3.5 A R_{IMON} = 0 Ω

图 11-8. Load Transient Without Cable Compensation



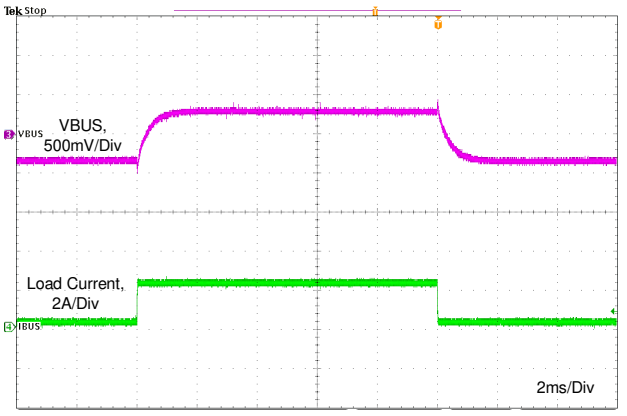
I_{LOAD} = 0.75 A to 2.25 A R_{IMON} = 0 Ω

图 11-9. Load Transient Without Cable Compensation



I_{LOAD} = 0 A to 3.5 A R_{IMON} = 13 kΩ

图 11-10. Load Transient with Cable Compensation



I_{LOAD} = 0.75 A to 2.25 A R_{IMON} = 13 kΩ

图 11-11. Load Transient with Cable Compensation

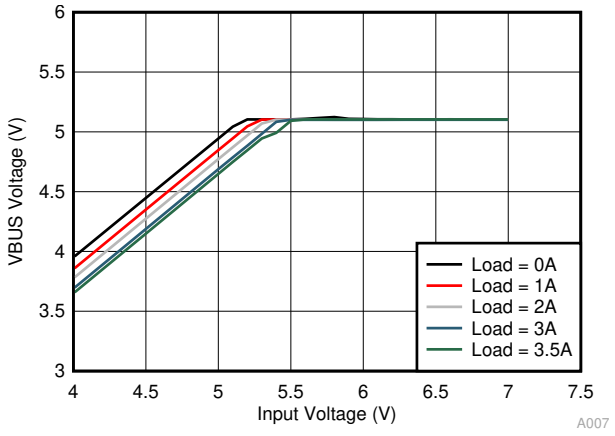
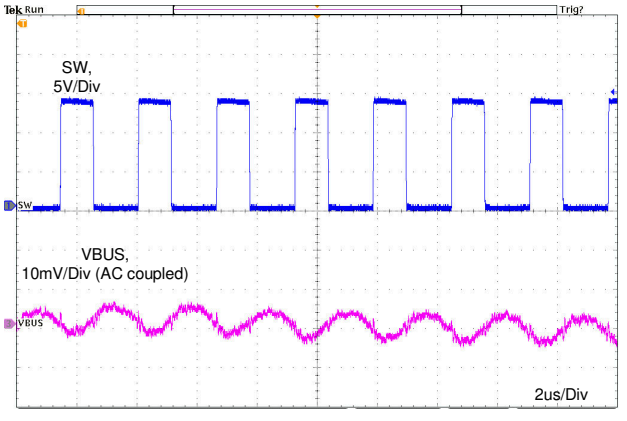
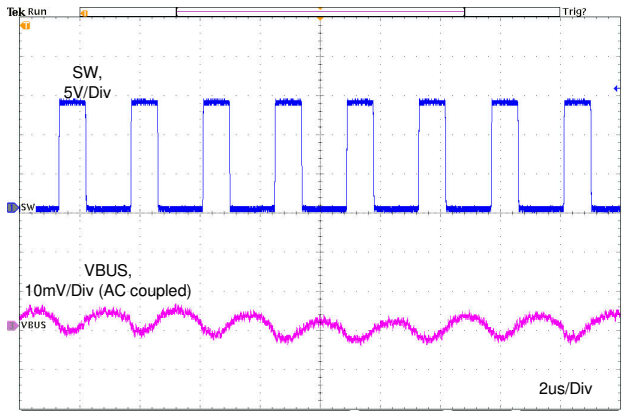


图 11-12. Dropout Characteristic



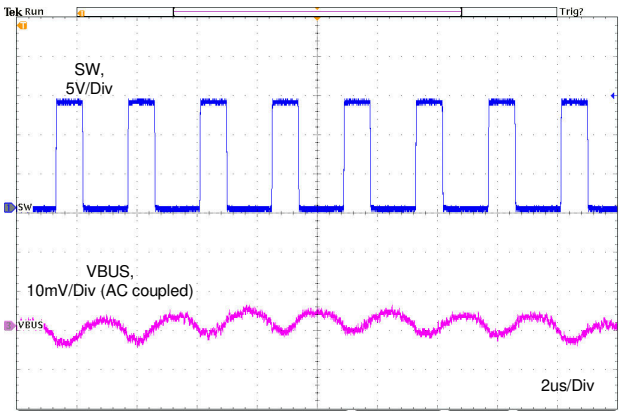
R_{IMON} = 13 kΩ

图 11-13. 3.5-A Output Ripple



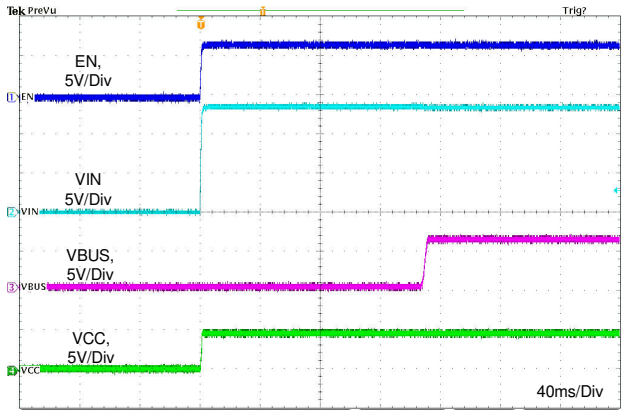
R_{IMON} = 13 kΩ

图 11-14. 100-mA Output Ripple



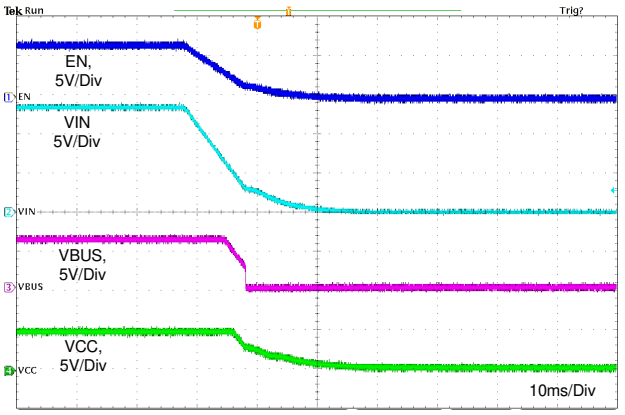
R_{IMON} = 13 kΩ

图 11-15. No Load Output Ripple



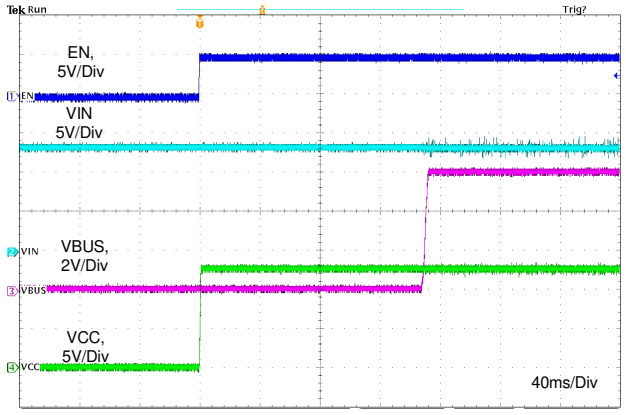
VIN = 0 V to 13.5 V CC1 = R_d I_{LOAD} = 3 A

图 11-16. Startup Relate to VIN



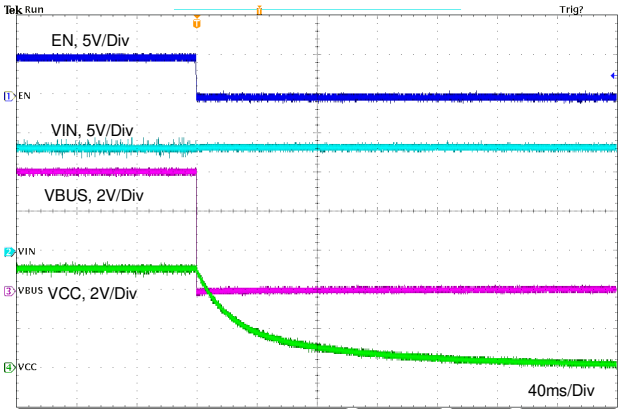
VIN = 13.5 V to 0 V CC1 = R_d I_{LOAD} = 3 A

图 11-17. Shutdown Relate to VIN



EN = 0 V to 5 V CC1 = R_d I_{LOAD} = 3 A

图 11-18. Startup Relate to EN



EN = 5 V to 0 V CC1 = R_d I_{LOAD} = 3 A

图 11-19. Shutdown Relate to EN

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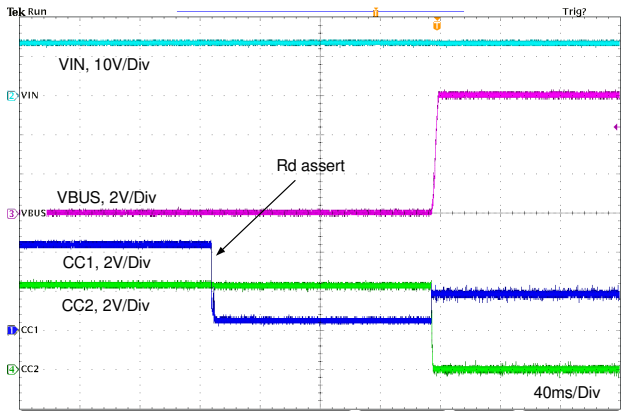
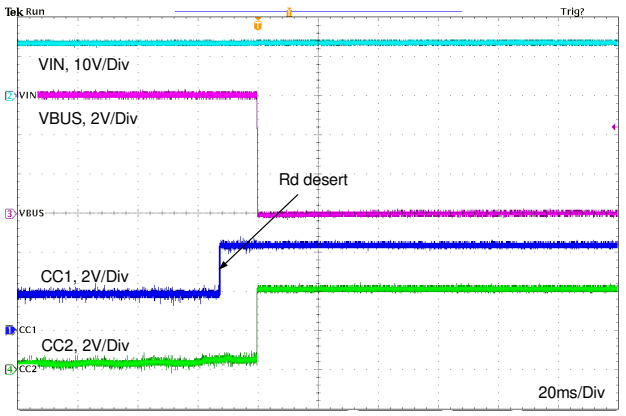


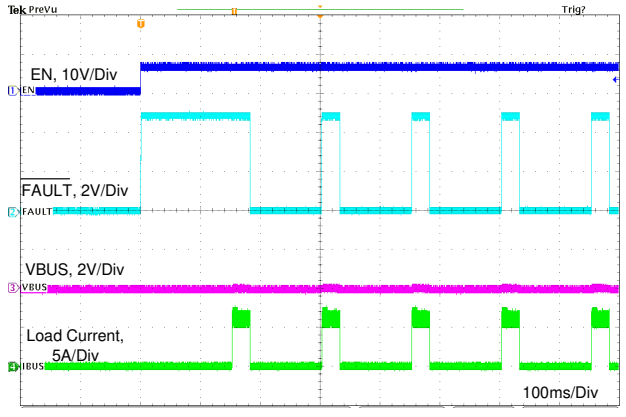
CC1 = Open to R_d CC2 = Open I_{LOAD} = 3 A

图 11-20. Rd Assert



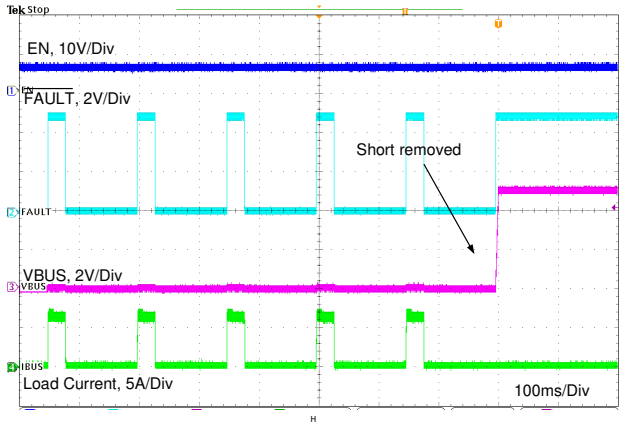
CC1 = R_d to Open CC2 = Open I_{LOAD} = 3 A

图 11-21. Rd Desert



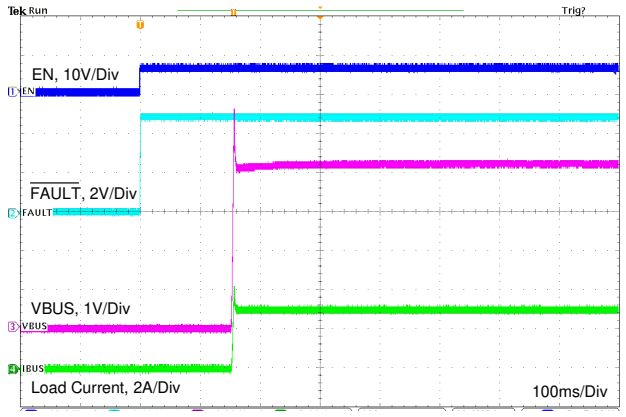
EN to High VBUS = GND R_{LIMIT} = 13 kΩ

图 11-22. Enable Into Short Without External FET



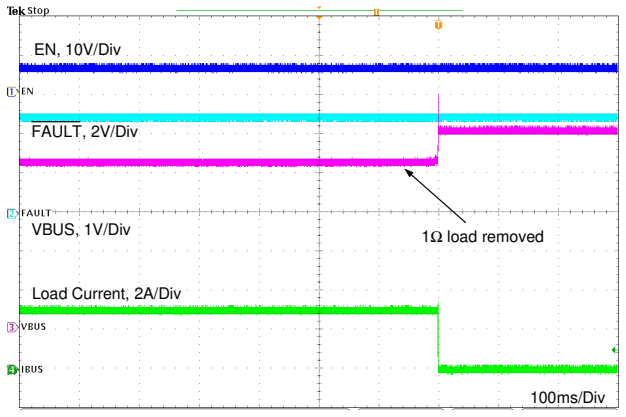
R_{LIMIT} = 13 kΩ

图 11-23. Short Circuit Recovery Without External FET



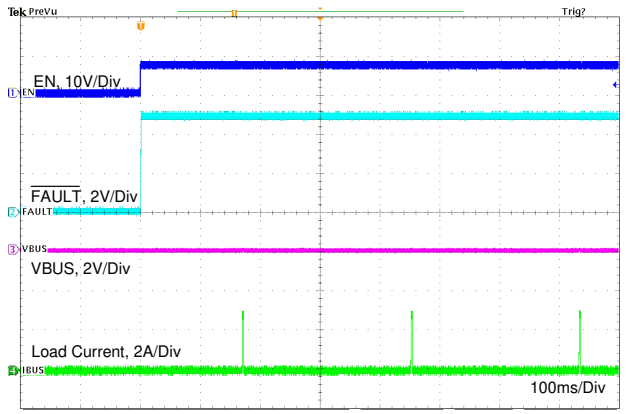
EN to High VBUS = GND R_{LIMIT} = 13 kΩ

图 11-24. Enable Into 1-Ω Load Without External FET



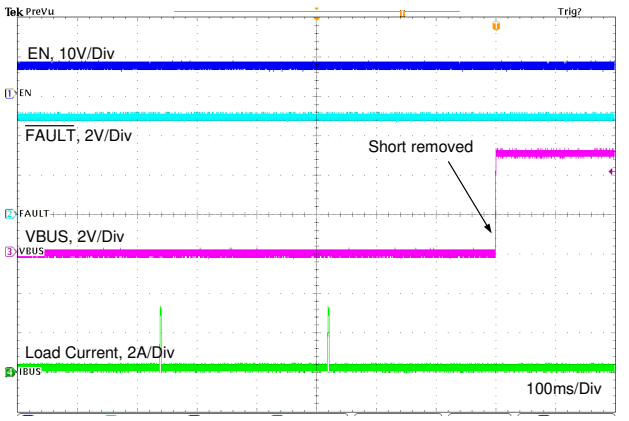
R_{LIMIT} = 13 kΩ

图 11-25. 1-Ω Load Recovery Without External FET



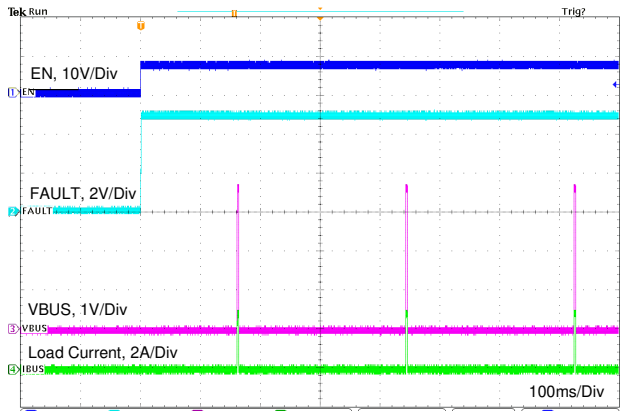
EN to High VBUS = GND R_{LIMIT} = 6.8 kΩ

图 11-26. Enable Into Short With External FET



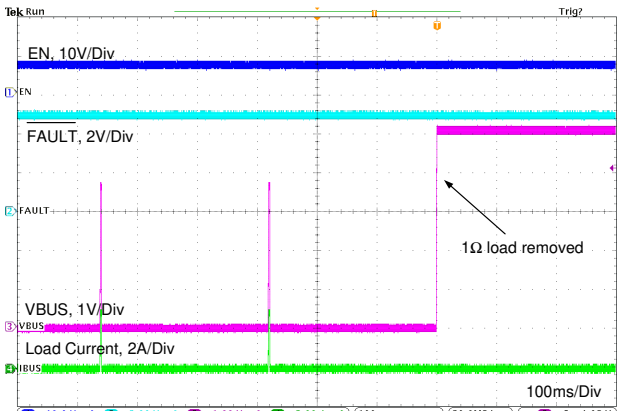
R_{LIMIT} = 6.8 kΩ

图 11-27. Short Circuit Recovery With External FET



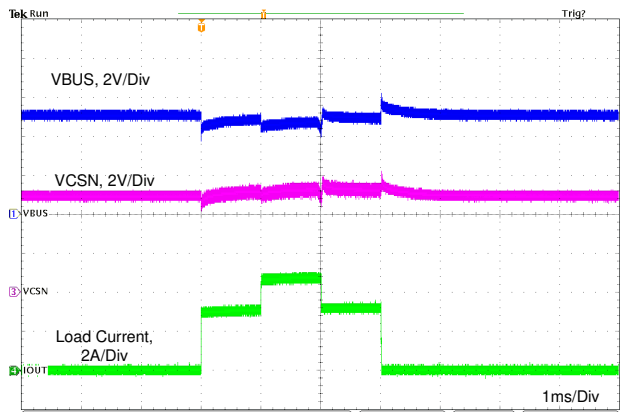
EN to High VBUS = GND R_{LIMIT} = 6.8 kΩ

图 11-28. Enable Into 1-Ω Load With External FET



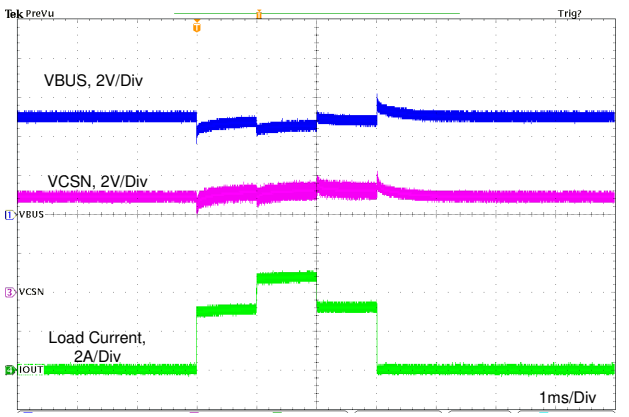
R_{LIMIT} = 6.8 kΩ

图 11-29. 1-Ω Load Recovery With External FET



I_{LOAD1} = 3 A I_{LOAD2} = 4.8 A R_{LIMIT} = 13 kΩ

图 11-30. MFI Over-Current Test Without External FET



I_{LOAD1} = 3 A I_{LOAD2} = 4.8 A R_{LIMIT} = 6.8 kΩ

图 11-31. MFI Over-Current Test With External FET

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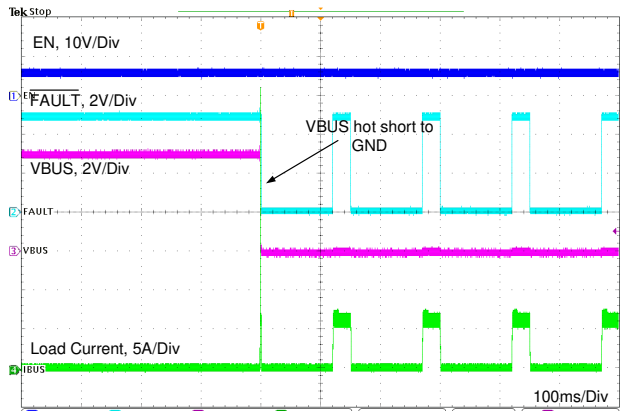
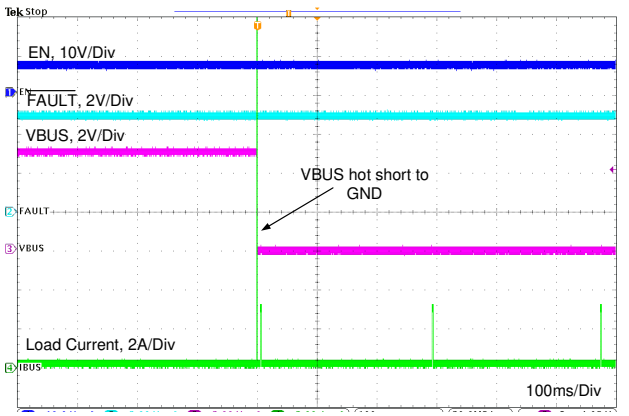


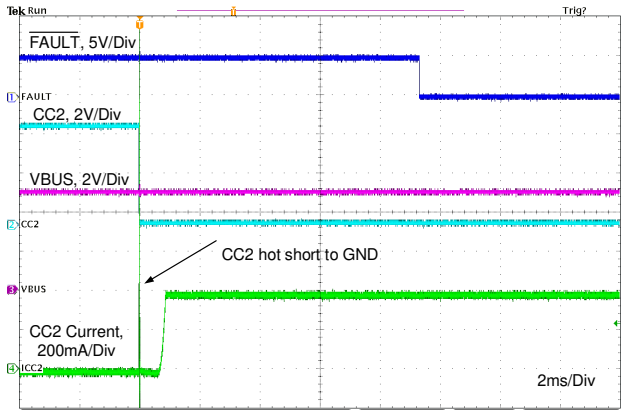
R_{LIMIT} = 13 kΩ

图 11-32. VBUS Hot Short to GND Without External FET



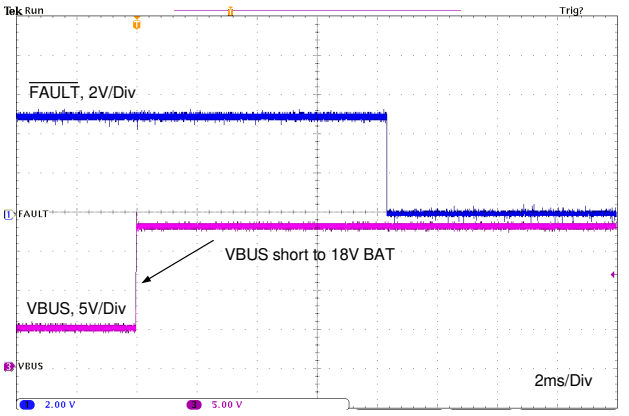
R_{LIMIT} = 6.8 kΩ

图 11-33. VBUS Hot Short to GND with External FET



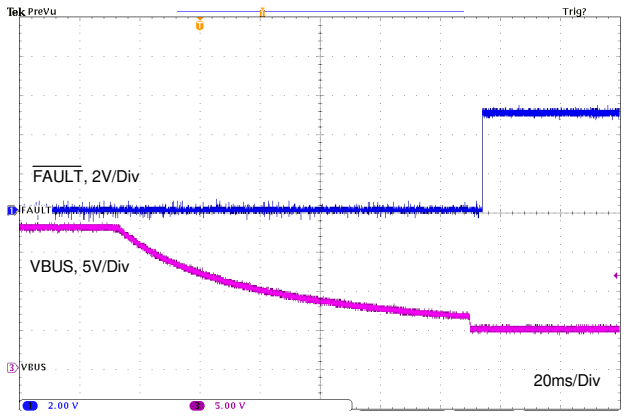
CC1 = R_d CC2 = R_a

图 11-34. CC2 Hot Short to GND



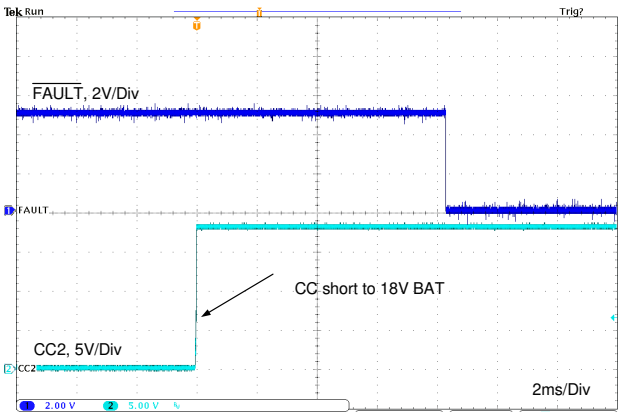
CC1 = R_d CC2 = OPEN NO LOAD

图 11-35. VBUS Short to BAT with External FET



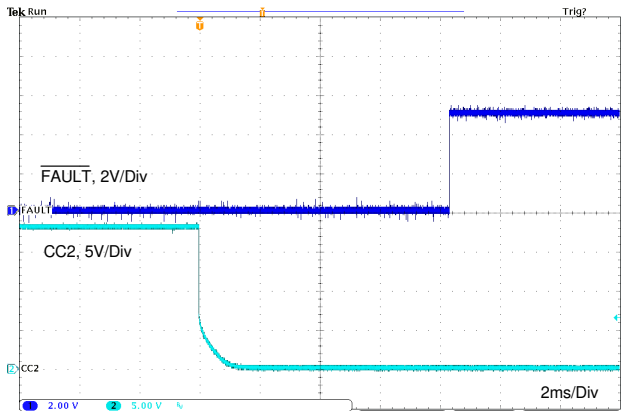
CC1 = R_d CC2 = OPEN NO LOAD

图 11-36. VBUS Short to BAT Recovery With External FET



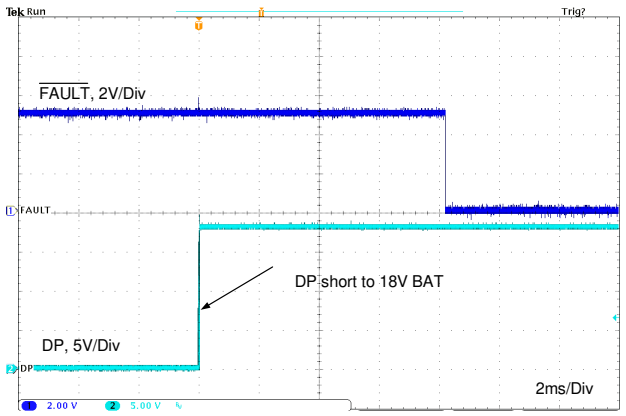
CC1 = R_d CC2 = OPEN NO LOAD

图 11-37. CC Short to BAT



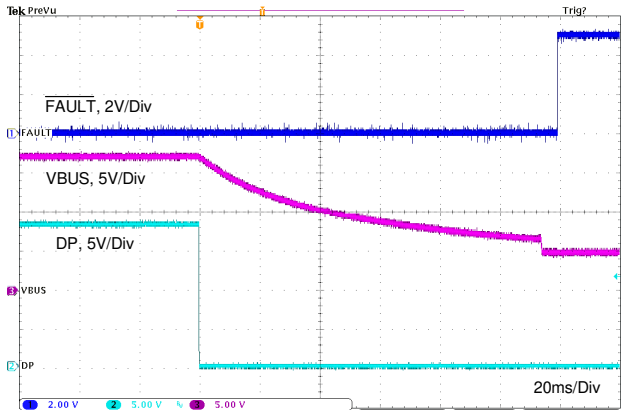
CC1 = R_d CC2 = OPEN NO LOAD

图 11-38. CC Short to BAT Recovery



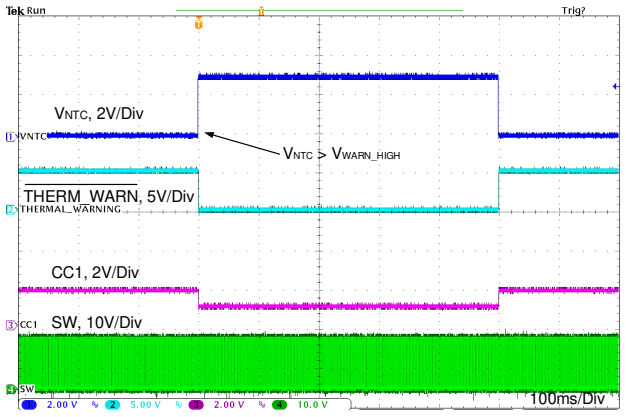
CC1 = R_d CC2 = OPEN NO LOAD

图 11-39. DP Short to BAT



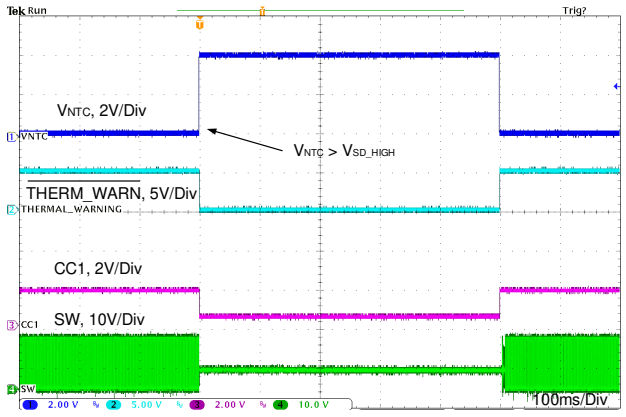
CC1 = R_d CC2 = OPEN NO LOAD

图 11-40. DP Short to BAT Recovery



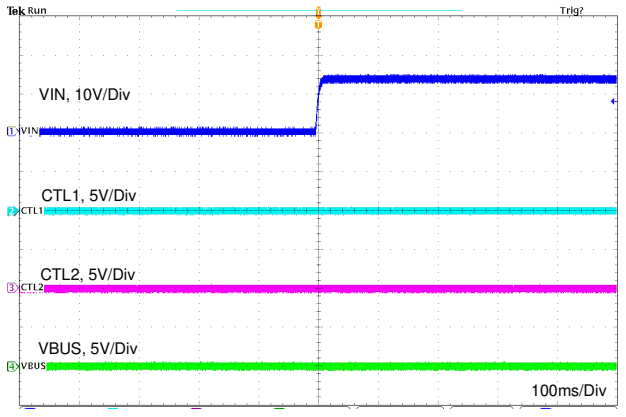
V_{NTC} = 0 V to 3 V CC1 = R_d CC2 = OPEN

图 11-41. Thermal Sensing with NTC Behavior 1



V_{NTC} = 0 V to 4 V CC1 = R_d CC2 = OPEN

图 11-42. Thermal Sensing with NTC Behavior 2



V_{IN} = 0 V to 13.5 V CC1 = R_d CTRL12 = 00

图 11-43. Client mode Startup

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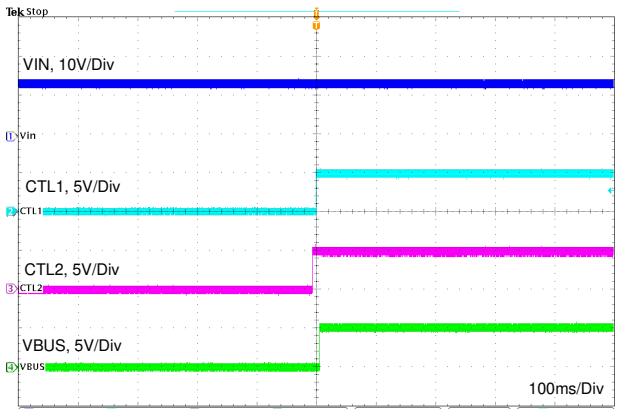

V_{IN}13.5 V　　CC1 = R_d　　CTRL12 = 00 to 11

图 11-44. Client Mode to CDP Mode

12 Power Supply Recommendations

The TPS2583xA-Q1 is designed to operate from an input voltage supply range between 6 V and 36 V. This input supply should be able to withstand the maximum input current and maintain a stable voltage. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the TPS2583xA-Q1 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the TPS2583x, additional bulk capacitance may be required in addition to the ceramic input capacitors. The amount of bulk capacitance is not critical, but a 47-μF or 100-μF electrolytic capacitor is a typical choice.

13 Layout

13.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI. For more detailed EMC design consideration and test report, please refer to PCB Layout and Parameters Recommendation for TPS2583X EMC Performance.

1. ***Input capacitor:*** The input bypass capacitor C_{IN} must be placed as close as possible to the IN and PGND pins. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the PGND pin and PAD. A combination of different values and packages of capacitors can help improve the EMC performance (for example: 10 μF + 0.1 μF + 2.2 nF). Besides, the distance between the input filter section and the output power section must be at least 15 mm to prevent the output high-frequency signal from coupling into the input filter. A 10-uF cap cross V_{IN} and PGND pin on top of SW is suggested for TPS2583x-Q1.
2. ***V_{CC} bypass capacitor:*** Place bypass capacitors for V_{CC} close to the VCC pin and ground the bypass capacitor to device ground.
3. Use a ground plane in one of the middle layers as noise shielding and heat dissipation path.
4. Connect the thermal pad to the ground plane. The QFN package has a thermal pad (PAD) connection that must be soldered down to the PCB ground plane. This pad acts as a heat-sink connection. The integrity of this solder connection has a direct bearing on the total effective $R_{\theta JA}$ of the application.
5. Make V_{IN}, V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
6. Provide enough PCB area for proper heat sinking. As stated in the section, enough copper area must be used to ensure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper; and no less than one ounce. Use an array of heat-sinking vias to connect the thermal pad (PAD) to the ground plane on the bottom PCB layer. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes.
7. The SW pin connecting to the inductor should be as short as possible, and just wide enough to carry the load current without excessive heating. Short, thick traces or copper pours (shapes) will bring a high current conduction capacity to minimize parasitic resistance, but it will also cause a larger parasitic capacitance. Thus a balance should be found between smaller parasitic resistance and larger parasitic capacitance. And the current path should be kept straight forward to the inductor, otherwise the L-shaped or T-shaped path will make a sudden change of the impedance which causes signal reflection and impacts the performance of EMC. The output capacitors should be placed close to the V_{OUT} end of the inductor and closely grounded to PGND pin and exposed PAD. Besides, do not punch vias on SW lines. Using shielded inductors or molded inductors to reduce high-frequency radiation.
8. ***Sense and Set Resistors:*** The R_{SNS} and R_{SET} resistors connect to the current sense amplifier inputs at the CSP and CSN/OUT pins. For best current limit and cable compensation accuracy; short, parallel traces give the best performance. If it is not possible to place R_{SNS} and R_{SET} near the CSP and CSN/OUT pins, it is recommended that the traces from sense resistor be routed in parallel and of similar lengths. A small filter capacitor in parallel with R_{SNS} and a small filter capacitor from CSN/OUT to AGND help decouple noise.
9. R_{ILIMIT} and R_{IMON} resistors should be placed as close as possible to the ILIMIT and IMON pins and connected to AGND. If needed, these components can be placed on the bottom side of the PCB with signals routed through small vias.

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10. Trace routing of DP_IN, DM_IN, DP_OUT, and DM_OUT: Route these traces as micro-strips with nominal differential impedance of 90 Ω. Minimize the use of vias in the high-speed data lines. Keep the reference GND plane devoid from cuts or splits above the differential pairs to prevent impedance discontinuities.
11. Keep the CC lines close to the same length. Do not create stubs or test points on the CC lines.
12. $\overline{\text{POL}}$, $\overline{\text{LD_DET}}$, $\overline{\text{FAULT}}$ and $\overline{\text{THERM_WARN}}$ (TPS25831-Q1) are open-drain outputs. They can be connected to the VCC pin via pull-up resistors. Suggested resistor value is 100 kΩ.
13. The area enclosed by current loop of input side and output side should be as small as possible; the area enclosed by the BOOT circuit should be as small as possible.
14. Power ground PGND and the signal ground AGND should be separated in the actual PCB layout.

13.2 Ground Plane and Thermal Considerations

It is recommended to use one of the middle layers as a solid ground plane. Ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. The PGND pins should be connected to the ground plane using vias right next to the bypass capacitors. PGND pin is connected to the source of the internal LS switch. The PGND net contains noise at switching frequency and may bounce due to load variations. PGND trace, as well as VIN and SW traces, should be constrained to one side of the ground plane. The other side of the ground plane contains much less noise and should be used for sensitive routes. AGND and PGND should be connected under the QFN package PAD.

It is recommended to provide adequate device heat sinking by utilizing the PAD of the IC as the primary thermal path. Use a minimum 2 row, 2 column "+" array of 12 mil thermal vias to connect the PAD to the system ground plane heat sink. The vias should be evenly distributed under the PAD. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top of, 2 oz / 1 oz / 1 oz / 2 oz. Four layer boards with enough copper thickness provide low current conduction impedance, proper shielding and lower thermal resistance.

The thermal characteristics of the TPS2583x-Q1 are specified using the parameter θ_{JA}, which characterize the junction temperature of silicon to the ambient temperature in a specific system. Although the value of θ_{JA} is dependent on many variables, it still can be used to approximate the operating junction temperature of the device. To obtain an estimate of the device junction temperature, one may use the following relationship:

$$T_J = P_D \times \theta_{JA} + T_A \quad (15)$$

where

T_J = Junction temperature in °C

$P_D = V_{IN} \times I_{IN} \times (1 - \text{Efficiency}) - 1.1 \times I_{OUT}^2 \times \text{DCR}$ in Watt

DCR = Inductor DC parasitic resistance in Ω

θ_{JA} = Junction to ambient thermal resistance of the device in °C/W

T_A = Ambient temperature in °C

θ_{JA} is highly related to PCB size and layout, as well as environmental factors such as heat sinking and air flow.

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13.3 Layout Example

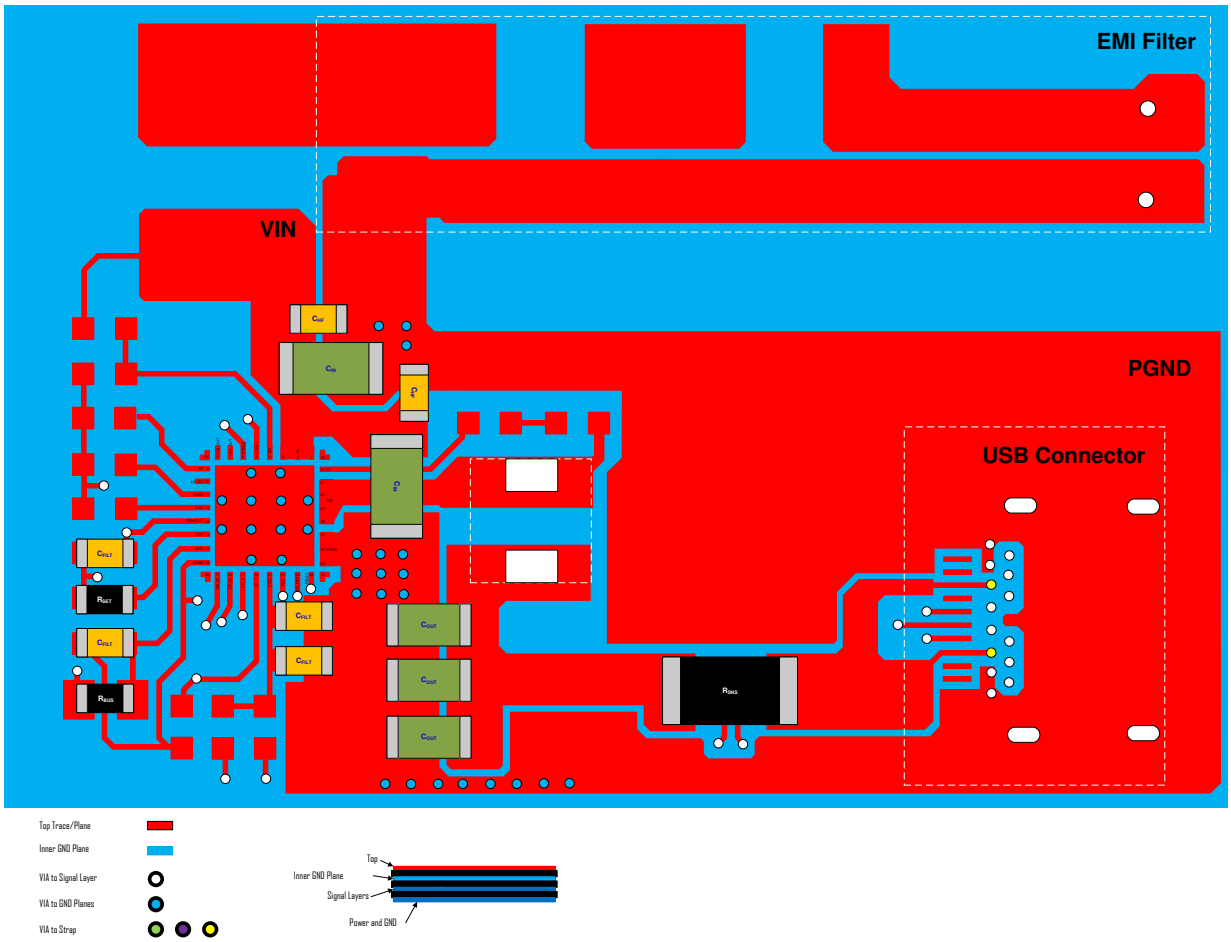

图 13-1. Layout

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14 Device and Documentation Support

14.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 14-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS25830A-Q1	Click here	Click here	Click here	Click here	Click here
TPS25832A-Q1	Click here	Click here	Click here	Click here	Click here

14.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

14.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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14.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS25830AQCWRHBRQ1	ACTIVE	VQFN	RHB	32	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T25830A	Samples
TPS25830AQWRHBRQ1	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	T25830A	Samples
TPS25832AQCWRHBRQ1	ACTIVE	VQFN	RHB	32	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T25832A	Samples
TPS25832AQWRHBRQ1	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	T25832A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

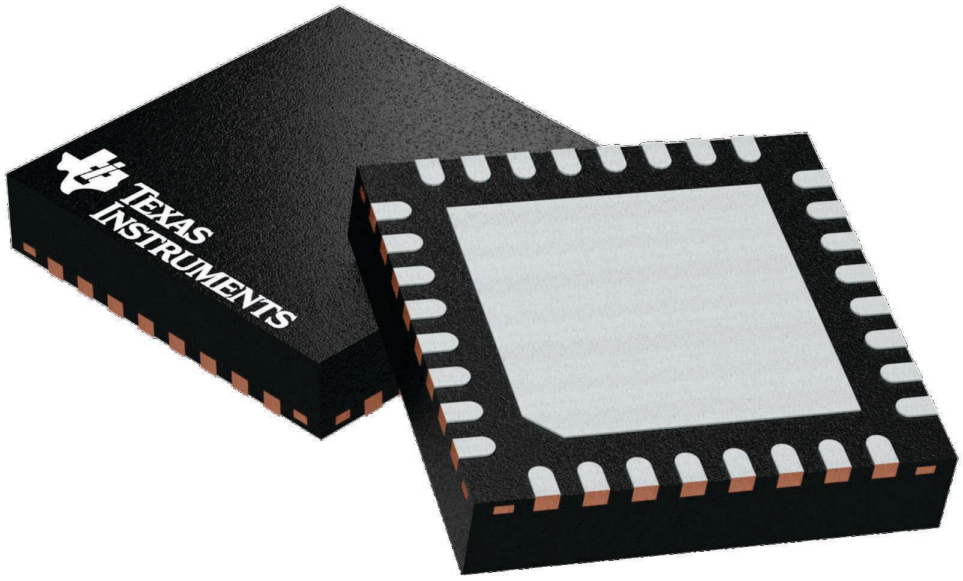
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

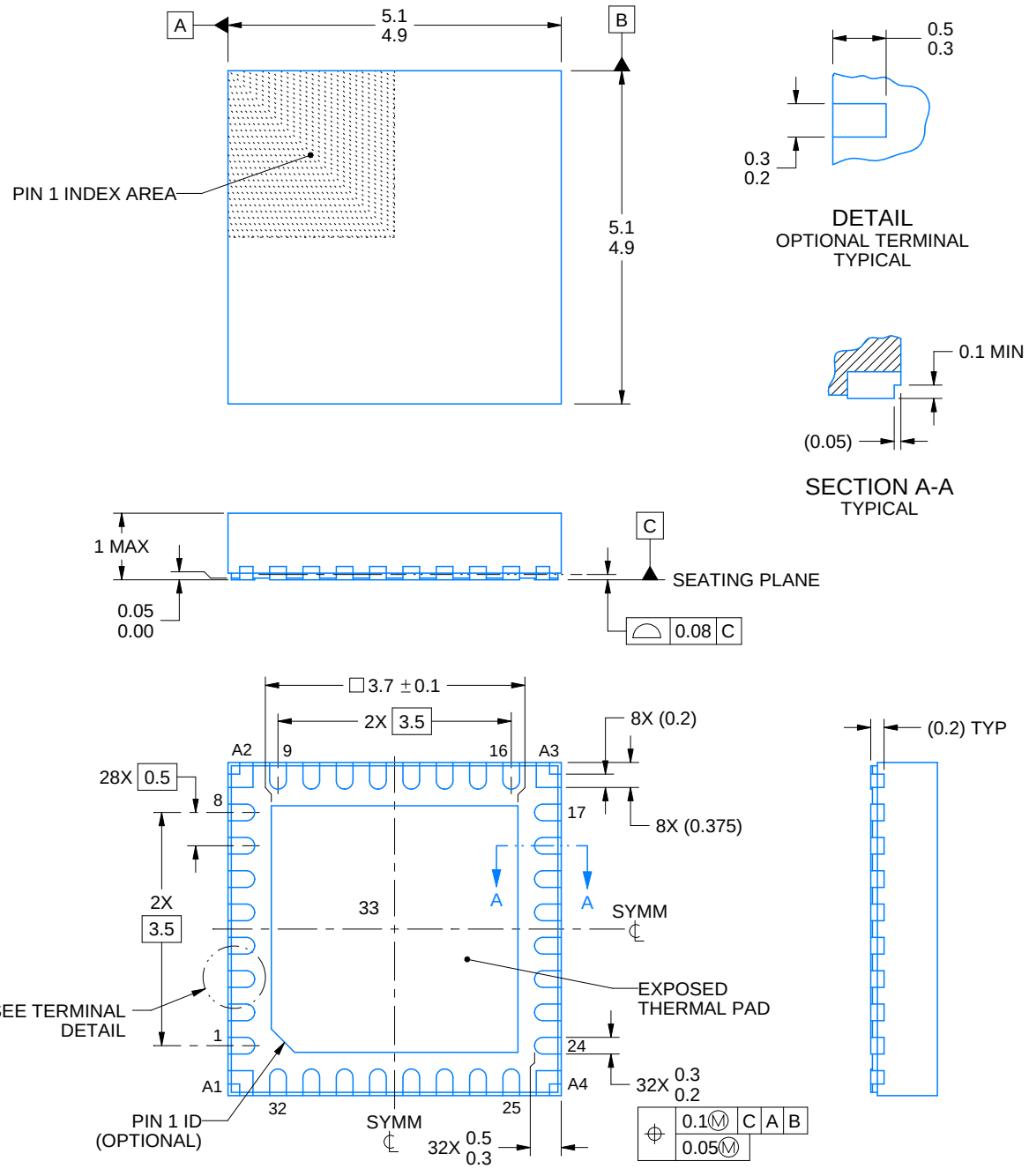
4224745/A

PACKAGE OUTLINE

RHB0032R

VQFN - 1 mm max height

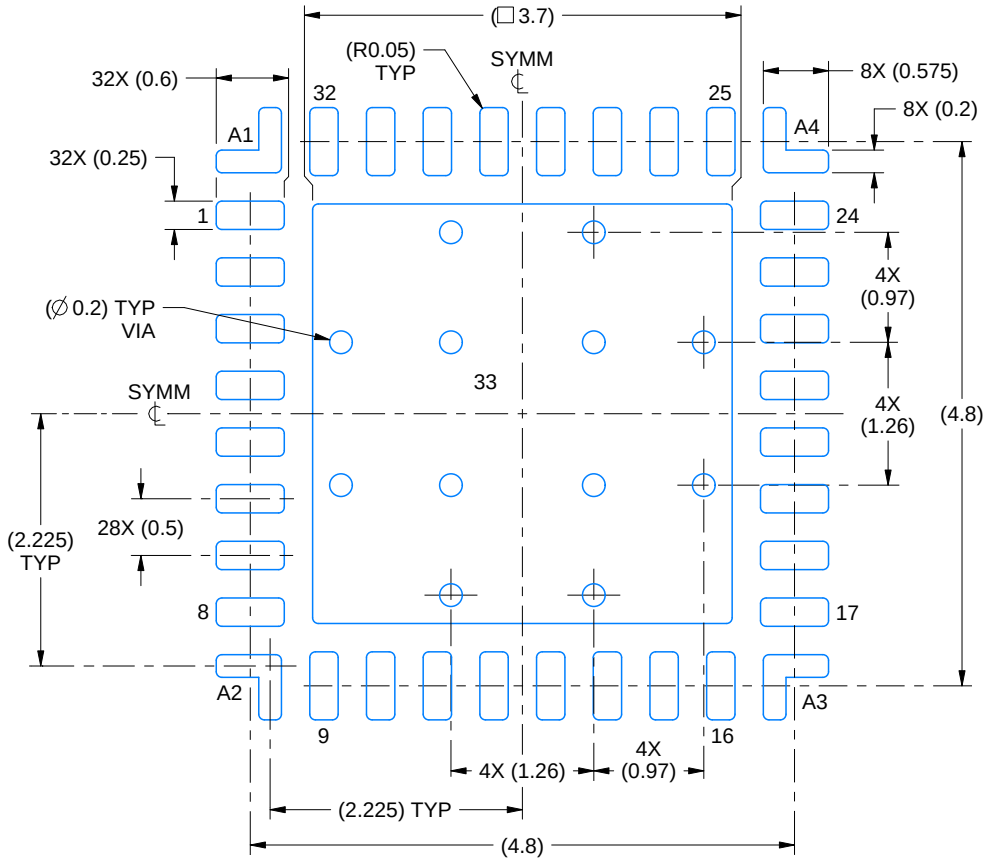
PLASTIC QUAD FLATPACK - NO LEAD



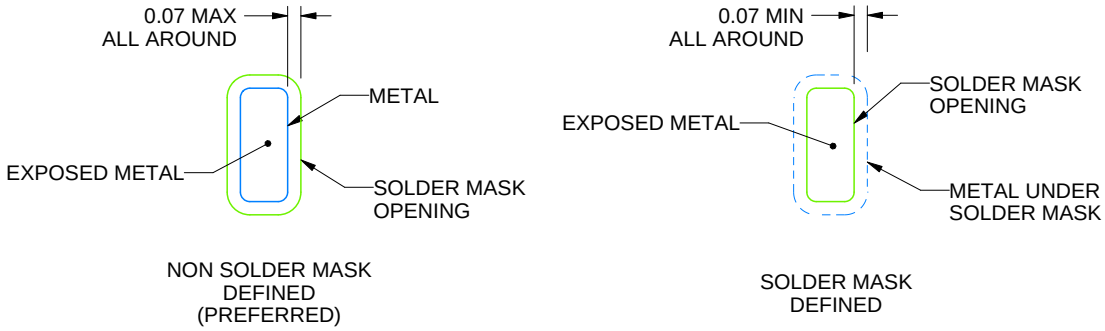
4223771/A 06/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

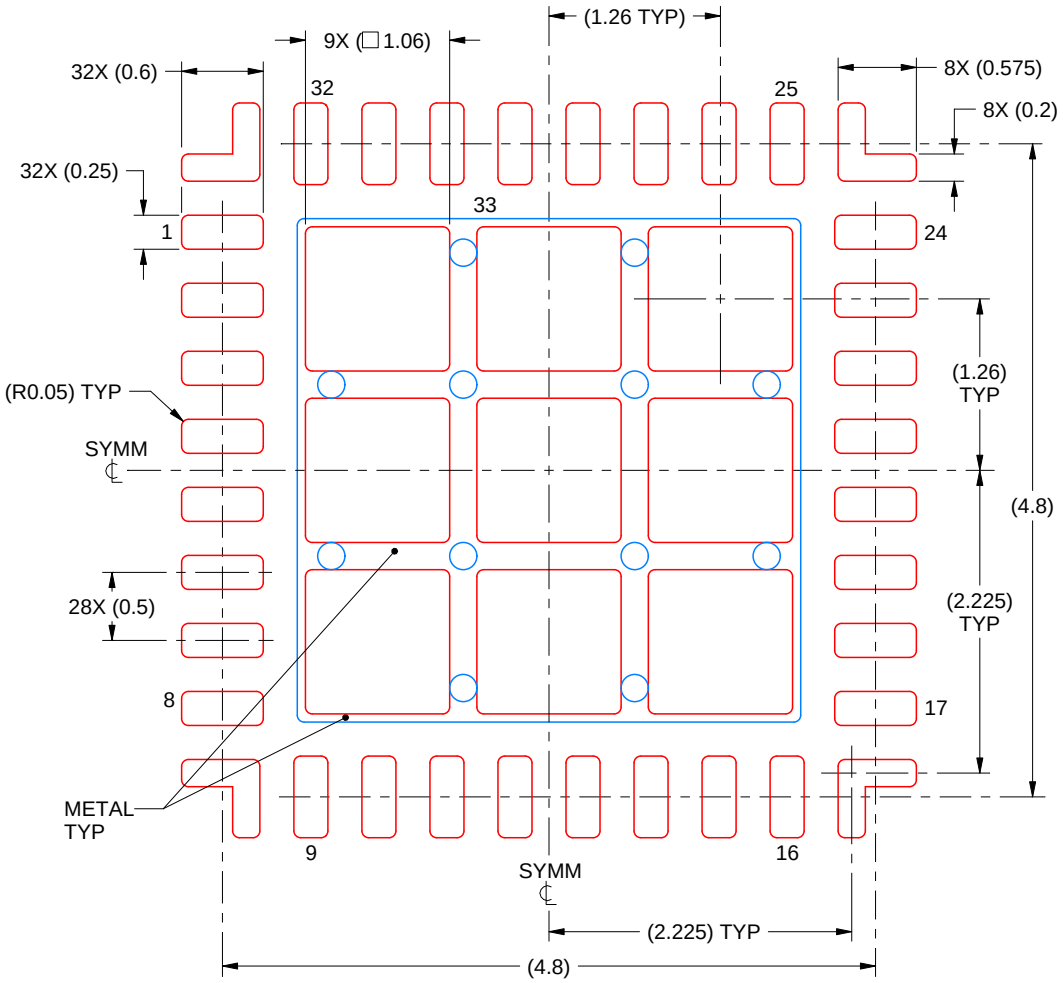


SOLDER MASK DETAILS

4223771/A 06/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33
74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:18X

4223771/A 06/2017

NOTES: (continued)

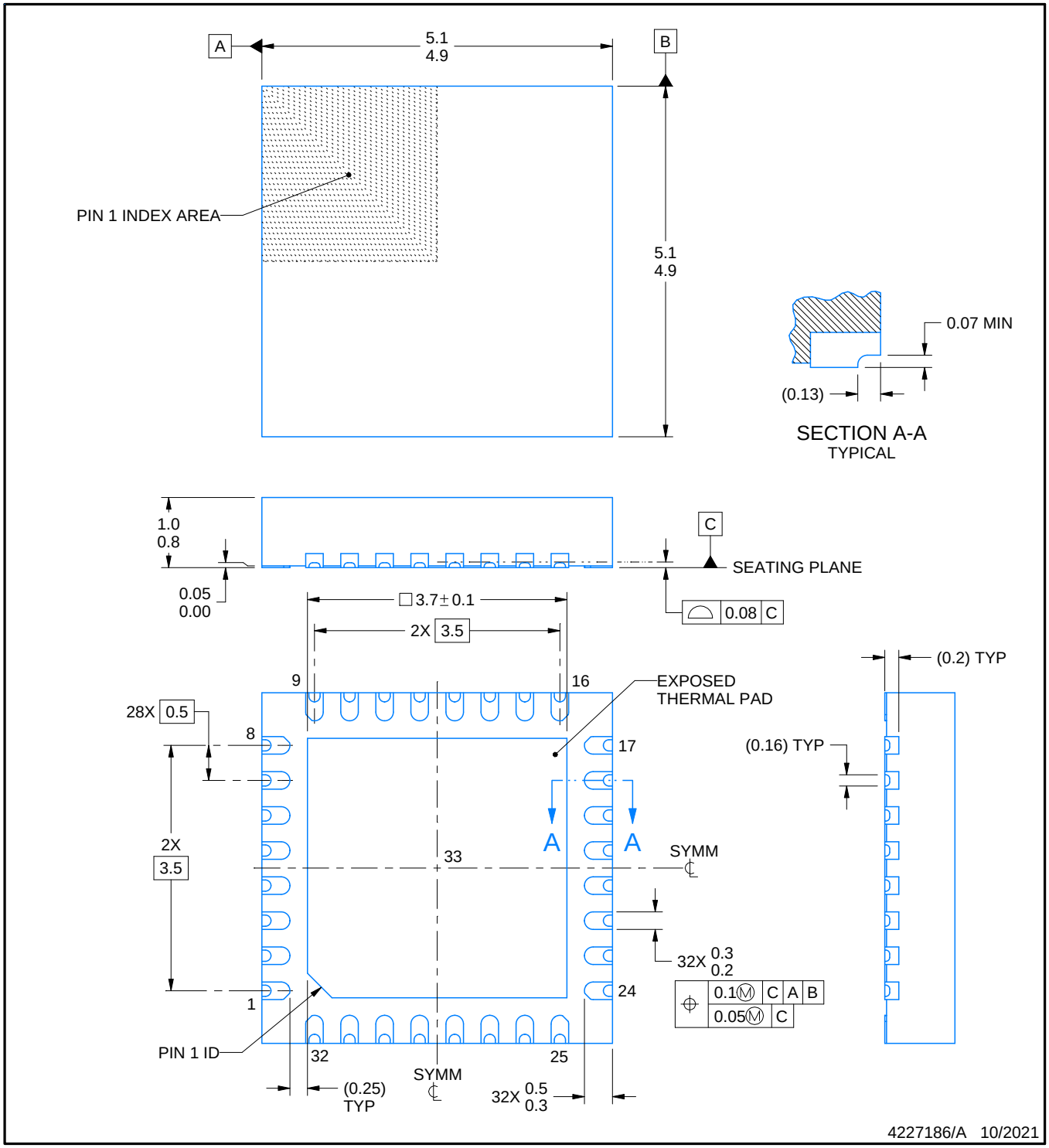
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RHB0032AA

PACKAGE OUTLINE

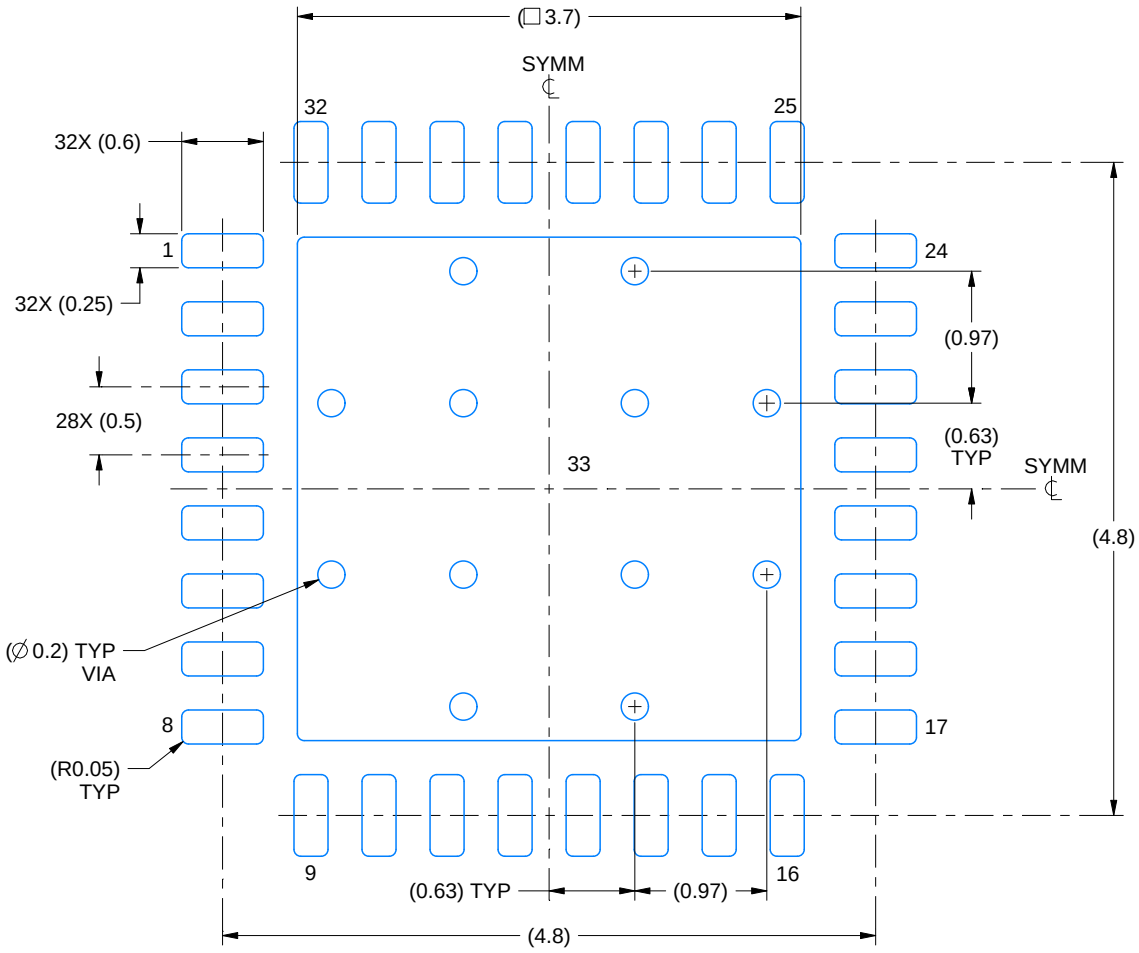
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

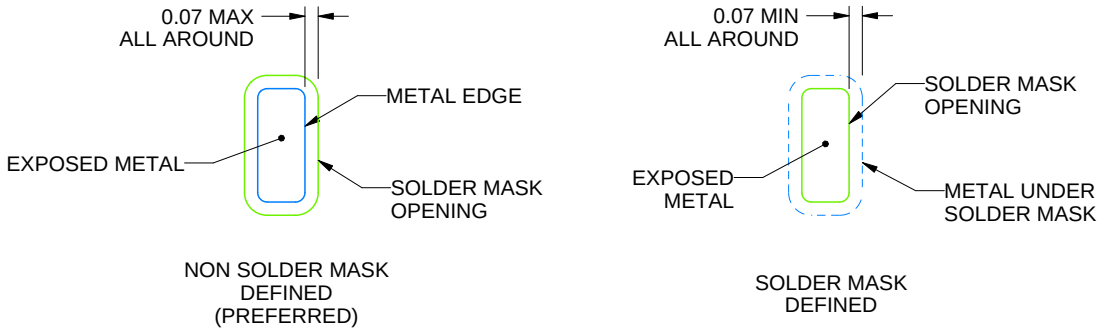
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE:18X

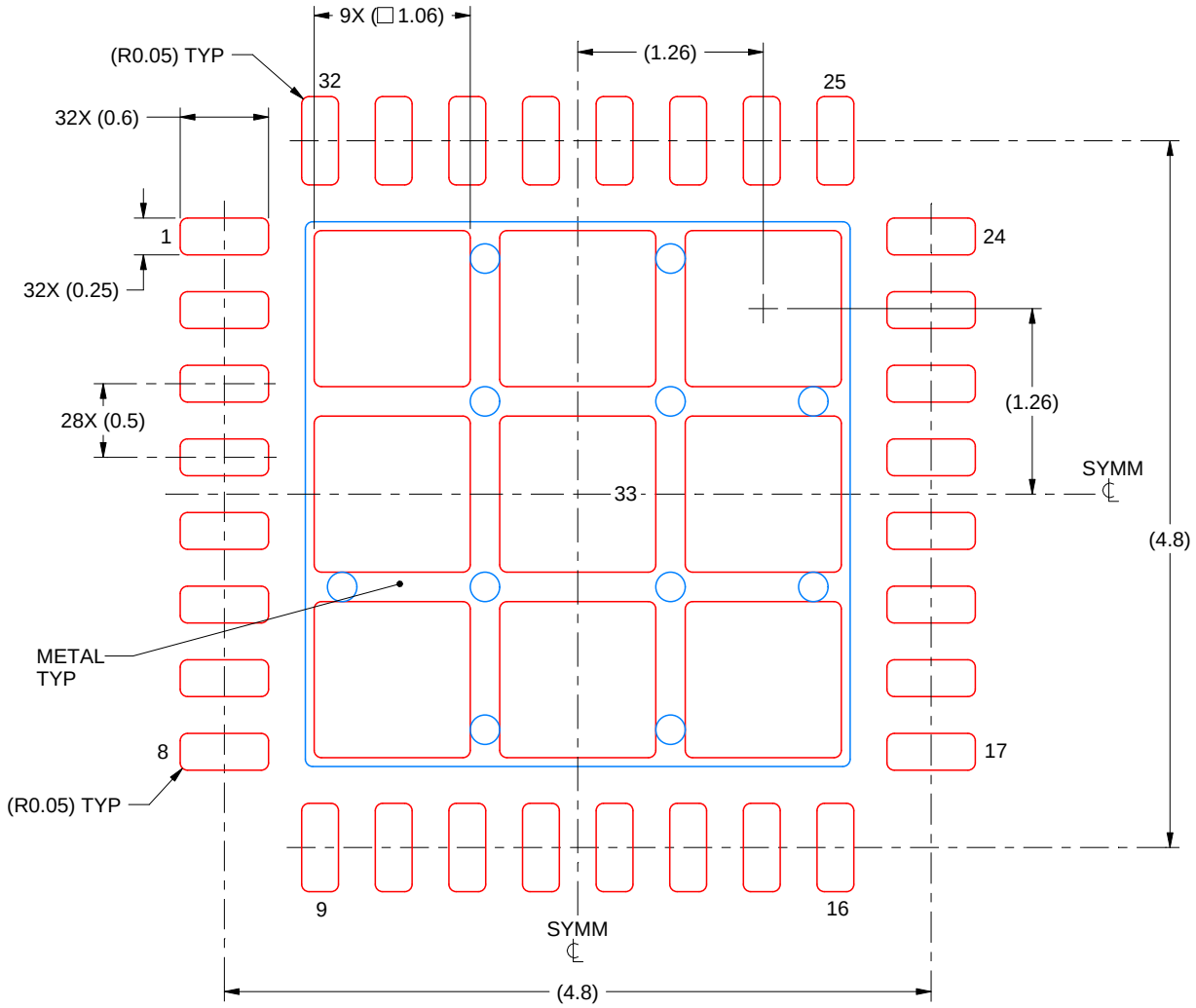


SOLDER MASK DETAILS

4227186/A 10/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4227186/A 10/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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