TPS53321 5-A Step-Down Regulator With Integrated Switcher

1 Features

- 96% Maximum Efficiency
- Continuous 5-A Output Current
- Supports All MLCC Output Capacitor
- SmoothPWM™ Auto-Skip Eco-Mode™ for Light-Load Efficiency
- Optimized Efficiency at Light and Heavy Loads
- Voltage Mode Control
- Supports Master-Slave Interleaved Operation
- Synchronization up to ±20% of Nominal Frequency
- Conversion Voltage Range Between 2.9 V and 6 V
- Soft-Stop Output Discharge During Disable
- Adjustable Output Voltage Ranging Between 0.6 V and 0.84 V × V_{IN}
- Overcurrent, Overvoltage, and Overtemperature Protection
- Small 3 mm × 3 mm, 16-Pin QFN Package
- Open-Drain Power Good Indication
- Internal Boot Strap Switch
- Low $R_{DS(on)}$, 24 mΩ With 3.3-V Input and 19-mΩ With 5-V Input
- Supports Prebias Start-Up

2 Applications

- 5-V Step-Down Rails
- 3.3-V Step-Down Rails

3 Description

The TPS53321 device provides a fully integrated 3-V to 5-V V_{IN} integrated synchronous FET converter solution with 16 total components in 200 mm^2 of PCB area. Due to the low ON-resistance and TI's Proprietary SmoothPWM™ skip mode of operation, it enables 96% peak efficiency and over 90% efficiency at loads as light as 100 mA. It requires only two 22-µF ceramic output capacitors for a power dense 5-A solution.

The TPS53321 features a 1.1-MHz switching frequency, skip mode operation support, prebias start-up, internal soft start, output soft discharge, internal VBST switch, power good, EN/input UVLO, overcurrent, overvoltage, undervoltage, and overtemperature protections, and all ceramic output capacitor support. It supports supply voltage from 2.9 V to 3.5 V and conversion voltage from 2.9 V to 6 V. The output voltage is adjustable from 0.6 V to 0.84 V × V_{IN}.

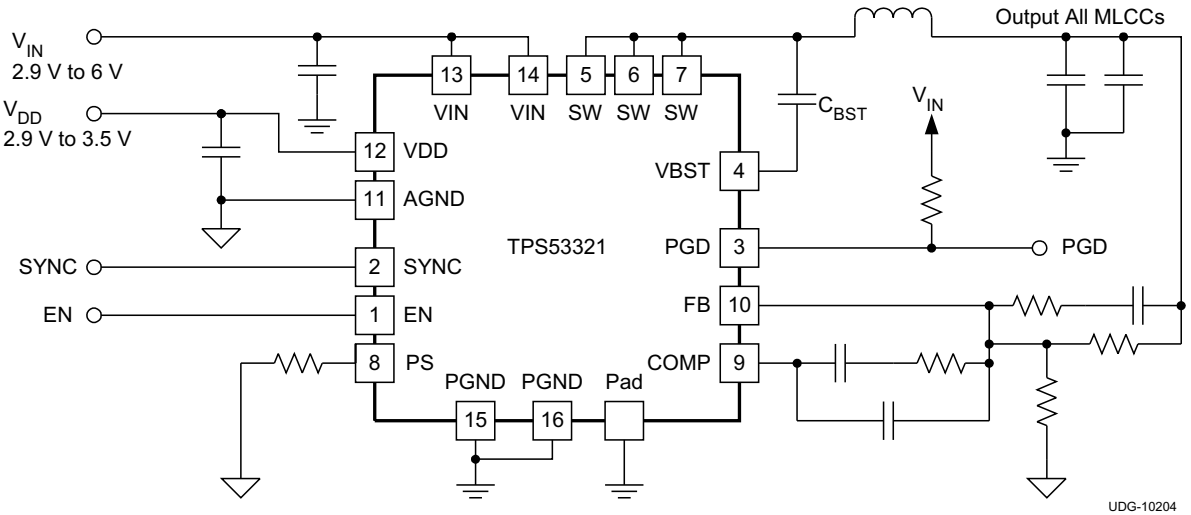
The TPS53321 is available in the 3 mm × 3 mm 16-pin QFN package (Green RoHs compliant and Pb free) and operates between –40°C and 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS53321	QFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

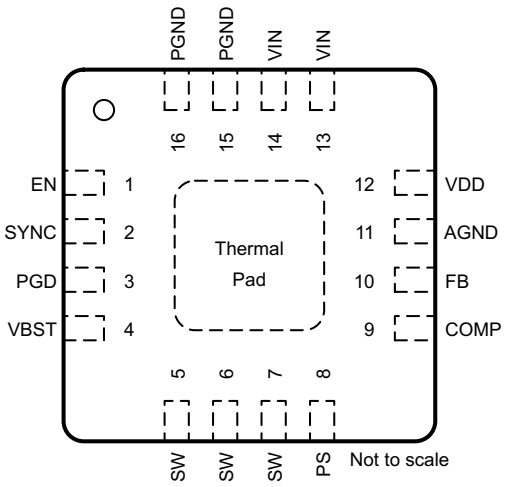
Changes from Original (December 2010) to Revision A **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table; see POA at the end of the data sheet ... 1
- Deleted Lead temperature, 1.6 mm (1/16 inch) from case for 10 seconds: 300°C ... 4
- Deleted *Package Dissipation Ratings* table ... 5
- Added *Thermal Information* table ... 5
- Changed R2 value in *Typical 3.3-V Input Application Circuit Diagram* From: 4.02 kΩ To: 2.67 kΩ ... 12
- Changed R2 value in *Master and Slave Configuration Schematic* From: 4.02 kΩ To: 2.67 kΩ ... 16
- Changed R12 value in *Master and Slave Configuration Schematic* From: 2.67 kΩ To: 4.02 kΩ ... 16

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5 Pin Configuration and Functions

RGT Package
16-Pin QFN
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	EN	I	Enable. Internally pulled up to VDD with a 1.35-MΩ resistor.
2	SYNC	B	Synchronization signal for input interleaving. Master SYNC pin sends out 180° out-of-phase signal to slave SYNC. SYNC frequency must be within ±20% of slave nominal frequency.
3	PGD	O	Power good output flag. Open-drain output. Pull up to an external rail through a resistor.
4	VBST	P	Supply input for high-side MOSFET (bootstrap terminal). Connect capacitor from this pin to SW terminal.
5	SW	B	Output inductor connection to integrated power devices
6	SW	B	Output inductor connection to integrated power devices
7	SW	B	Output inductor connection to integrated power devices
8	PS	I	Mode configuration pin (with 10-µA current): Connecting to ground: FCCM slave Pulled high or floating (internal pulled high): FCCM master Connect a 24.3-kΩ resistor to GND: DE slave Connect a 57.6-kΩ resistor to GND: HEF mode Connect a 105-kΩ resistor to GND : reserved mode Connect a 174-kΩ resistor to GND: DE master
9	COMP	O	Error amplifier compensation terminal. Type III compensation method is recommended for stability.
10	FB	I	Voltage feedback. Also used for OVP, UVP, and PGD determination.
11	AGND	G	Device analog ground terminal
12	VDD	P	Input bias supply for analog functions
13	VIN	P	Gate driver supply and power conversion voltage input
14	VIN	P	Gate driver supply and power conversion voltage input
15	PGND	P	IC power GND terminal
16	PGND	P	IC power GND terminal

(1) B = Bidirectional, G = Ground, I = Input, O = Output, P = Supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Input voltage	VIN, EN		–0.3	7	V
	VBST		–0.3	17	
	VBST(with respect to SW)		–0.3	7	
	FB, PS, VDD		–0.3	3.7	
Output voltage	SW	DC	–0.3	7	V
		Pulse < 20 ns, E = 5 µJ	–3	10	
	PGD		–0.3	7	
	COMP, SYNC		–0.3	3.7	
	PGND		–0.3	0.3	
Junction temperature, T_J			–40	150	°C
Ambient temperature, T_A			–40	85	°C
Storage temperature, T_{stg}			–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
	Input voltage	VIN	2.9		6	V
		VDD	2.9	3.3	3.5	
		VBST	–0.1		13.5	
		VBST(with respect to SW)	–0.1		6	
		EN	–0.1		6	
		FB, PS	–0.1		3.5	
	Output voltage	SW	–1		6.5	V
		PGD	–0.1		6	
		COMP, SYNC	–0.1		3.5	
		PGND	–0.1		0.1	
T_J	Junction temperature		–40		125	°C

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6.4 Thermal Information

THERMAL METRIC[1]		TPS53321 RGT (QFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended free-air temperature range, V_{IN} = 3.3 V, V_{VDD} = 3.3 V, and PGND = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY: VOLTAGE, CURRENTS, and UVLO						
V_{IN}	VIN supply voltage	Nominal input voltage range	2.9		6	V
I_{VINSDN}	VIN shutdown current	EN = LO			3	µA
V_{UVLO}	VIN UVLO threshold	Ramp up, EN = HI		2.8		V
$V_{UVLOHYS}$	VIN UVLO hysteresis	VIN UVLO Hysteresis		130		mV
V_{DD}	Internal circuitry supply voltage	Nominal 3.3-V input voltage range	2.9	3.3	3.5	V
I_{DDSDN}	VDD shutdown current	EN = LO			5	µA
I_{DD}	Standby current	EN = HI, no switching		2.2	3.5	mA
V_{DDUVLO}	3.3-V UVLO threshold	Ramp up, EN = HI		2.8		V
$V_{DDUVLOHYS}$	3.3-V UVLO hysteresis			75		mV
VOLTAGE FEEDBACK LOOP: VREF AND ERROR AMPLIFIER						
V_{VREF}	VREF	Internal precision reference voltage		0.6		V
$TOLV_{REF}$	VREF Tolerance	0°C ≤ T_A ≤ 85°C	–1%		1%	
		–40°C ≤ T_A ≤ 85°C	–1.25%		1.25%	
UGBW[1]	Unity gain bandwidth		14			MHz
A_{OL}[1]	Open-loop gain		80			dB
I_{FBINT}	FB input leakage current	Sourced from FB pin			30	nA
I_{EAMAX}[1]	Output sinking and sourcing current	C_{COMP} = 20 pF		5		mA
SR[1]	Slew rate			5		V/µs
OCP: OVERCURRENT AND ZERO CROSSING						
I_{OCPL}	Overcurrent limit on upper FET	When I_{OUT} exceeds this threshold for 4 consecutive cycles. V_{IN}=3.3 V, V_{OUT}=1.5 V with 1-µH inductor, T_A = 25°C	6	6.5	7	A
I_{OCPH}	One time overcurrent latch off on the lower FET	Immediately shuts down when sensed current reach this value. V_{IN}=3.3 V, V_{OUT}=1.5 V with 1-µH inductor, T_A = 25°C	6.25	6.8	7.35	A
t_{HICCUP}	Hiccup time interval		12.5	14.5	16.5	ms
V_{ZXOFF}[1]	Zero crossing comparator internal offset	PGND – SW, skip mode	–4.5	–3	–1.5	mV
PROTECTION: OVP, UVP, PGD, AND INTERNAL THERMAL SHUTDOWN						
V_{OVP}	Overvoltage protection threshold voltage	Measured at FB w/r/t VREF	114%	117%	120%	
V_{UVP}	Undervoltage protection threshold voltage	Measured at FB w/r/t VREF	80%	83%	86%	

(1) Ensured by design. Not production tested.

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Electrical Characteristics (continued)

over recommended free-air temperature range, V_{IN} = 3.3 V, V_{VDD} = 3.3 V, and PGND = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PGDL}	PGD low threshold	Measured at FB w/r/t VREF	80%	83%	86%	
V_{PGDU}	PGD upper threshold	Measured at FB w/r/t VREF	114%	117%	120%	
$V_{INMINPG}$	Minimum Vin voltage for valid PGD at start-up	Measured at V_{IN} with 1-mA (or 2-mA) sink current on PGD pin at start-up		1		V
THSD(1)	Thermal shutdown	Latch off controller, attempt soft-stop	130	140	150	°C
$THSD_{HYS}$(1)	Thermal shutdown hysteresis	Controller restarts after temperature has dropped		40		°C
LOGIC PINS: I/O VOLTAGE AND CURRENT						
V_{PGPD}	PGD pulldown voltage	Pulldown voltage with 4-mA sink current		0.2	0.4	V
I_{PGLK}	PGD leakage current	Hi-Z leakage current, apply 3.3-V in off state	–2	0	2	µA
R_{ENPU}	Enable pullup resistor			1.35		MΩ
V_{ENH}	EN logic high threshold		1.1	1.18	1.3	V
V_{ENHYS}	EN hysteresis			0.18	0.24	V
PS_{THS}	PS mode threshold voltage	Level 1 to level 2(2)		0.12		V
		Level 2 to level 3		0.4		
		Level 3 to level 4		0.8		
		Level 4 to level 5		1.4		
		Level 5 to level 6		2.2		
I_{PS}	PS source	10-µA pullup current when enabled	8	10	12	µA
f_{SYNCSL}	Slave SYNC frequency range	Versus nominal switching frequency	–20%		20%	
PW_{SYNC}	SYNC low pulse width			110		ns
I_{SYNC}	SYNC pin sink current	T_A = 25°C		10		µA
$V_{SYNCTHS}$(1)	SYNC threshold	Falling edge		1		V
$V_{SYNCHYS}$(1)	SYNC hysteresis			0.5		V
BOOT STRAP: VOLTAGE AND LEAKAGE CURRENT						
I_{VBSTLK}	VBST leakage current	V_{IN} = 3.3 V, V_{VBST} = 6.6 V, T_A = 25°C			1	µA
TIMERS: SS, FREQUENCY, RAMP, ON-TIME AND I/O TIMING						
t_{SS_1}	Delay after EN asserting	EN = HI, master or HEF mode		0.2		ms
t_{SS_2}	Delay after EN asserting	EN = HI, slave waiting time		0.5		ms
t_{SS_3}	Soft-start ramp-up time	Rising from V_{SS} = 0 V to V_{SS} = 0.6 V		0.4		ms
$t_{PGDENDLY}$	PGD start-up delay time	Rising from V_{SS} = 0 V to V_{SS} = 0.6 V, from V_{SS} reaching 0.6 V to V_{PGD} going high		1.2		ms
t_{OVPDLY}	Overvoltage protection delay time	Time from FB out of +20% of VREF to OVP fault	1	1.7	2.5	µs
t_{UVPDLY}	Undervoltage protection delay time	Time from FB out of –20% of VREF to UVP fault		11		µs
f_{SW}	Switching frequency control	FCCM	0.99	1.1	1.21	MHz
	Ramp amplitude(1)	2.9 V < V_{IN} < 6.0 V		V_{IN}/4		V
$t_{MIN(off)}$	Minimum OFF time	FCCM or DE mode		100	140	ns
		HEF mode		175	250	
D_{MAX}	Maximum duty cycle, FCCM and DE mode	f_{SW} = 1.1 MHz, 0°C ≤ T_A ≤ 85°C	84%	89%		
	Maximum duty cycle, HEF mode	f_{SW} = 1.1 MHz, 0°C ≤ T_A ≤ 85°C	75%	81%		
R_{SFTSTP}	Soft-discharge transistor resistance	V_{EN} = Low, V_{IN} = 3.3 V, V_{OUT} = 0.5 V		60		Ω

(2) See PS pin description for levels.

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6.6 Typical Characteristics

Inductor PCMC065T-1R0 (1 µH, 5.6 mΩ) is used.

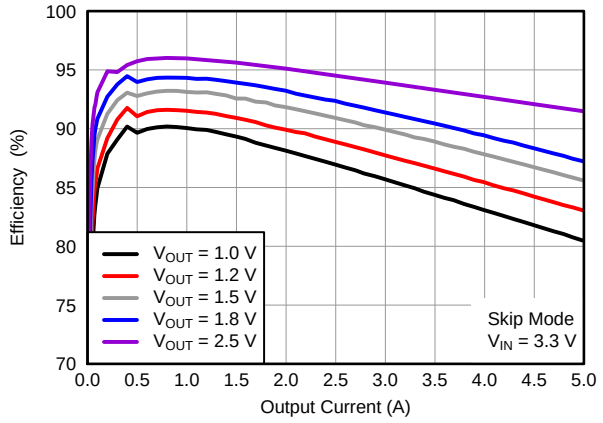


Figure 1. Efficiency vs Output Current, Skip Mode, V_{IN} = 3.3 V

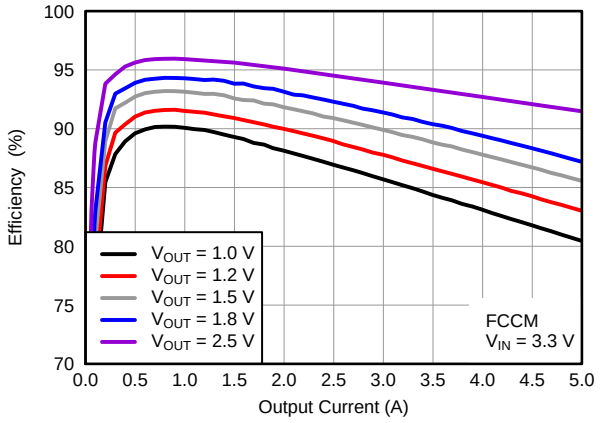


Figure 2. Efficiency vs Output Current, FCCM, V_{IN} = 3.3 V

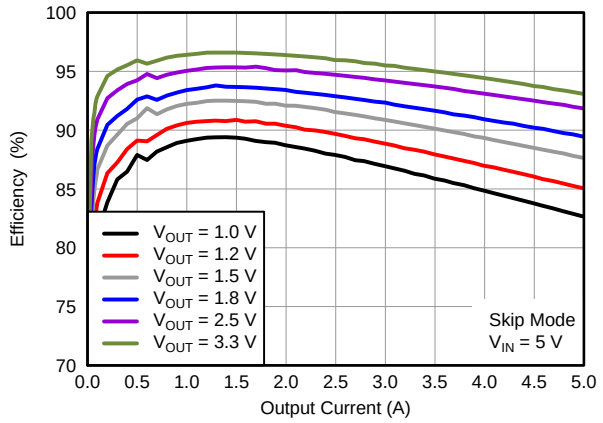


Figure 3. Efficiency vs Output Current, Skip Mode, V_{IN} = 5 V

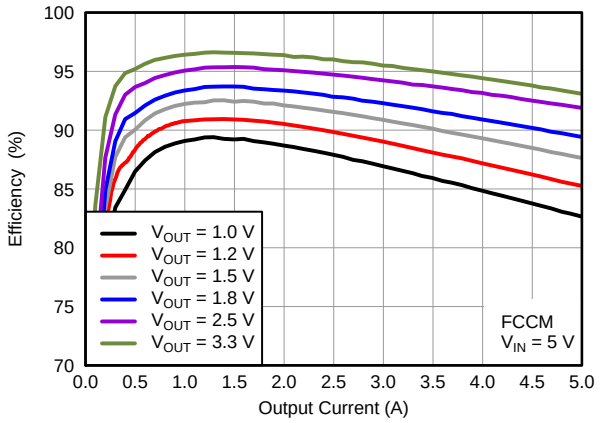


Figure 4. Efficiency vs Output Current, FCCM, V_{IN} = 5 V

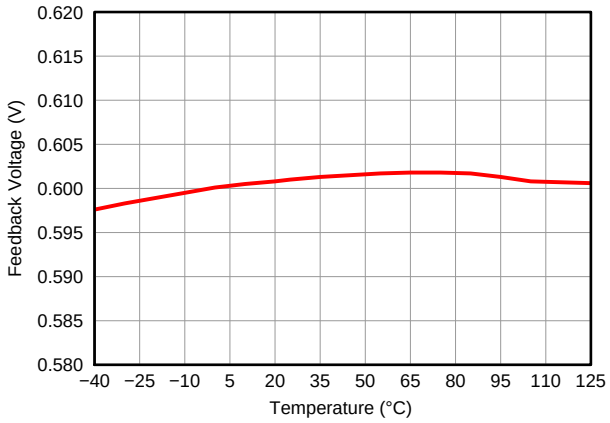


Figure 5. Feedback Voltage vs Ambient Temperature

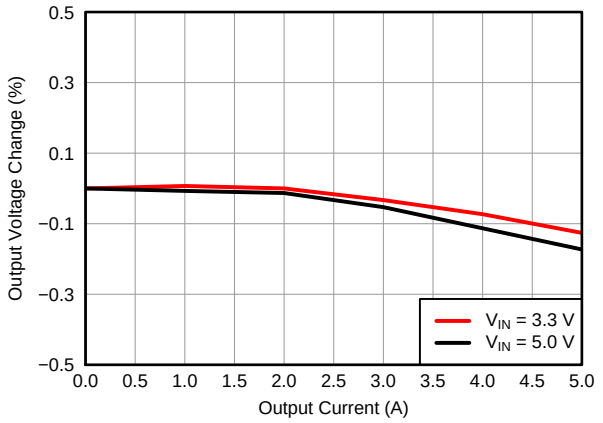


Figure 6. Output Voltage Change vs Output Current

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Typical Characteristics (continued)

Inductor PCMC065T-1R0 (1 µH, 5.6 mΩ) is used.

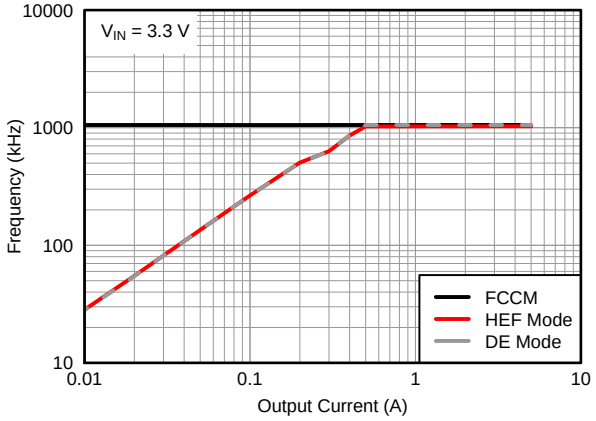


Figure 7. Frequency vs Output Current at V_{IN} = 3.3 V

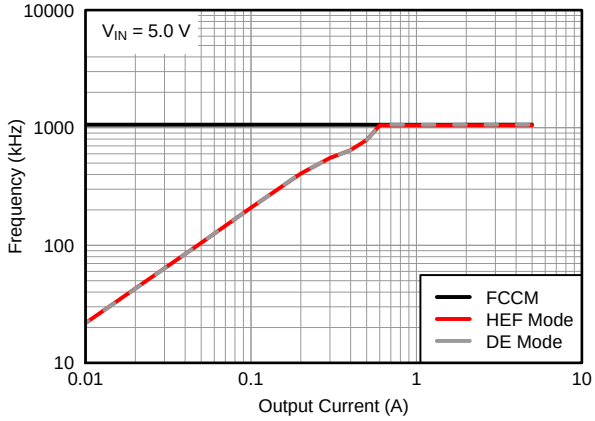


Figure 8. Frequency vs Output Current at V_{IN} = 5 V

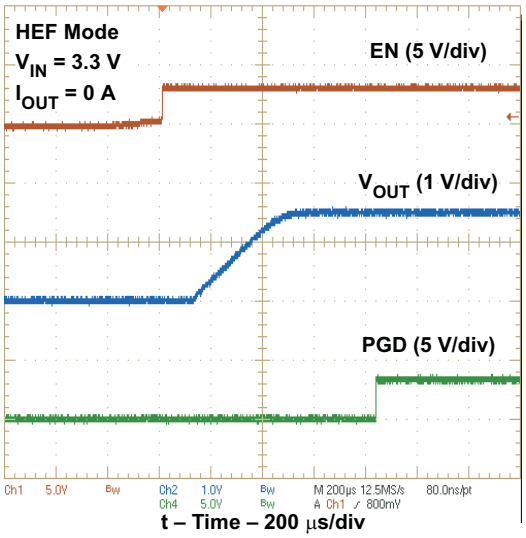


Figure 9. Normal Start-Up Waveform

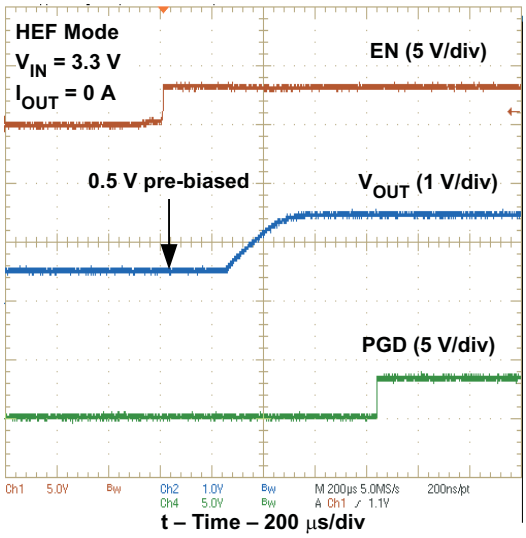


Figure 10. Prebias Start-Up Waveform

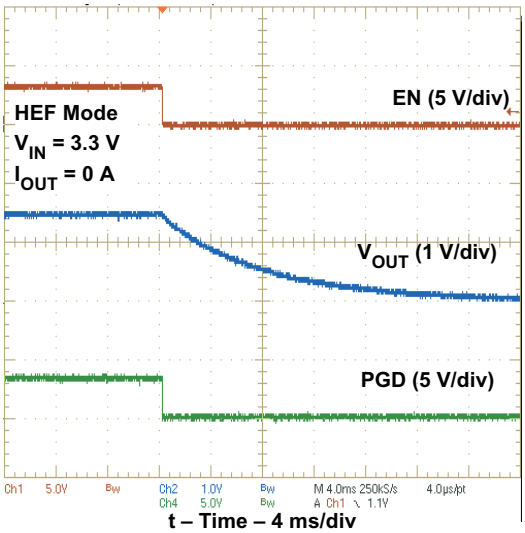


Figure 11. Soft-Stop Waveform

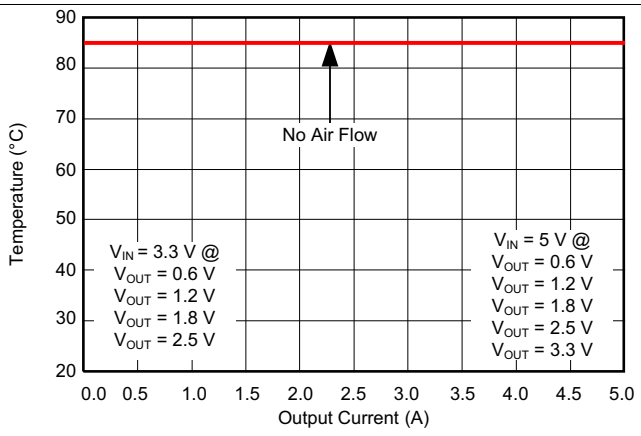


Figure 12. Safe Operating Area

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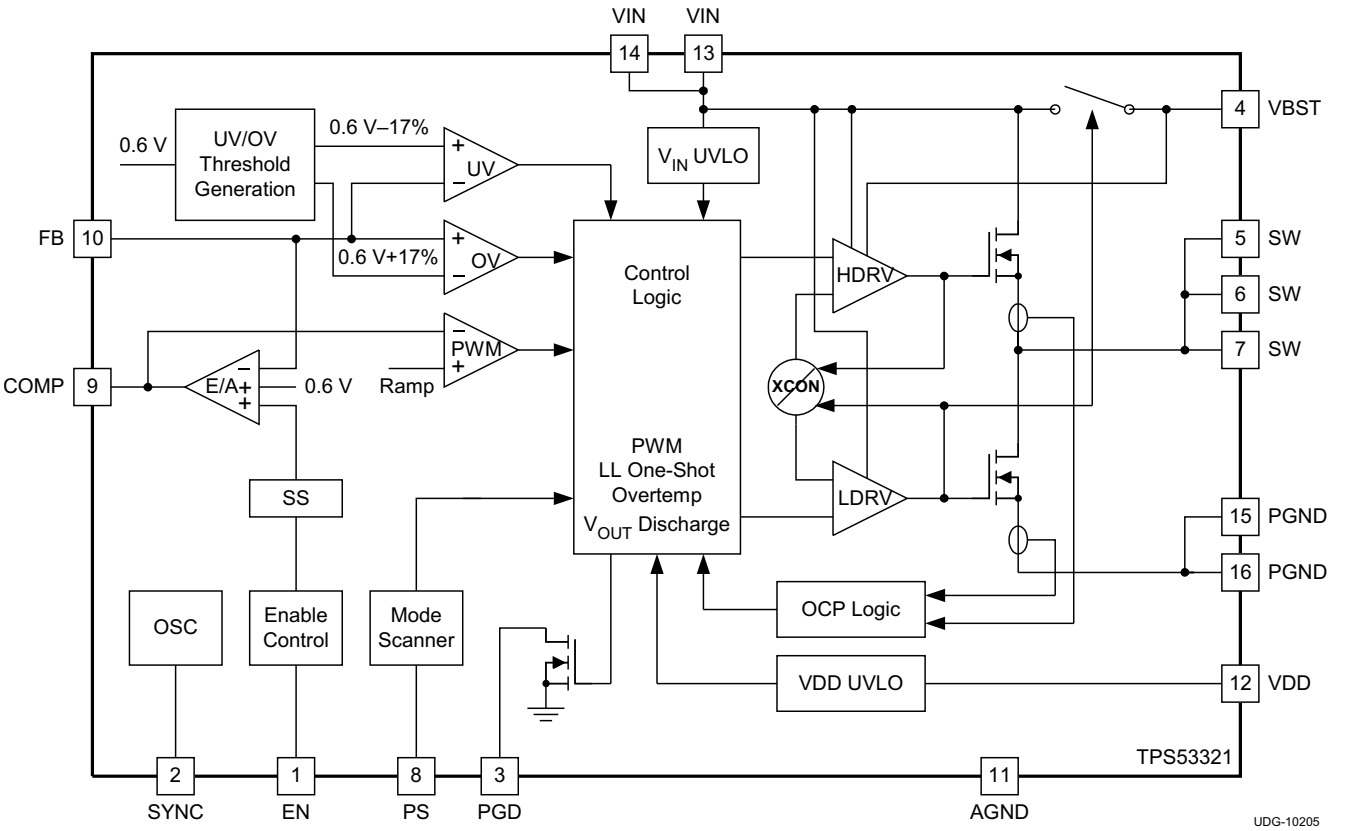
7 Detailed Description

7.1 Overview

The TPS53321 is a high-efficiency switching regulator with two integrated N-channel MOSFETs and is capable of delivering up to 5 A of load current. The TPS53321 provides output voltage between 0.6 V and 0.84 × V_{IN} from 2.9 V to 6 V wide input voltage range.

This device employs five operation modes to fit various application requirements. The *master or slave* mode enables a two-phase interleaved operation to reduce input ripple. The *skip* mode operation provides reduced power loss and increases the efficiency at light load. The unique, patented PWM modulator enables smooth light load to heavy load transition while maintaining fast load transient.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Soft Start

The soft-start function reduces the inrush current during the start up sequence. A slow-rising reference voltage is generated by the soft-start circuitry and sent to the input of the error amplifier. When the soft-start ramp voltage is less than 600 mV, the error amplifier uses this ramp voltage as the reference. When the ramp voltage reaches 600 mV, the error amplifier switches to a fixed 600-mV reference. The typical soft-start time is 400 µs.

7.3.2 Power Good

The TPS53321 monitors the voltage on the FB pin. If the FB voltage is between 83% and 117% of the reference voltage, the power good signal remains high. If the FB voltage falls outside of these limits, the internal open-drain output pulls the power good pin (PGD) low.

Feature Description (continued)

During start-up, V_{IN} must be higher than 1 V to have valid power good logic, and the power good signal is delayed for 1.2 ms after the FB voltage falls to within the power good limits. There is also 10-µs delay during the shutdown sequence.

7.3.3 Undervoltage Lockout (UVLO) Protection

The TPS53321 provides undervoltage lockout (UVLO) protection for both power input (V_{IN}) and bias input (VDD) voltage. If either of them is lower than the UVLO threshold voltage minus the hysteresis, the device shuts off. When the voltage rises above the threshold voltage, the device restarts. The typical UVLO rising threshold is 2.8 V for both V_{IN} and V_{VDD}. A hysteresis voltage of 130 mV for V_{IN} and 75 mV for V_{VDD} is also provided to prevent glitch.

7.3.4 Overcurrent Protection

The TPS53321 continuously monitors the current flowing through the high-side and the low-side MOSFETs. If the current through the high-side FET exceeds 6.5 A, the high-side FET turns off and the low-side FET turns on until the next PWM cycle. An overcurrent (OC) counter starts to increment each occurrence of an overcurrent event. The converter shuts down immediately when the OC counter reaches four. The OC counter resets if the detected current is less 6.5 A after an OC event.

Another set of overcurrent circuitry monitors the current flowing through low-side FET. If the current through the low-side FET exceeds 6.8 A, the overcurrent protection is enabled and immediately turns off both the high-side and the low-side FETs and shuts down the converter. The device is fully protected against overcurrent during both on-time and off-time. The device attempts to restart after a hiccup delay of 14.5 ms (typical). If the overcurrent condition clears before restart, the device starts up normally.

7.3.5 Overvoltage Protection

The TPS53321 monitors the voltage divided feedback voltage to detect overvoltage and undervoltage conditions. When the feedback voltage is greater than 117% of the reference, the high-side MOSFET turns off and the low-side MOSFET turns on. The output voltage then drops until it reaches the undervoltage threshold. At that point the low-side MOSFET turns off and the device enters a high-impedance state.

7.3.6 Undervoltage Protection

When the feedback voltage is lower than 83% of the reference voltage, the undervoltage protection timer starts. If the feedback voltage remains lower than the undervoltage threshold voltage after 10 µs, the device turns off both the high-side and the low-side MOSFETs and goes into a high-impedance state. The device attempts to restart after a hiccup delay of 14.5 ms (typical).

7.3.7 Overtemperature Protection

The TPS53321 continuously monitors the die temperature. If the die temperature exceeds the threshold value (140˚C typical), the device shuts off. When the device temperature falls to 40˚C below the overtemperature threshold, it restarts and returns to normal operation.

7.3.8 Output Discharge

When the enable pin is low, the TPS53321 discharges the output capacitors through an internal MOSFET switch between SW and PGND while high-side and low-side MOSFETs remain off. The typical discharge switch ON-resistance is 60 Ω. This function is disabled when V_{IN} is less than 1 V.

7.3.9 Master and Slave Operation and Synchronization

Two TPS53321 can operate interleaved when configured as master and slave. The SYNC pins of the two devices are connected together for synchronization. In CCM, the master device sends the 180° out-of-phase pulse to the slave device through the SYNC pin, which determines the leading edge of the PWM pulse. If the slave device does not receive the SYNC pulse from the master device or if the SYNC connection is broken during operation, the slave device continues to operate using its own internal clock.

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Feature Description (continued)

In DE mode, the master and slave switching node does not synchronize to each other if either one of them is operating in DCM. When both master and slave enter CCM, the switching nodes of the master and the slave synchronize to each other.

The SYNC pin of the slave device can also connect to external clock source within ±20% of the 1.1-MHz switching frequency. The falling edge of the SYNC triggers the rising edge of the PWM signal.

7.4 Device Functional Modes

7.4.1 Operation Modes

The TPS53321 offers five operation modes determined by the PS pin connections listed in Table 1.

Table 1. Operation Mode Selection

PS PIN CONNECTION	OPERATION MODE	AUTO-SKIP AT LIGHT LOAD	MASTER/SLAVE SUPPORT
GND	FCCM Slave	—	Slave
24.3 kΩ to GND	DE Slave	Yes	Slave
57.6 kΩ to GND	HEF Mode	Yes	—
174 kΩ to GND	DE Master	Yes	Master
Floating or pulled to VDD	FCCM Master	—	Master

In *forced continuous conduction* mode (FCCM), the high-side FET is ON during the on-time and the low-side FET is ON during the off-time. The switching is synchronized to the internal clock thus the switching frequency is fixed.

In *diode emulation* (DE) mode, the high-side FET is ON during the on-time and low-side FET is ON during the off-time until the inductor current reaches zero. An internal zero-crossing comparator detects the zero crossing of inductor current from positive to negative. When the inductor current reaches zero, the comparator sends a signal to the logic control and turns off the low-side FET.

When the load is increased, the inductor current is always positive and the zero-crossing comparator does not send a zero-crossing signal. The converter enters into *continuous conduction* mode (CCM) when no zero-crossing is detected for two consecutive PWM pulses. The switching synchronizes to the internal clock and the switching frequency is fixed.

In *high-efficiency* (HEF) mode, the operation is the same as DE mode at light load. However, the converter does not synchronize to the internal clock during CCM. Instead, the PWM modulator determines the switching frequency.

7.4.2 Eco-Mode™ Light-Load Operation

In skip modes (DE and HEF) when the load current is less than one-half of the inductor peak current, the inductor current becomes negative by the end of off-time. During light load operation, the low-side MOSFET is turned off when the inductor current reaches zero. The energy delivered to the load per switching cycle is increased compared to the normal PWM mode operation and the switching frequency is reduced. The switching loss is reduced, thereby improving efficiency.

In both DE and HEF mode, the switching frequency is reduced in discontinuous conduction mode (DCM). When the load current is 0 A, the minimum switching frequency is reached. The difference between V_{VBST} and V_{SW} must be maintained at a value higher than 2.4 V.

7.4.3 Forced Continuous Conduction Mode (FCCM)

When the PS pin is grounded or greater than 2.2 V, the TPS53321 is operating in *forced continuous conduction mode* in both light-load and heavy-load conditions. In this mode, the switching frequency remains constant over the entire load range, making it suitable for applications that require tight control of switching frequency at a cost of lower efficiency at light load.

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8 Application and Implementation

NOTE

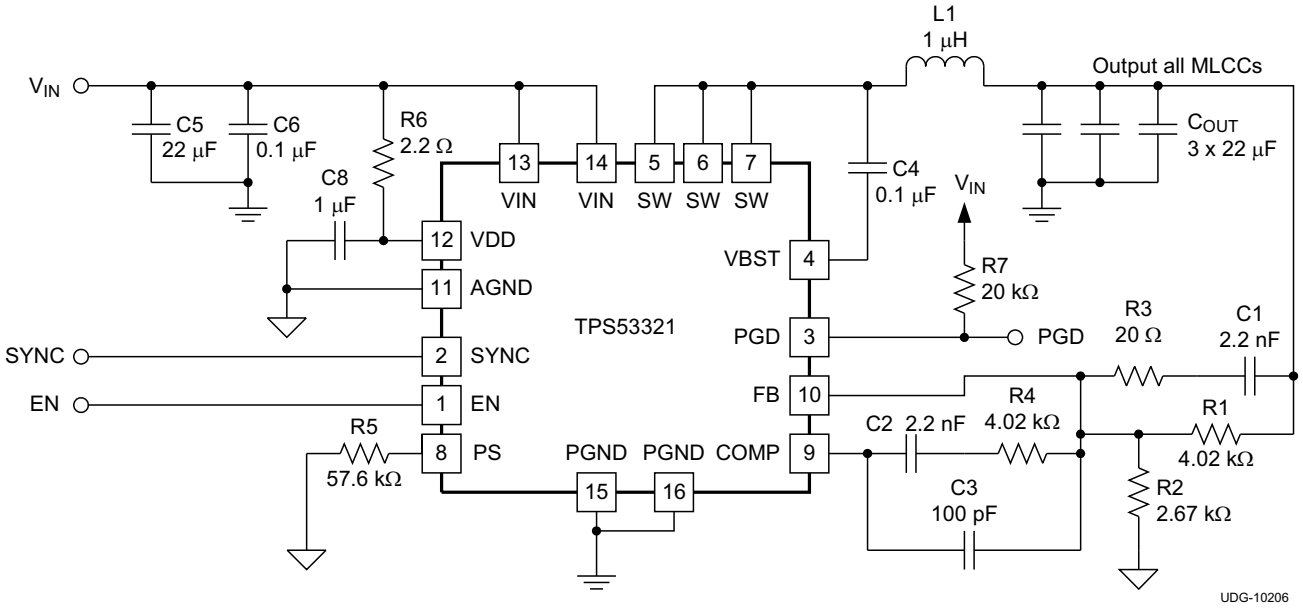
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS53321 device is a high-efficiency synchronous-buck converter. The device suits low output voltage point-of-load applications with 5-A or lower output current in computing and similar digital consumer applications.

8.2 Typical Application

This design example describes a voltage-mode, 5-A synchronous buck converter with integrated MOSFETs. The device provides a fixed 1.5-V output at up to 5 A from a 3.3-V input bus.



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Figure 13. Typical 3.3-V Input Application Circuit Diagram

8.2.1 Design Requirements

Table 2 lists the design specifications for this application example.

Table 2. TPS53321 Design Example Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
Input voltage, VIN	Vin	2.9	3.3	6	V
Maximum input current	Vin = 3.3 V,1.5 V/5 A		2.67		A
No load input current	Vin = 3.3 V,1.5 V/0 A		12.5		mA

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Typical Application (continued)

Table 2. TPS53321 Design Example Specifications (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS					
Output voltage, Vo		1.485	1.5	1.515	V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		1%		
Output voltage ripple	Vin = 3.3 V, 1.5 V/0 A to 5 A			20	mVpp
Output load current		0		5	A
Output over current			6.5		A
OUTPUT CHARACTERISTICS					
Switching frequency	Fixed		1.1		MHz
1.5-V full load efficiency	Vin = 3.3 V, 1.5 V/5 A		85.94%		
	Vin = 5 V, 1.5 V/5 A		87%		
Operating temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 Determine the Value of R1 and R2

The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in Figure 13. R1 is connected between the FB pin and the output, and R2 is connected between the FB pin and GND. The recommended value for R1 is from 1 kΩ to 5 kΩ. Determine R2 using equation in Equation 1.

$$R2 = \frac{0.6}{V_{OUT} - 0.6} \times R1 \tag{1}$$

8.2.2.2 Choose the Inductor

The inductance value must be determined to give the ripple current of approximately 20% to 40% of maximum output current. The inductor ripple current is determined by Equation 2.

$$I_{L(ripple)} = \frac{1}{L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \tag{2}$$

The inductor also requires low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation.

8.2.2.3 Choose the Output Capacitor(s)

The output capacitor selection is determined by output ripple and transient requirement. When operating in CC mode, the output ripple has three components calculated with Equation 3 through Equation 6.

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} \tag{3}$$

$$V_{RIPPLE(C)} = \frac{I_{L(ripple)}}{8 \times C_{OUT} \times f_{SW}} \tag{4}$$

$$V_{RIPPLE(ESR)} = I_{L(ripple)} \times ESR \tag{5}$$

$$V_{RIPPLE(ESL)} = \frac{V_{IN} \times ESL}{L} \tag{6}$$

When ceramic output capacitors are used, the ESL component is usually negligible. In the case when multiple output capacitors are used, ESR and ESL must be the equivalent of ESR and ESL of all the output capacitor in parallel.

When operating in DCM, the output ripple is dominated by the component determined by capacitance. It also varies with load current and can be expressed as shown in Equation 7.

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$$V_{RIPPLE(DCM)} = \frac{\left(\alpha \times I_{L(ripple)} - I_{OUT}\right)^2}{2 \times C_{OUT} \times f_{SW} \times I_{L(ripple)}}$$

where

- α is the DCM on-time coefficient and can be expressed in Equation 8 (typical value 1.25) (7)

$$\alpha = \frac{t_{ON(DCM)}}{t_{ON(CCM)}} \quad (8)$$

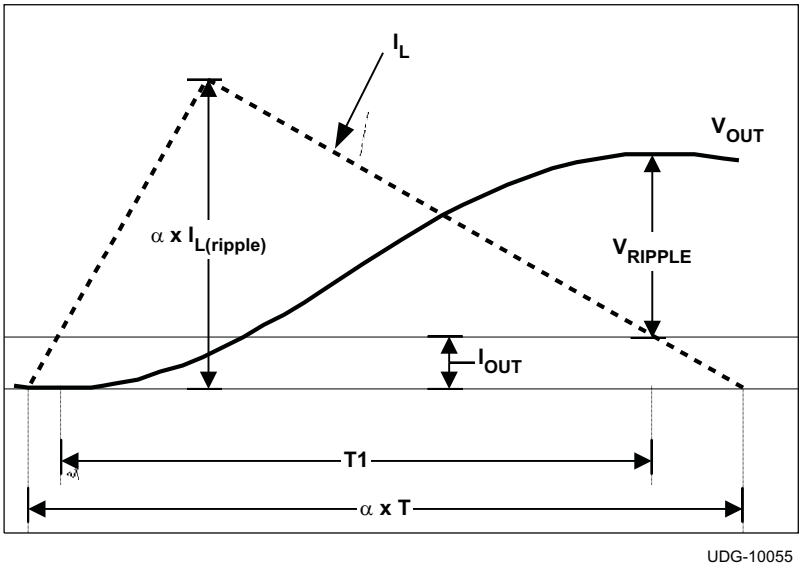


Figure 14. DCM V_{OUT} Ripple Calculation

8.2.2.4 Choose the Input Capacitor

The selection of input capacitor must be determined by the ripple current requirement. The ripple current generated by the converter must be absorbed by the input capacitors as well as the input source. The RMS ripple current from the converter can be expressed in Equation 9.

$$I_{IN(ripple)} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

where

- D is the duty cycle and can be expressed as shown in Equation 10 (9)

$$D = \frac{V_{OUT}}{V_{IN}} \quad (10)$$

To minimize the ripple current drawn from the input source, sufficient input decoupling capacitors must be placed close to the device. The ceramic capacitor is recommended because it provides low ESR and low ESL. The input voltage ripple can be calculated as shown in Equation 11 when the total input capacitance is determined.

$$V_{IN(ripple)} = \frac{I_{OUT} \times D}{f_{SW} \times C_{IN}} \quad (11)$$

8.2.2.5 Compensation Design

The TPS53321 uses voltage mode control. To effectively compensate the power stage and ensure fast transient response, Type III compensation is typically used.

The control to output transfer function can be described in Equation 12.

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$$G_{CO} = 4 \times \frac{1 + s \times C_{OUT} \times ESR}{1 + s \times \left(\frac{L}{DCR + R_{LOAD}} + C_{OUT} \times (ESR + DCR) \right) + s^2 \times L \times C_{OUT}} \quad (12)$$

The output L-C filter introduces a double pole which can be calculated as shown in Equation 13.

$$f_{DP} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}} \quad (13)$$

The ESR zero can be calculated as shown in Equation 14.

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \quad (14)$$

Figure 15 and Figure 16 show the configuration of Type III compensation and typical pole and zero locations. Equation 16 through Equation 20 describe the compensator transfer function and poles and zeros of the Type III network.

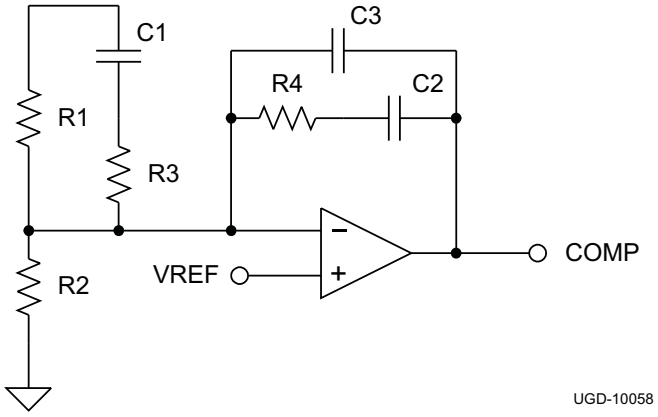


Figure 15. Type III Compensation Network Configuration Schematic

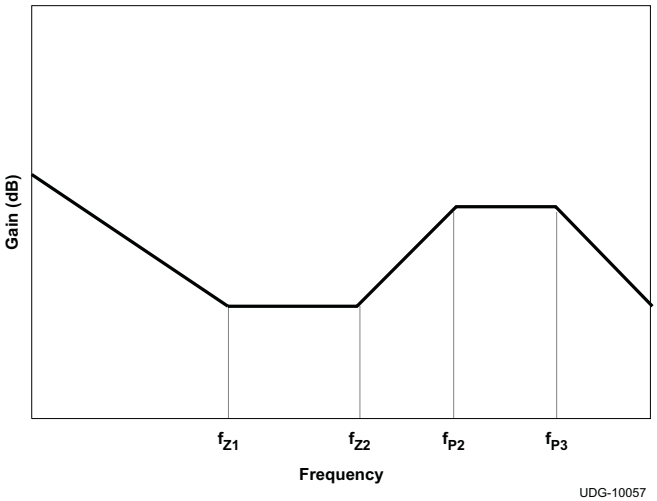


Figure 16. Type III Compensation Gain Plot and Zero/Pole Placement

$$G_{EA} = \frac{(1 + s \times C_1 \times (R_1 + R_3))(1 + s \times R_4 \times C_2)}{(s \times R_1 \times (C_2 + C_3)) \times (1 + s \times C_1 \times R_3) \times \left(1 + s \times R_4 \frac{C_2 \times C_3}{C_2 + C_3}\right)} \quad (15)$$

$$f_{Z1} = \frac{1}{2 \times \pi \times R_4 \times C_2} \quad (16)$$

$$f_{Z2} = \frac{1}{2 \times \pi \times (R_1 + R_3) \times C_1} \cong \frac{1}{2 \times \pi \times R_1 \times C_1} \quad (17)$$

$$f_{P1} = 0 \quad (18)$$

$$f_{P2} = \frac{1}{2 \times \pi \times R_3 \times C_1} \quad (19)$$

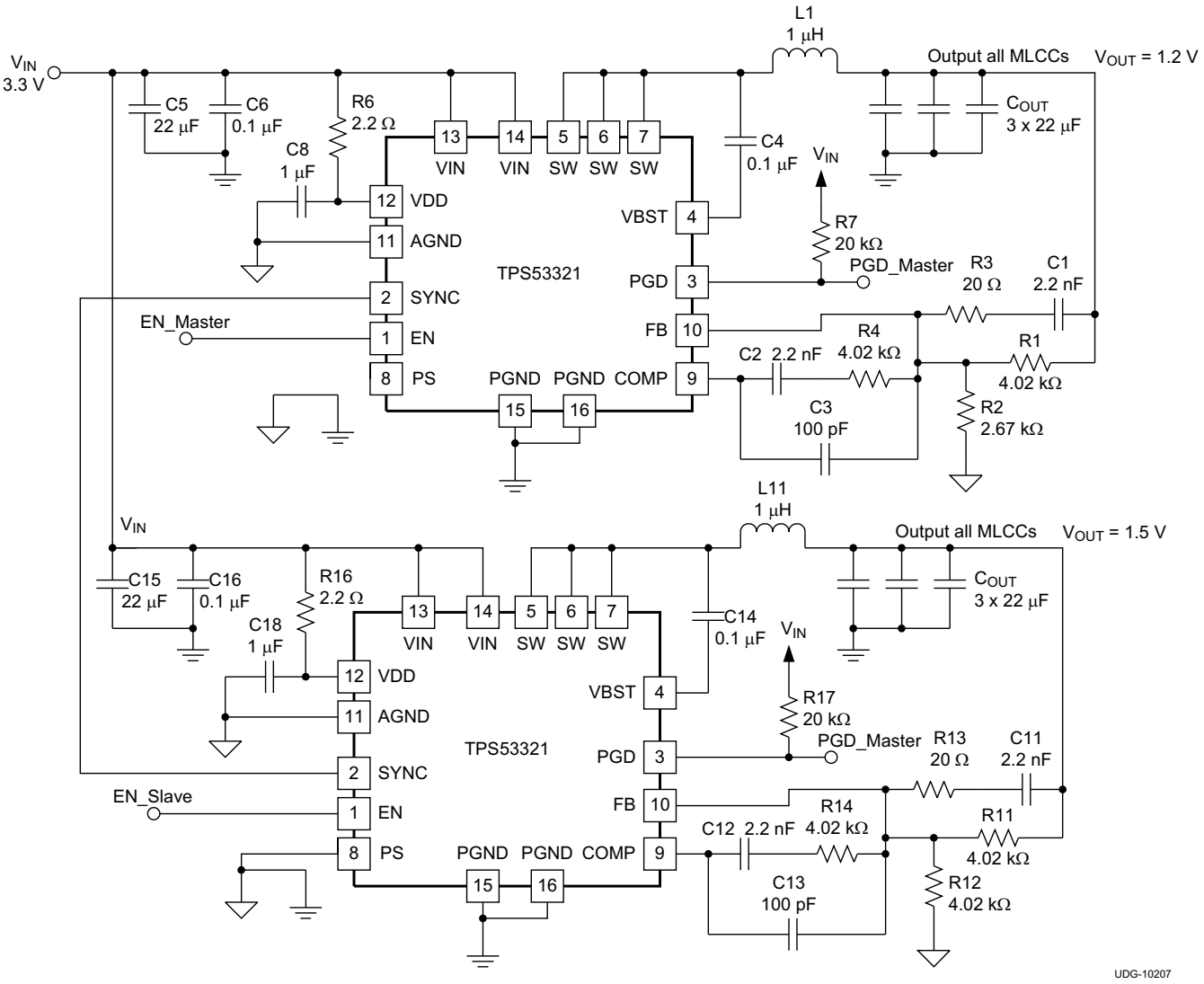
$$f_{P3} = \frac{1}{2 \times \pi \times R_4 \times \left(\frac{C_2 \times C_3}{C_2 + C_3}\right)} \cong \frac{1}{2 \times \pi \times R_4 \times C_3} \quad (20)$$

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The two zeros can be placed near the double pole frequency to cancel the response from the double pole. One pole can be used to cancel ESR zero, and the other non-zero pole can be placed at half switching frequency to attenuate the high frequency noise and switching ripple. Suitable values can be selected to achieve a compromise between high phase margin and fast response. A phase margin higher than 45 degrees is required for stable operation.

For DCM operation, a C3 between 56 pF and 150 pF is recommended for output capacitance between 20 µF to 200 µF.

Figure 17 shows the master and slave configuration schematic for a design with a 3.3-V input.



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Figure 17. Master and Slave Configuration Schematic

8.2.3 Application Curves

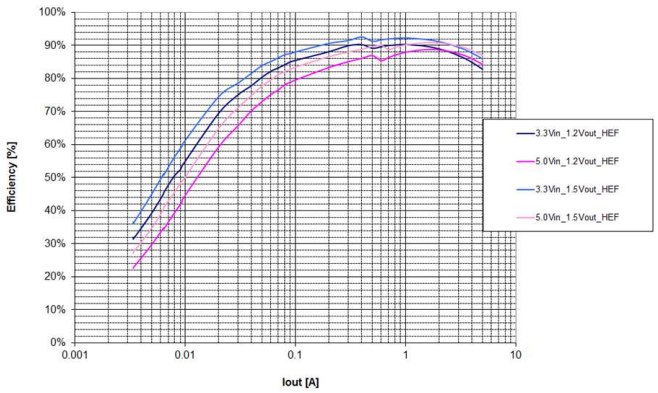


Figure 18. Efficiency

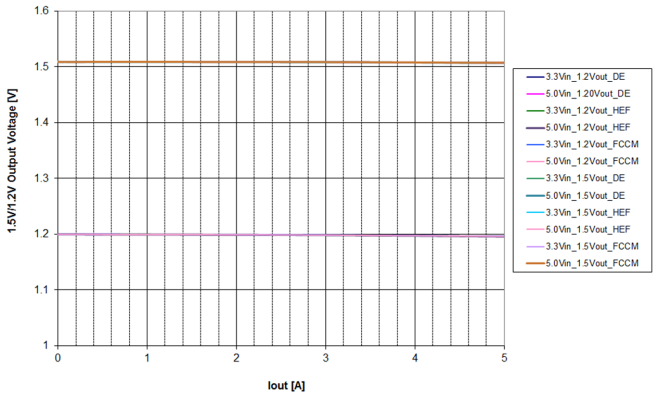


Figure 19. Load Regulation

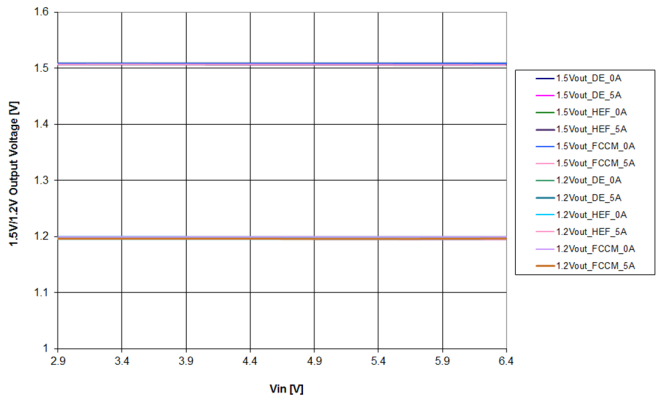


Figure 20. Line Regulation

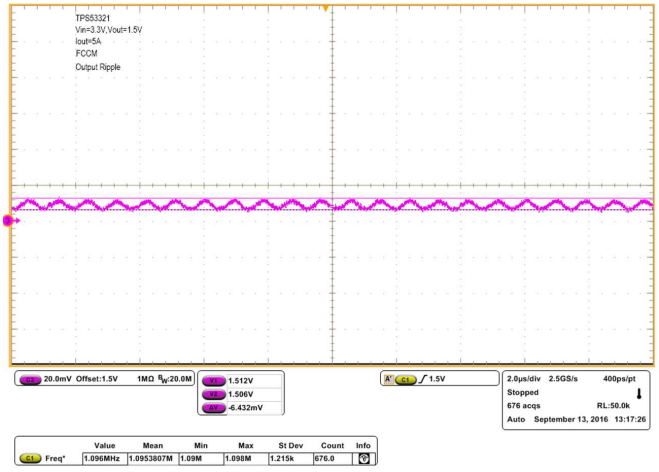


Figure 21. 1.5-V Output Ripple

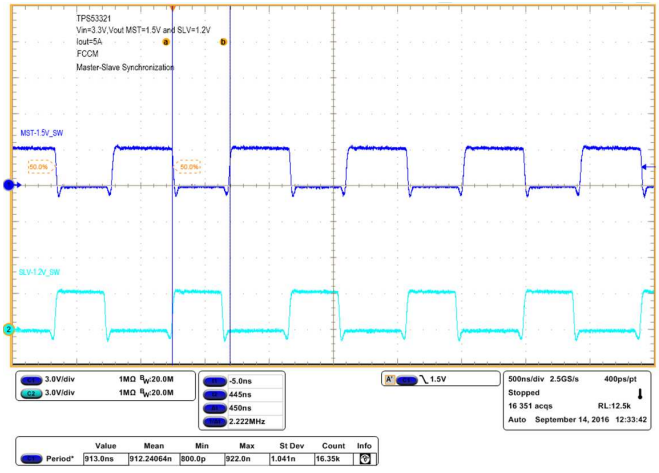


Figure 22. Master-Slave 180° Synchronization

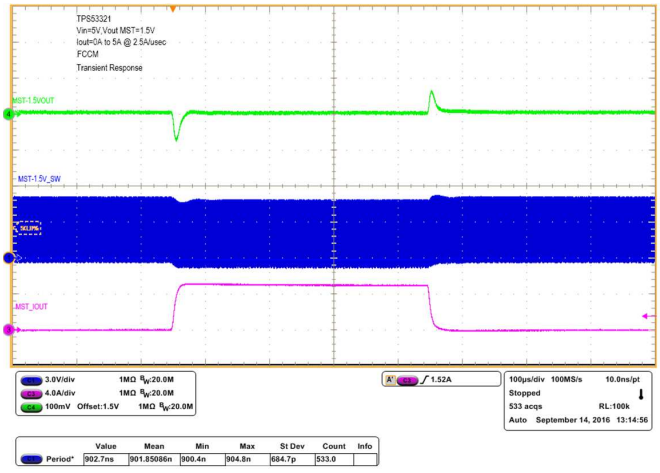


Figure 23. 1.5-V Output Transient

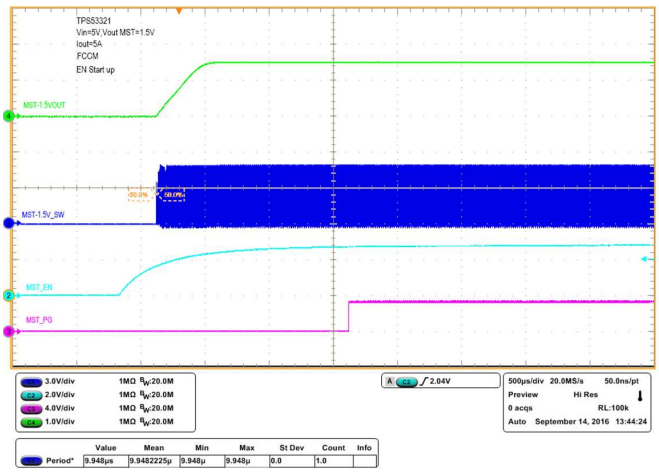


Figure 24. 1.5-V Turnon Waveform

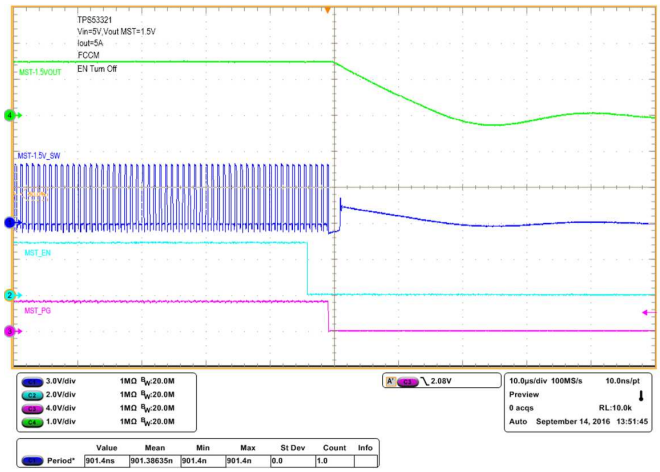


Figure 25. 1.5-V Turnoff Waveform

9 Power Supply Recommendations

The TPS53321 devices are designed to operate from an input voltage supply range between 2.9 V and 6 V (2.9 V to 3.5 V biased). This input supply must be well regulated. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in *Layout*.

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10 Layout

10.1 Layout Guidelines

Good layout is essential for stable power supply operation. Follow these guidelines for a clean PCB layout:

- Separate the power ground and analog ground planes. Connect them together at one location.
- Use four vias to connect the thermal pad to power ground.
- Place VIN and VDD decoupling capacitors as close to the device as possible.
- Use wide traces for V_{IN}, V_{OUT}, PGND, and SW. These nodes carry high current and also serve as heat sinks.
- Place feedback and compensation components as close to the device as possible.
- Keep analog signals (FB, COMP) away from noisy signals (SW, SYNC, VBST).
- See TPS53321 evaluation module for a layout example.

Figure 26 shows and example layout for the TPS53321.

10.2 Layout Example

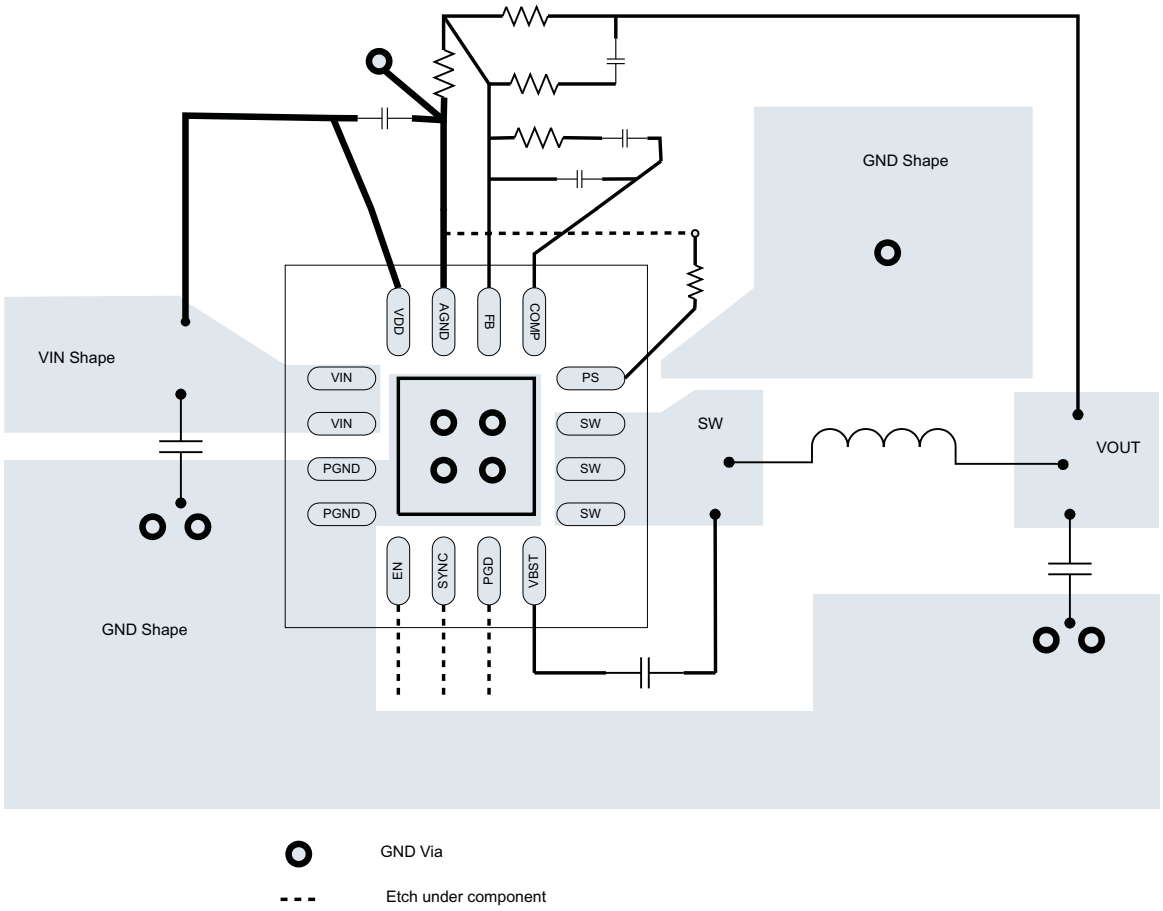


Figure 26. TPS53321 Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

SmoothPWM, Eco-Mode, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53321RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3321	Samples
TPS53321RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3321	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

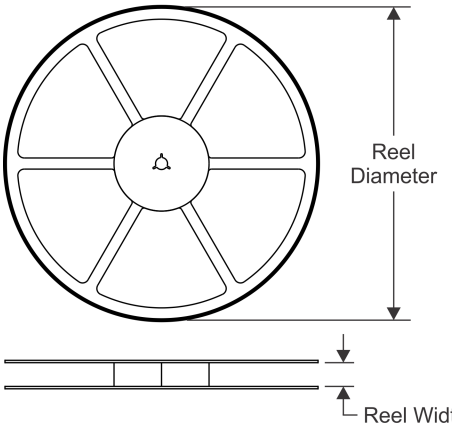
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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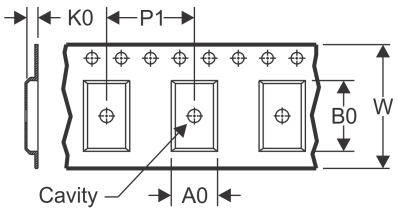
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

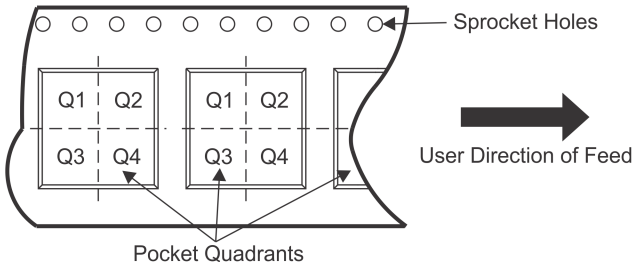


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

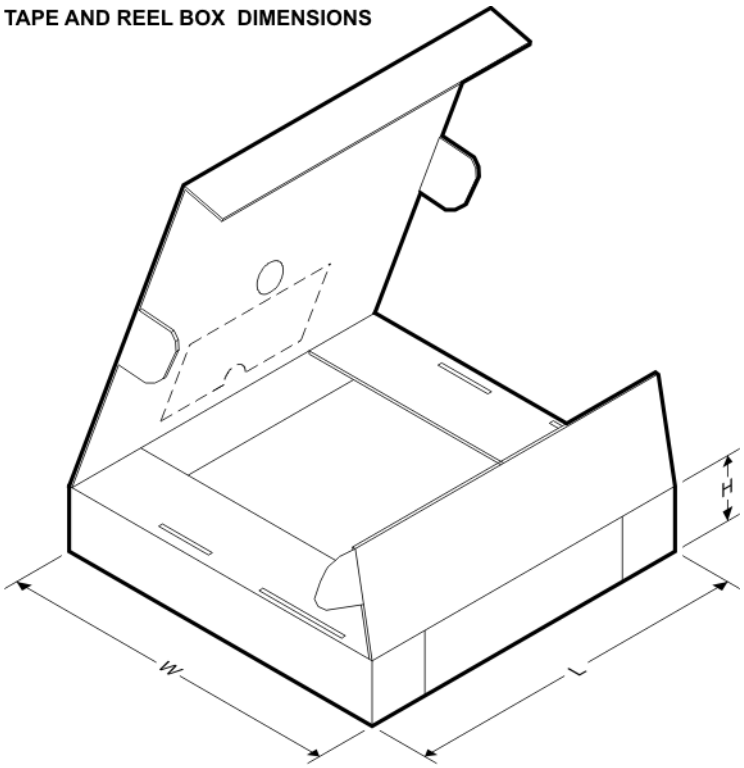
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53321RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS53321RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

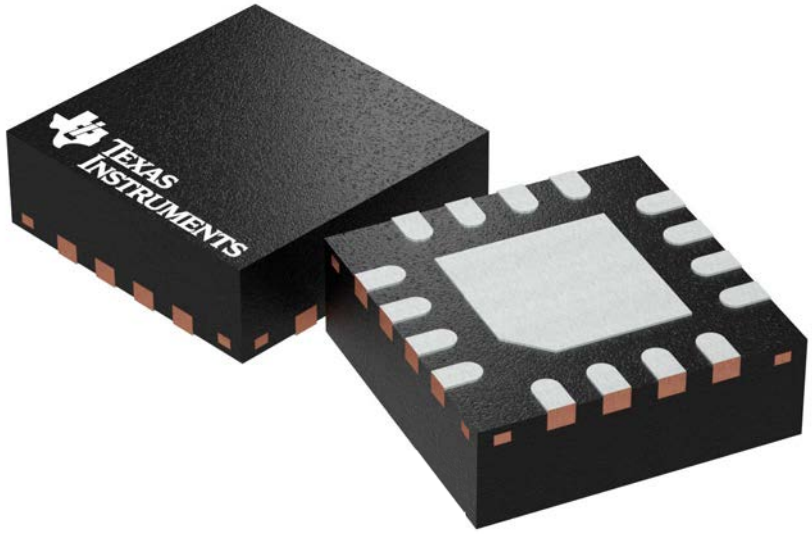


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53321RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS53321RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

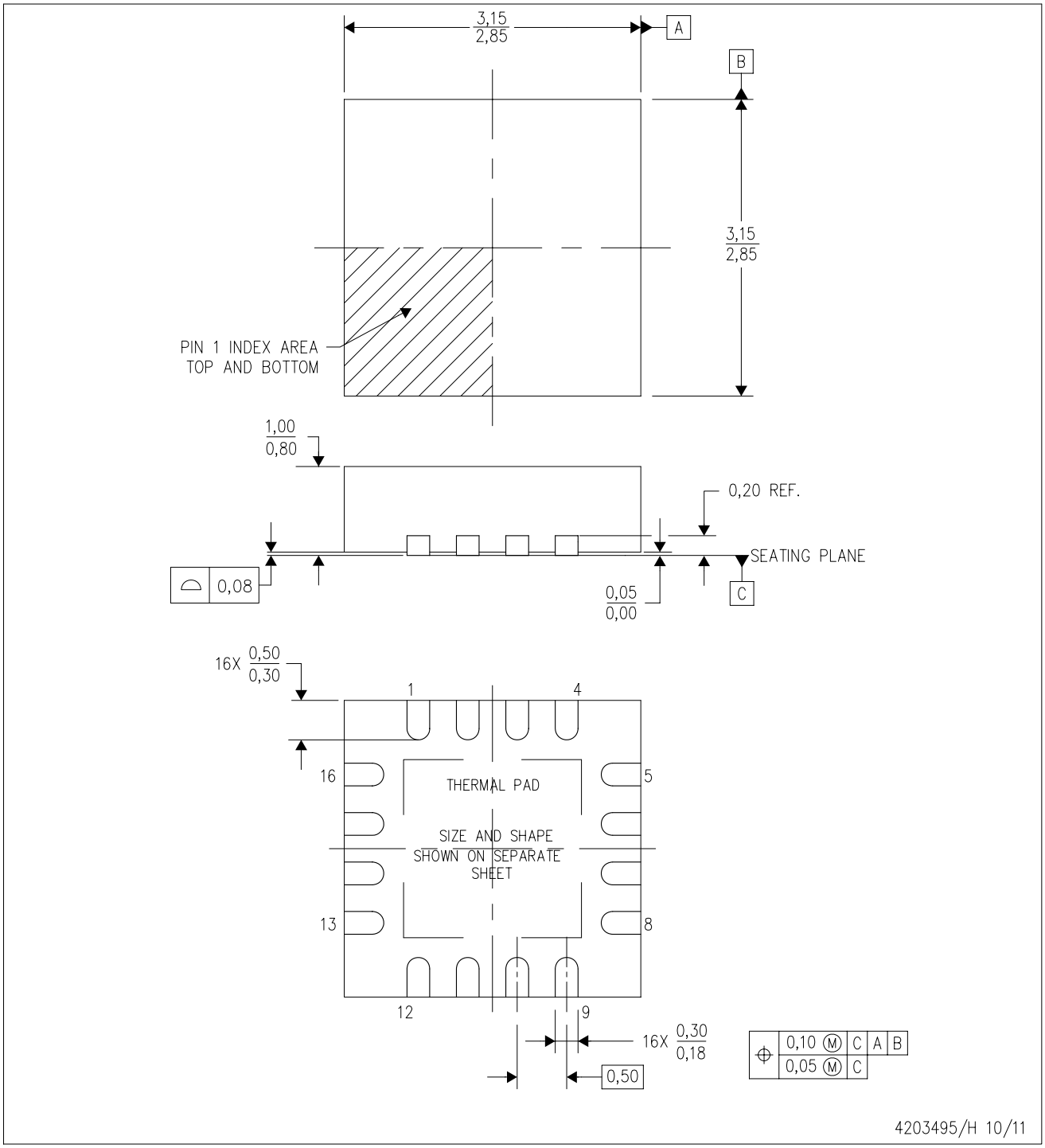
RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

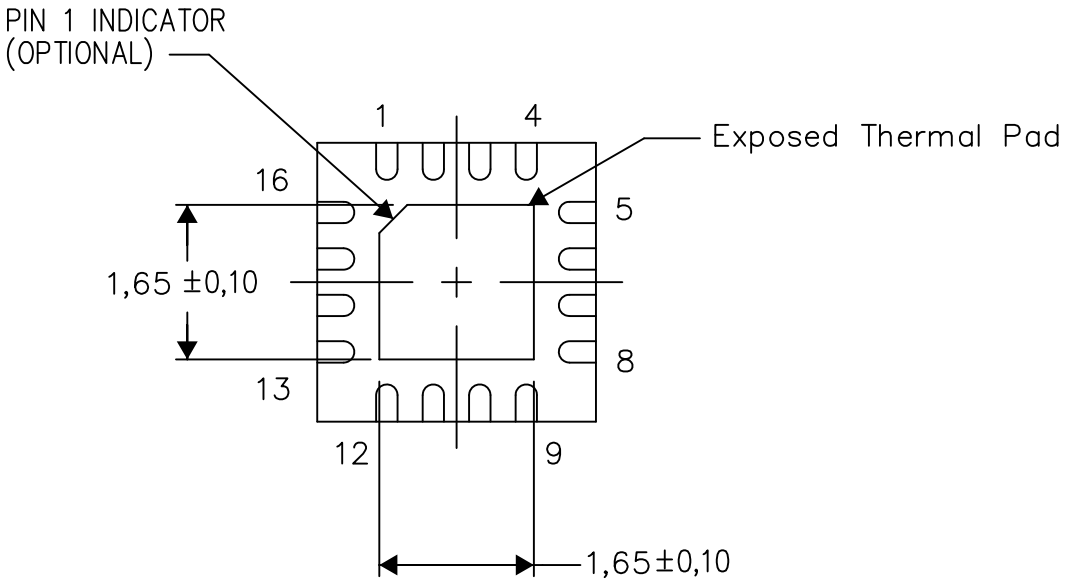
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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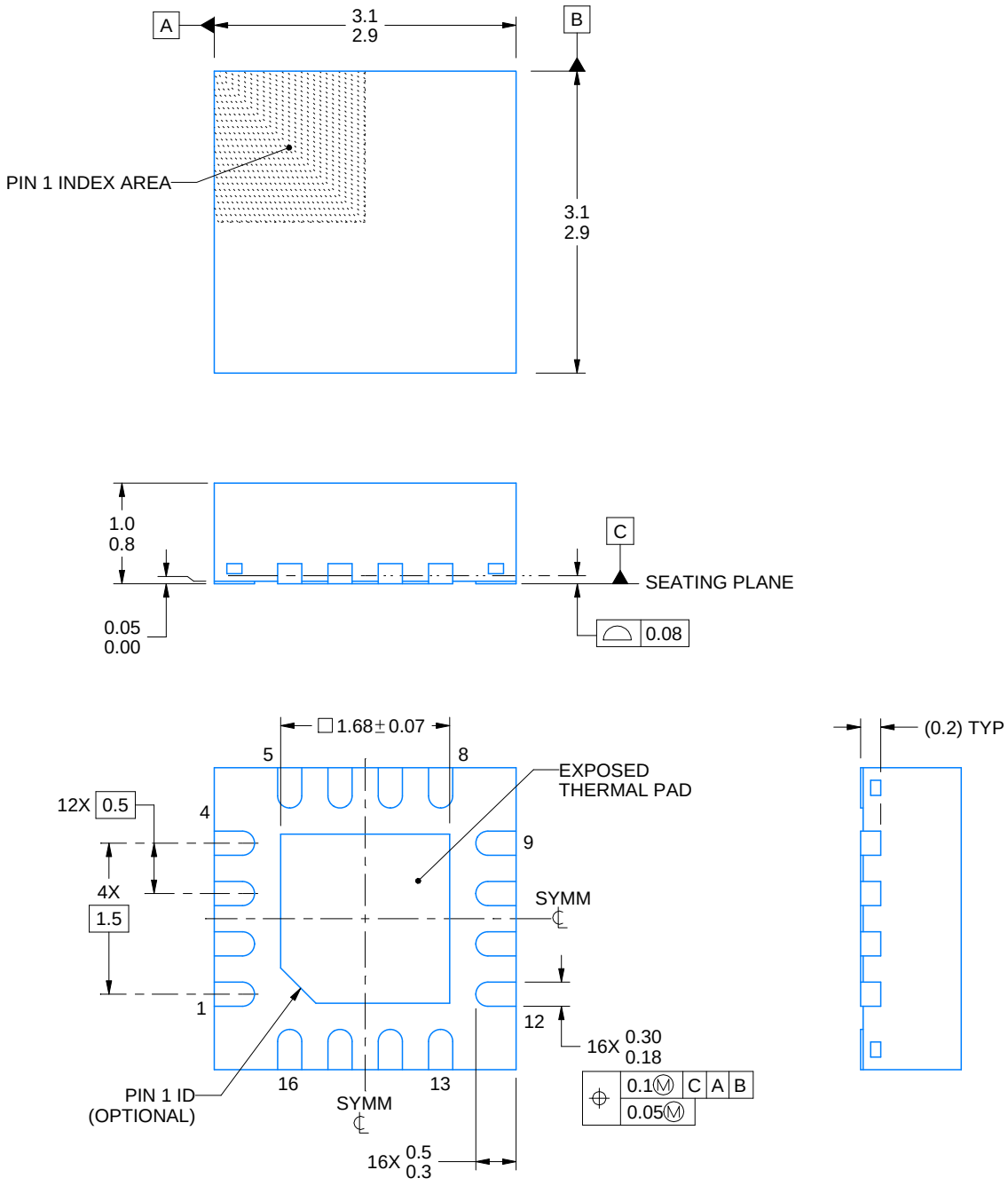
NOTE: All linear dimensions are in millimeters

RGT0016C

PACKAGE OUTLINE

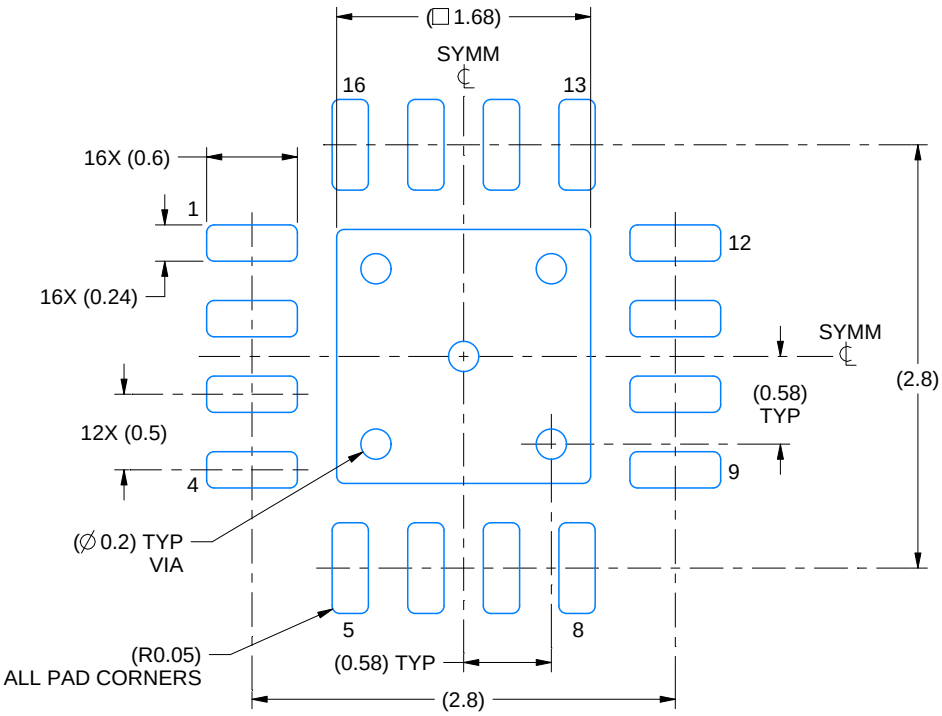
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

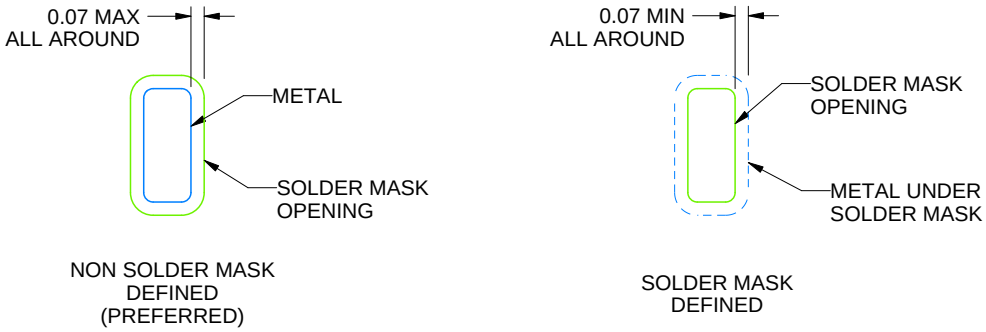


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

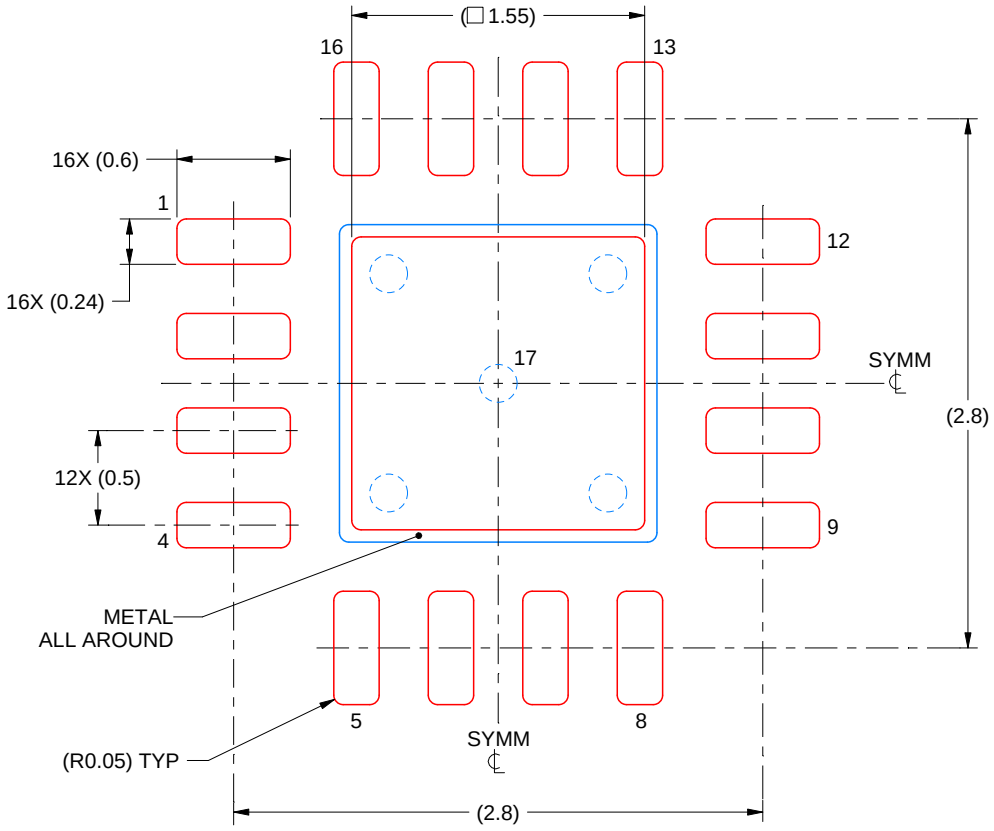


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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