4.5-V 至 14-V 输入大电流同步降压转换器

查询样品: TPS56121

特性

- **4.5-V** 至 **14-V** 输入电压范围
- 整合功率块技术
- 输出电流高达 **15 A**
- **300 kHz**、**500 kHz** 与 **1 MHz** 固定频率选项
- 高侧与低侧 **MOSFET $R_{DS(on)}$** 传感
- 可编程软启动
- 误差精度为 **1%** 的 **600 mV** 参考电压
- 前馈电压模式控制
- 支持预偏置输出
- 热关断
- **22** 引脚 **5** 毫米 **x 6** 毫米 **PQFN PowerPAD™** 封装

应用范围

- 负载点 **(POL)** 电源模块
- 针对电信与网络应用的高密度 **DC-DC** 转换器

说明

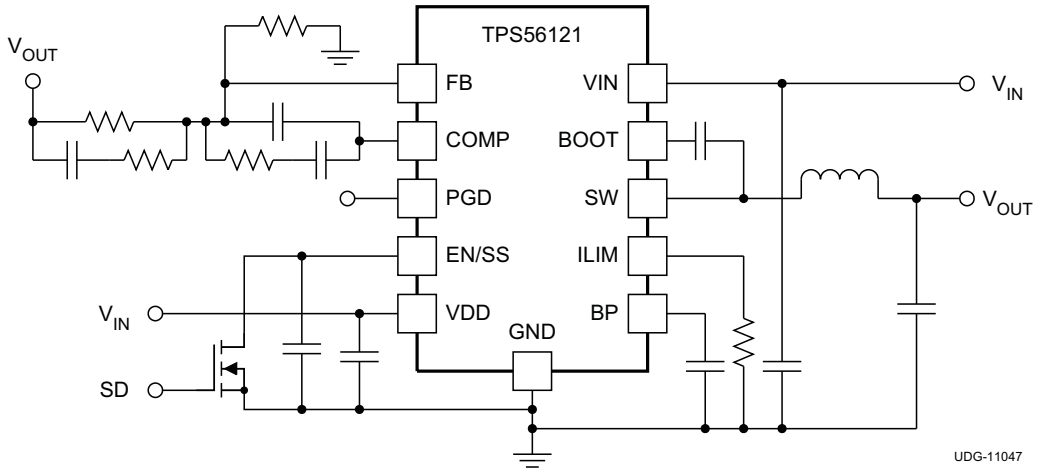
TPS56121 是一款工作电源电压在 4.5 V 与14 V 之间的高效率大电流同步降压转换器。该器件可在高达 15 A 的负载下产生低至 0.6 V 的输出电压。 集成型 NexFET™ 功率 MOSFET 可带来小型化与易用性优势。

该器件可通过电压前馈补偿实施电压模式控制，能够在输入电压变化时立即做出响应。

TPS56121 采用热增强型 22-引 PQFN (DQP) PowerPAD™ 封装。

该器件支持高度的设计灵活性，可提供各种用户可编程功能，其中包括软启动、过流保护 (OCP) 级以及环路补偿。 OCP 级可通过由 ILIM 引脚连接至电路接地的单个外部电阻器进行编程。 在初始上电排序过程中，该器件可进入校准环节，测量 ILIM 引脚电压，并设置内部I OCP 电压级。 在工作中，可在通电时通过将可编程 OCP 电压级与整个低侧 FET 的电压压降进行比较来判断是否为过流状况。 然后，其可在消除故障后进入关断 / 重启环节。

SIMPLIFIED APPLICATION



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE	PINS	TRANSPORT MEDIA	MINIMUM QUANTITY	ORDERABLE NUMBER
-40°C to 150°C	Plastic QFN (DQP)	22	Tape-and-reel	250	TPS56121DQPT
				2500	TPS56121DQPR

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE		UNIT
		MIN	TYP	
Voltage Range	VDD, VIN	–0.3	16.5	V
	SW	–3	25	
	SW (< 100 ns pulse width, 10 µJ)	-5		
	BOOT	–0.3	30	
	BOOT-SW (differential from BOOT to SW)	–0.3	7	
	COMP, PGOOD, FB, BP, EN/SS, ILIM	–0.3	7	
Electrostatic discharge	(HBM) QSS 009-105 (JESD22-A114A)		2	kV
	(CBM) QSS 009-147 (JESD22-C101B.01)		1.5	
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those included under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods of time may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS56121 PQFN 22 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	34.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	22.9	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	5.0	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{DD}	VIN Input voltage	4.5		14	V
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

–40°C ≤ T_J ≤ 125°C, V_{VDD} = 12 V, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE REFERENCE						
V_{FB}	FB input voltage	T_J = 25°C, 4.5 V ≤ V_{VDD} ≤ 14 V	597	600	603	mV
		–40°C ≤ T_J ≤ 125°C, 4.5 V ≤ V_{VDD} ≤ 14 V	594	600	606	
INPUT SUPPLY						
V_{VDD}	Input supply voltage range		4.5		14	V
$IVDD_{SD}$	Shutdown supply current	$V_{EN/SS}$ = 0.2 V		80	120	µA
$IVDD_Q$	Quiescent, non-switching	Let EN/SS float, V_{FB} = 1 V		2.5	5.0	mA
V_{UVLO}	UVLO ON Voltage		4.0		4.3	V
$V_{UVLO(HYS)}$	UVLO hysteresis		500		700	mV
ENABLE/SOFT-START						
V_{IH}	High-level input voltage, EN/SS		0.55	0.70	1.00	V
V_{IL}	Low-level input voltage, EN/SS		0.27	0.30	0.33	V
I_{SS}	Soft-start source current		8	10	12	µA
V_{SS}	Soft-start voltage level – Start of ramp		0.4	0.8	1.3	V
BP REGULATOR						
V_{BP}	Output voltage	I_{BP} = 10 mA	6.2	6.5	6.8	V
V_{DO}	Regulator dropout voltage, V_{VDD} – V_{BP}	I_{BP} = 25 mA, V_{VDD} = 4.5 V		70	125	mV
OSCILLATOR						
f_{SW}	Switching Frequency	R_{COMP} = 40.2 kΩ, 4.5 V ≤ V_{VDD} ≤ 14 V	270	300	330	kHz
		R_{COMP} = open, 4.5 V ≤ V_{VDD} ≤ 14 V	450	500	550	kHz
		R_{COMP} = 13.3 kΩ, 4.5 V ≤ V_{VDD} ≤ 14 V	0.8	0.95	1.1	MHz
V_{RAMP} (1)	Ramp amplitude		V_{VDD}/6.6	V_{VDD}/6	V_{VDD}/5.4	V
PWM						
D_{MAX} (1)	Maximum duty cycle	f_{sw} = 300 kHz, V_{FB} = 0 V, 4.5 V ≤ V_{VDD} ≤ 14 V	93%			
		f_{sw} = 500 kHz, V_{FB} = 0 V, 4.5 V ≤ V_{VDD} ≤ 14 V	90%			
		f_{sw} = 1 MHz, V_{FB} = 0 V, 4.5 V ≤ V_{VDD} ≤ 14 V	85%			
$t_{ON(min)}$ (1)	Minimum controllable pulse width				100	ns
ERROR AMPLIFIER						
GBWP (1)	Gain bandwidth product		10	24		MHz
A_OL (1)	Open loop gain		60			dB
I_{IB}	Input bias current (current out of FB pin)	V_{FB} = 0.6 V			75	nA
I_{EAOP}	Output source current	V_{FB} = 0 V	1.5			mA
I_{EAOM}	Output sink current	V_{FB} = 1 V	1.5			mA

(1) Ensured by design. Not production tested

ELECTRICAL CHARACTERISTICS (continued)

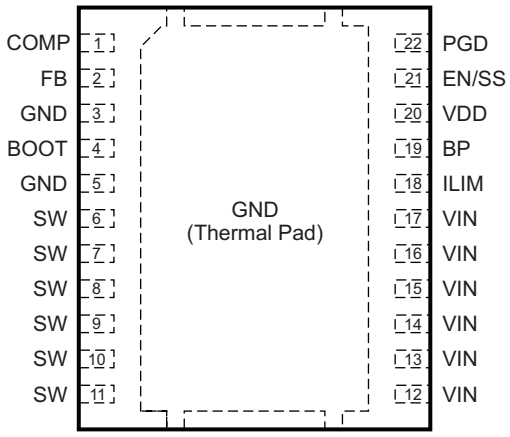
–40°C ≤ T_J ≤ 125°C, V_{VDD} = 12 V, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER GOOD						
V_{OV}	Feedback upper voltage limit for PGOOD		655	675	700	mV
V_{UV}	Feedback lower voltage limit for PGOOD		500	525	550	
$V_{PGD-HYST}$	PGOOD hysteresis voltage at FB			30	45	
R_{PGD}	PGOOD pull down resistance	V_{FB} = 0 V, I_{FB} = 5 mA		30	70	Ω
I_{PGDLK}	PGOOD leakage current	550 mV < V_{FB} < 655 mV, V_{PGOOD} = 5 V		10	20	µA
OUTPUT STAGE						
R_{HI}	High-side device resistance	T_J = 25°C, (V_{BOOT} – V_{SW}) = 5.5 V		4.5	6.5	mΩ
R_{LO}	Low side device resistance	T_J = 25°C		1.9	2.7	
OVERCURRENT PROTECTION (OCP)						
$t_{PSSC(min)}$ (2)	Minimum pulse time during short circuit			250		ns
t_{BLNKH} (2)	Switch leading-edge blanking pulse time (high-side detection)			150		
I_{OCH}	OC threshold for high-side FET	T_J = 25°C, (V_{BOOT} – V_{SW}) = 5.5 V	27	34	39	A
I_{ILIM}	ILIM current source	T_J = 25°C		10.0		µA
V_{OCLPRO} (2)	Programmable OC range for low side FET	T_J = 25°C	12		100	mV
t_{OFF}	OC retry cycles on EN/SS pin			4		Cycle
BOOT DIODE						
V_{DFWD}	Bootstrap diode forward voltage	I_{BOOT} = 5 mA		0.8		V
THERMAL SHUTDOWN						
T_{JSD} (2)	Junction shutdown temperature			145		ºC
T_{JSDH} (2)	Hysteresis			20		ºC

(2) Ensured by design. Not production tested

DEVICE INFORMATION

DQP PACKAGE
PQFN-22
(TOP VIEW)



Note: The thermal pad is also an electrical ground connection.

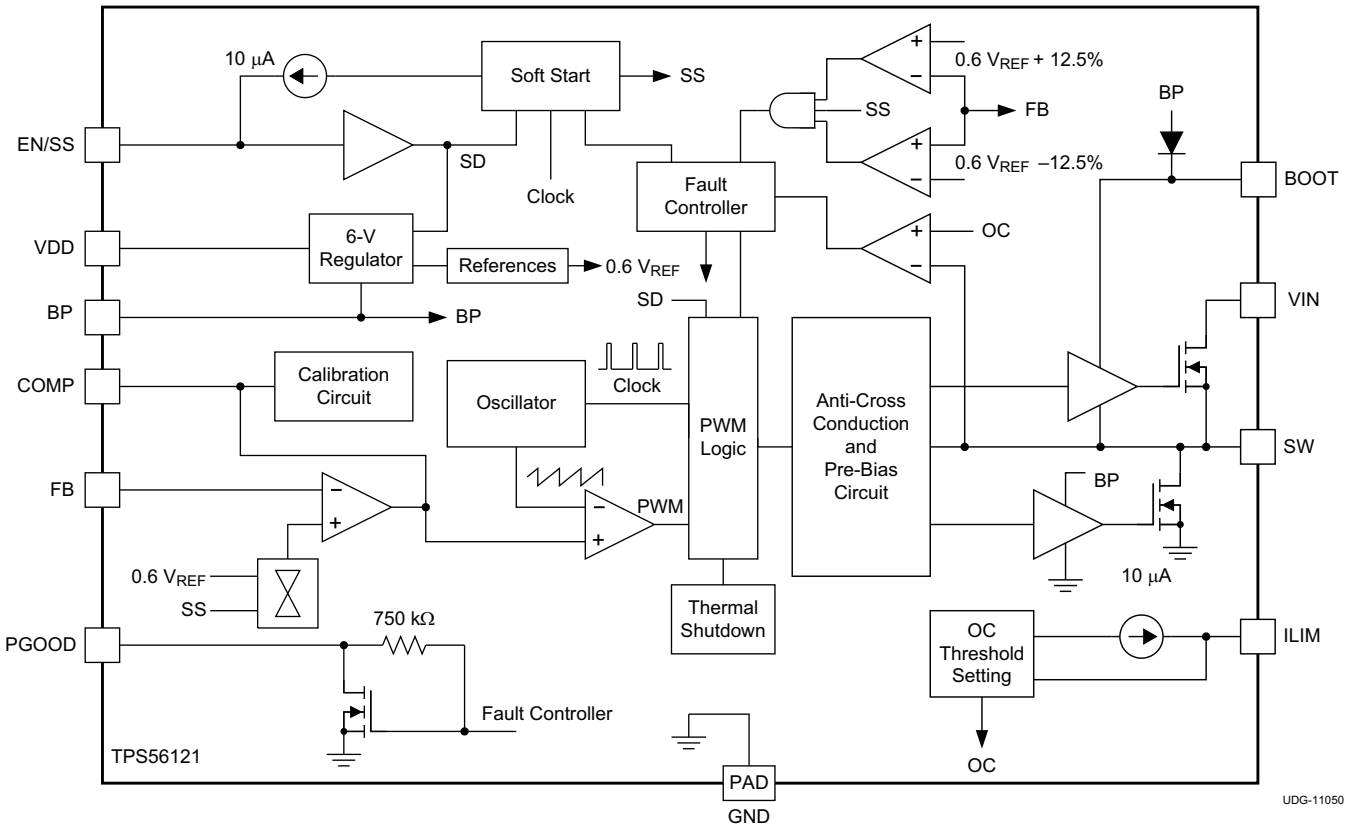
PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	4	O	Gate drive voltage for the high-side FET. A 100-nF capacitor (typical) must be connected between this pin and the SW pin. To reduce a voltage spike at SW, a BOOT resistor with a value between 5 Ω to 10 Ω may be placed in series with the BOOT capacitor to slow down turn-on of the high-side FET.
BP	19	O	Output bypass for the internal regulator. Connect a low-ESR bypass ceramic capacitor of 1 µF or greater from this pin to GND.
COMP	1	O	Output of the error amplifier and connection node for loop feedback components. Optionally, a 40.2 kΩ resistor from this pin to GND sets switching frequency to 300KHz instead of the default value of 500KHz; while a 13.3 kΩ resistor from this pin to GND sets switching frequency to 1 MHz.
EN/SS	21	I	Logic-level input starts or stops the controller via an external user command. Allowing this pin to float turns the controller on. Pulling this pin low disables the controller. This is also the soft-start programming pin. A capacitor connected from this pin to GND programs the soft-start time. The capacitor is charged with an internal current source of 10 µA. The resulting voltage ramp of this pin is also used as a second non-inverting input to the error amplifier after a 0.8 V (typical) level shift downwards. Output regulation is controlled by the internal level shifted voltage ramp until that voltage reaches the internal reference voltage of 600 mV. The voltage ramp of this pin reaches 1.4 V (typical).
FB	2	I	Inverting input to the error amplifier. In normal operation, the voltage on this pin is equal to the internal reference voltage.
GND	3	–	Ground reference for the device
	5		
GND	Thermal Pad	–	Ground reference for the device. This is also the thermal pad used to conduct heat from the device. This connection serves two purposes. The first is to provide an electrical ground connection for the device. The second is to provide a low thermal impedance path from the device die to the PCB. This pad should be tied externally to a ground plane.
ILIM	18	I	A resistor connected from this pin to GND sets the overcurrent threshold for the device (the low-side FET).
PGD	22	O	Open drain power good output.
SW	6	I	Switching node of the power conversion stage. Sense line for the adaptive anti-cross conduction circuitry. Acts as the common connection for the flying high-side FET driver.
	7		
	8		
	9		
	10		
	11		
VDD	20	I	Power input to the controller. A low-ESR bypass ceramic capacitor of 1 µF should be connected from this pin close to GND.

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	12	I	Power input to the high-side FET.
	13		
	14		
	15		
	16		
	17		

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

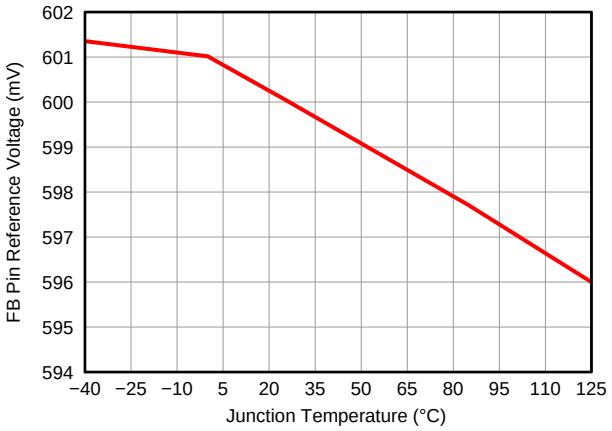


Figure 1. Reference Voltage vs. Junction Temperature

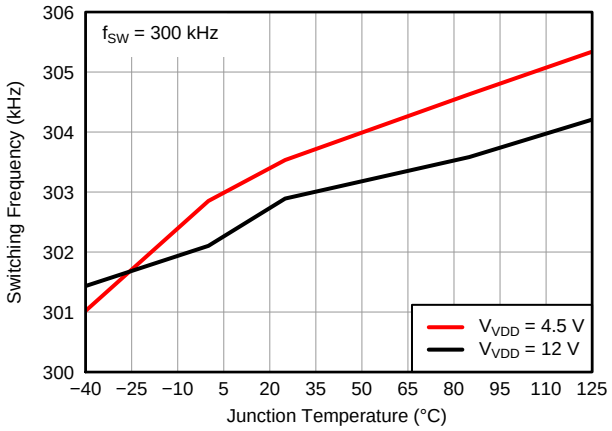


Figure 2. Switching Frequency vs. Junction Temperature (300 kHz)

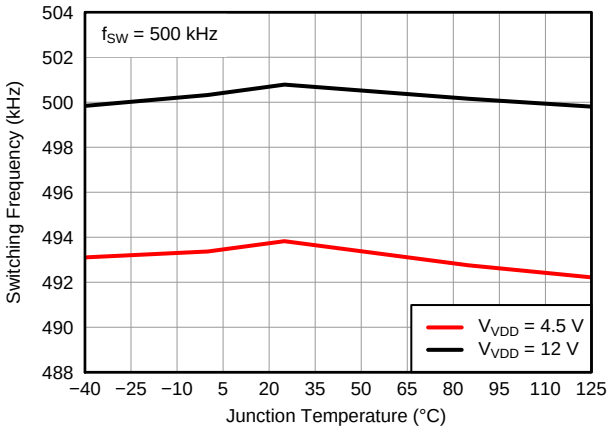


Figure 3. Switching Frequency vs. Junction Temperature (500 kHz)

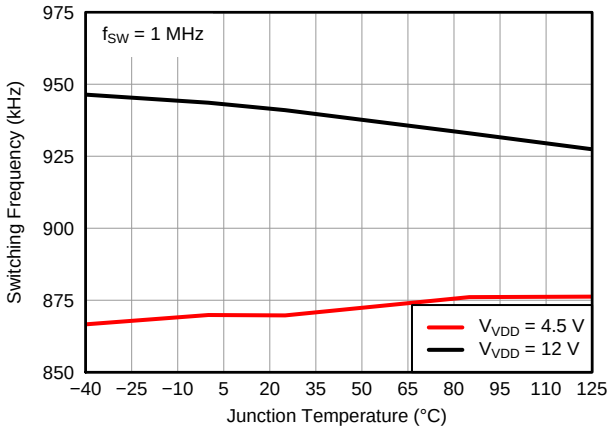


Figure 4. Switching Frequency vs. Junction Temperature (1 MHz)

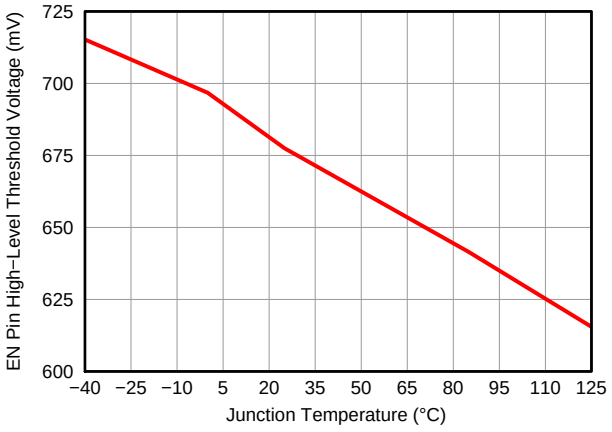


Figure 5. EN Pin High-Level Threshold Voltage vs. Junction Temperature

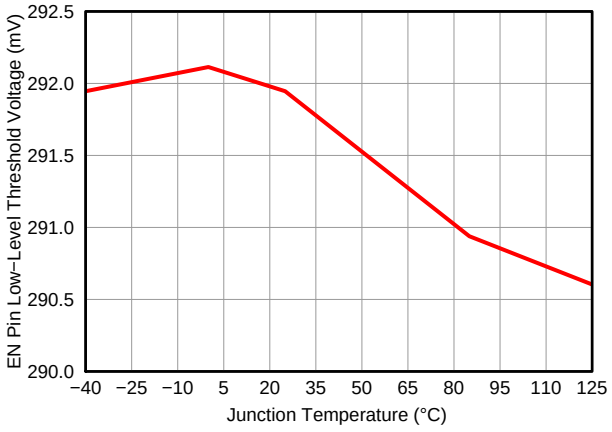


Figure 6. EN Pin Low-Level Threshold Voltage vs. Junction Temperature

TYPICAL CHARACTERISTICS (continued)

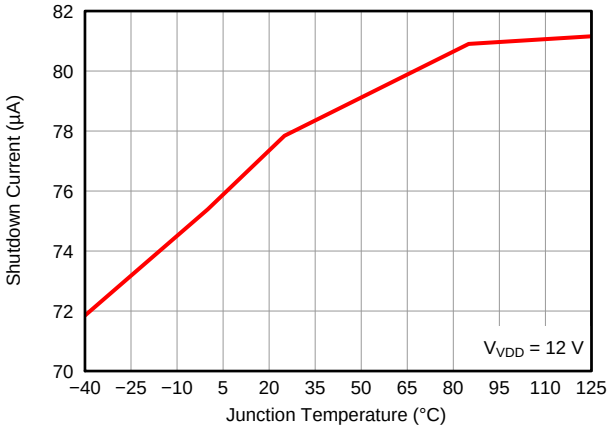


Figure 7. Shutdown Current vs. Junction Temperature

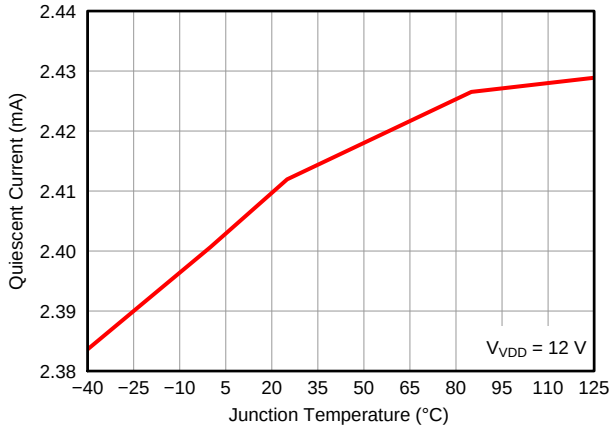


Figure 8. Quiescent Current vs. Junction Temperature

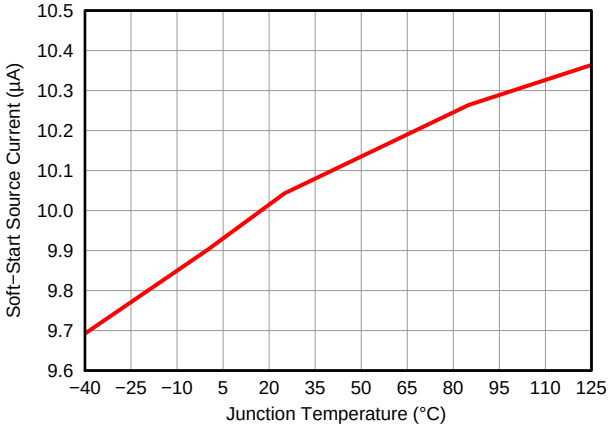


Figure 9. Soft-Start Source vs. Junction Temperature

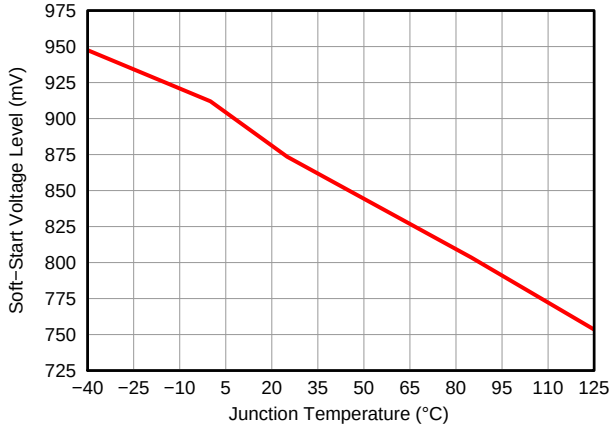


Figure 10. Soft-Start Voltage Level vs. Junction Temperature

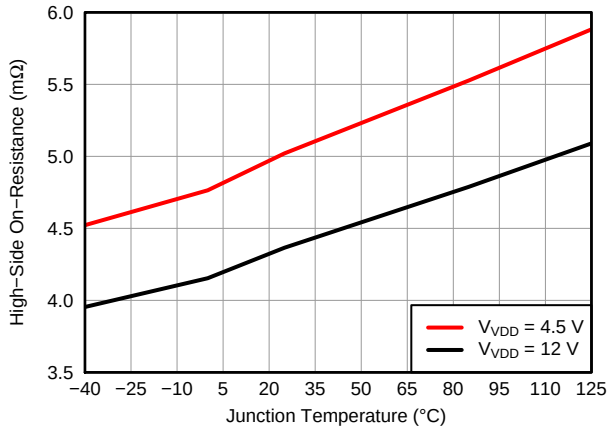


Figure 11. High-Side On Resistance vs. Junction Temperature

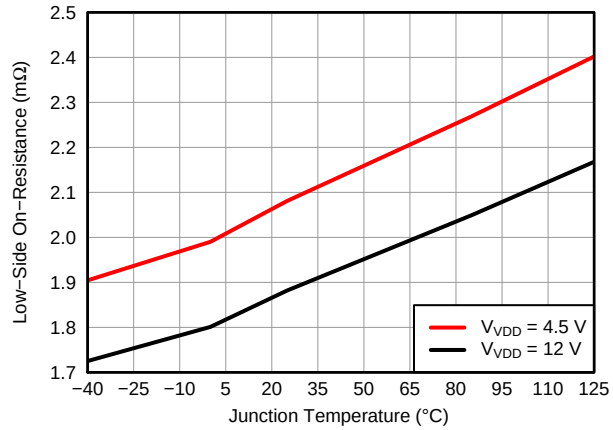


Figure 12. Low-Side On Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS

Figure 15 through Figure 18 are measured on a 2.5" × 2.5" × 0.062" FR4 board with 4 layers and 2 oz. copper, a 0.44-µH output inductor and a DCR of 0.32 mΩ.

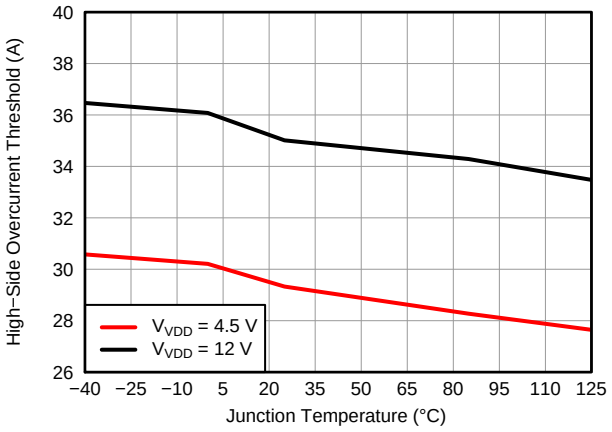


Figure 13. High-Side Overcurrent Threshold vs. Junction Temperature

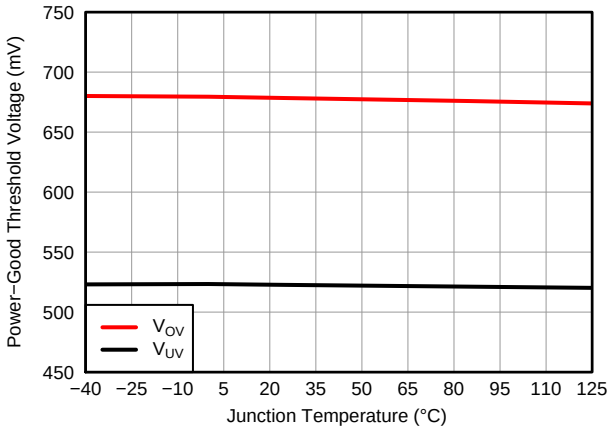


Figure 14. Power Good Threshold Voltage vs. Junction Temperature

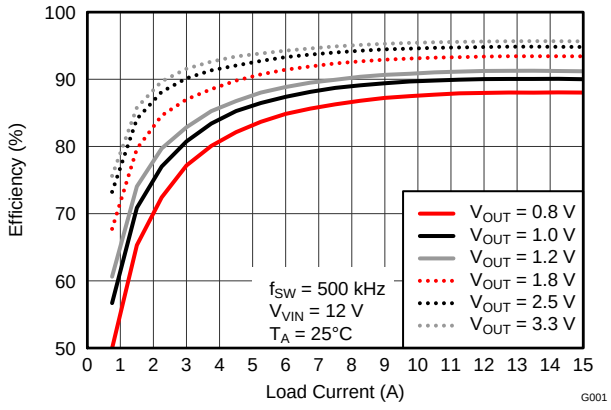


Figure 15. Efficiency vs. Load Current (V_{VIN} = 12 V)

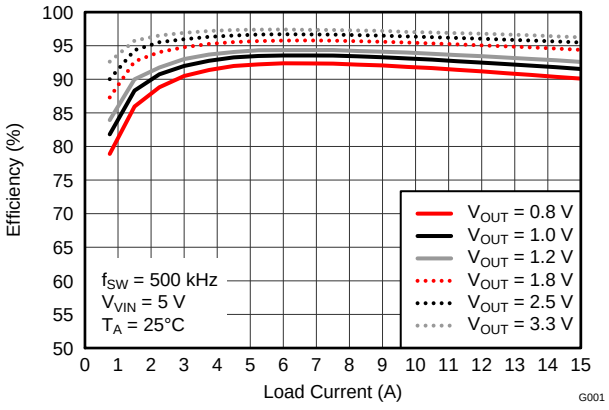


Figure 16. Efficiency vs. Load Current (V_{VIN} = 5 V)

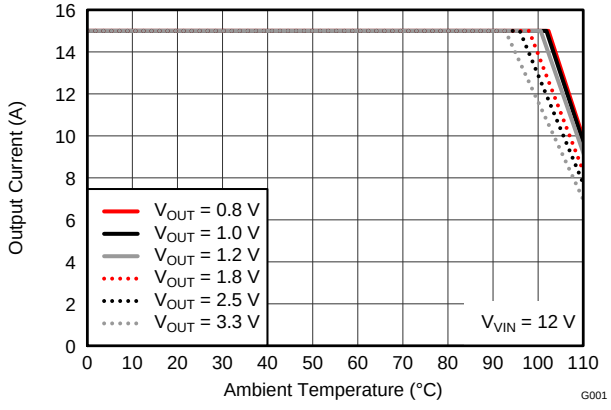


Figure 17. Output Current vs. Ambient Temperature (V_{VIN} = 12 V)

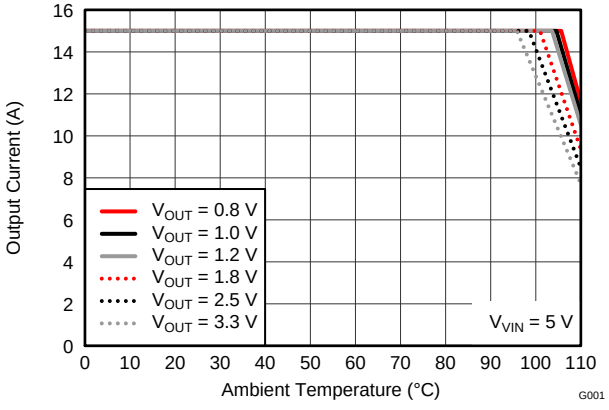


Figure 18. Output Current vs. Ambient Temperature (V_{VIN} = 5 V)

APPLICATION INFORMATION

Introduction

The TPS56121 is a 15-A high performance synchronous buck converter with two integrated N-channel NexFET™ power MOSFETs. The device implements a voltage-mode control with voltage feed-forward compensation that responds instantly to input voltage change. Pre-bias capability eliminates concerns about damaging sensitive loads.

Voltage Reference

The 600-mV bandgap cell is internally connected to the non-inverting input of the error amplifier. The reference voltage is trimmed with the error amplifier in a unity gain configuration to remove amplifier offset from the final regulation voltage. The 1% tolerance on the reference voltage allows the user to design a very accurate power supply.

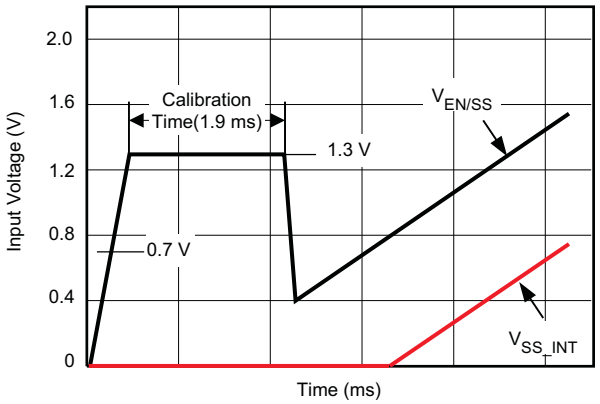


Figure 19. Startup Sequence and Timing

Enable Functionality, Startup Sequence and Timing

After input power is applied, an internal 40-µA current source begins to charge the soft-start capacitor connected from EN/SS to GND. When the voltage across that capacitor increases to 0.7 V, it enables the internal BP regulator followed by a calibration. Total calibration time is approximately 1.9 ms. See Figure 19. During the calibration, the device performs the following two functions.

COMP Pin Impedance Sensing

The device samples the impedance at the COMP pin and determines the appropriate operating switching frequency. If there is no resistor connected from the COMP pin to GND, the switching frequency is set to the default value of 500 kHz. If a resistor of 40.2 kΩ ± 10% is connected from the COMP pin to GND, the switching frequency is set to 300 kHz. Alternatively, if a resistor of 13.3 K ± 10% is connected from the COMP pin to GND, the switching frequency is set to 1 MHz.

After a 1.1-ms time period, the COMP pin is then brought low for 0.8 ms. This ensures that the feedback loop is preconditioned at startup and no sudden output rise occurs at the output of the converter when it is allowed to start switching.

Overcurrent Protection (OCP) setting

The device sources 10 µA (typical) to the resistor connected from the ILIM pin to GND. The voltage developed across that resistor multiplied by a factor of 2 is then sampled and latched off internally as the OCP trip level for the low-side FET until one cycles the input or toggles the EN/SS.

The voltage at EN/SS is internally clamped to 1.3 V before and/or during calibration to minimize the discharging time once calibration is complete. The discharging current is from an internal current source of 140 µA and it pulls the voltage down to 0.4 V. It then initiates the soft-start by charging up the capacitor using an internal current source of 10 µA. The resulting voltage ramp on this pin is used as a second non-inverting input to the error amplifier after an 800 mV (typical) downward level-shift; therefore, the actual soft-start does not take place until the voltage at this pin reaches 800 mV.

If the EN/SS pin is left floating, the controller starts automatically. EN/SS must be pulled down to less than 270 mV to ensure that the chip is in shutdown mode.

Soft-Start Time

The soft-start time of the TPS56121 is user programmable by selecting a single capacitor. The EN/SS pin sources 10 µA to charge this capacitor. The actual output ramp-up time is the amount of time that it takes for the 10 µA to charge the capacitor through a 600 mV range. There is some initial lag due to calibration and an offset (800 mV) from the actual EN/SS pin voltage to the voltage applied to the error amplifier.

The soft-start is accomplished in a closed-loop, meaning that the error amplifier controls the output voltage at all times during the soft-start period and the feedback loop is never open as occurs in duty cycle limit soft-start schemes. The error amplifier has two non-inverting inputs, one connected to the 600-mV reference voltage, and the other connected to the offset EN/SS pin voltage. The lower of these two voltages is what the error amplifier controls the FB pin to. As the voltage on the EN/SS pin ramps up past approximately 1.4 V (800 mV offset voltage plus the 600 mV reference voltage), the 600-mV reference voltage becomes the dominant input and the converter has reached its final regulation voltage.

The capacitance required for a given soft-start ramp time for the output voltage is calculated in Equation 1.

$$C_{SS} = \left(\frac{I_{SS}}{V_{FB}} \right) \times t_{SS} \quad (1)$$

where

- C_{SS} is the required capacitance on the EN/SS pin (nF)
- I_{SS} is the soft-start source current (10 µA)
- V_{FB} is the feedback reference voltage (0.6 V)
- t_{SS} is the desired soft-start ramp time (ms)

Oscillator

The oscillator frequency is internally fixed at 500 KHz if there is no resistor connected from COMP pin to GND. Optionally, a 40.2-kΩ resistor from the COMP pin to GND sets the frequency to 300 KHz. Alternatively, a 13.3-kΩ resistor from COMP pin GND sets the frequency to 1 MHz.

Overcurrent Protection (OCP)

Programmable OCP level at ILIM is from 6 mV to 50 mV. With a scale factor of 2, the actual OC trip point across the low-side FET is in the range of 12 mV to 100 mV.

If the voltage drop across R_{OCSET} reaches 300 mV during calibration (No R_{OCSET} resistor included), it disables OC protection. Once disabled, there is no low-side or high-side current sensing.

OCP level for the high-side FET is fixed at 34 A (typical). The high-side OCP provides pulse-by-pulse current limiting.

OCP sensing for the low-side FET is a true inductor valley current detection, using sample and hold. Equation 2 can be used to calculate R_{OCSET}.

$$R_{OCSET} = \left(I_{OUT(max)} - \left(\frac{I_{P-P}}{2} \right) \right) \times 95 + 62.5 \quad (2)$$

where

- I_{P-P} is the peak-to-peak inductor current (A)
- $I_{OUT(max)}$ is the trip point for OCP (A)
- R_{OCSET} is the resistor used for setting the OCP level (Ω)

An overcurrent (OC) condition is detected by sensing voltage drop across the low-side FET and across the high-side FET. If the voltage drop across either FET exceeds OC threshold, a count increments one count. If no OC condition is detected on either FET, the fault counter decrements by one counter. If three OC pulses are summed, a fault condition is declared which cycles the soft-start function in a hiccup mode. Hiccup mode is defined as four dummy soft-start timeouts followed by a real one if overcurrent condition is encountered during normal operation; or five dummy soft-start timeouts followed by a real one if overcurrent condition occurs from the beginning during start. This cycle continues indefinitely until the fault condition is removed.

Switching Node (SW)

The SW pin connects to the switching node of the power conversion stage. It acts as the return path for the high-side gate driver. When configured as a synchronous buck stage, the voltage swing on SW normally traverses from below ground to well above the input voltage. Parasitic inductance in the high-side FET and the output capacitance (C_{OSS}) of both power FETs form a resonant circuit that can produce high frequency (> 100 MHz) ringing on this node. The voltage peak of this ringing, if not controlled, can be significantly higher than the input voltage. Ensure that the peak ringing amplitude does not exceed the absolute maximum rating limit for the pin.

In many cases, a series resistor and capacitor snubber network connected from the switching node to PGND can be helpful in damping the ringing and decreasing the peak amplitude. Provide provisions for snubber network components in the layout of the printed circuit board. If testing reveals that the ringing amplitude at the SW pin exceeds the limit, then include snubber components.

Placing a BOOT resistor with a value between 5 Ω and 10 Ω in series with the BOOT capacitor slows down the turn-on of the high-side FET and can help to reduce the peak ringing at the switching node as well.

Input Undervoltage Lockout (UVLO)

The TPS56121 has fixed input under-voltage lockout (UVLO). In order for the device to turn on, the following conditions must be met:

- the EN/SS pin voltage must be greater than V_{IH}
- the input voltage must exceed UVLO on voltage V_{UVLO}

The UVLO has a minimum of 500 mV hysteresis built-in.

Pre-Bias Startup

The TPS56121 contains a unique circuit to prevent current from being pulled from the output during startup in the condition the output is pre-biased. There are no PWM pulses until the internal soft-start voltage rises above the error amplifier input (FB pin), if the output is pre-biased. Once the soft-start voltage exceeds the error amplifier input, the controller slowly initiates synchronous rectification by starting the synchronous rectifier with a narrow on time. It then increments the on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter.

This approach prevents the sinking of current from a pre-biased output, and ensures the output voltage startup and ramp to regulation is smooth and controlled.

Power Good

The TPS56121 provides an indication that output is good for the converter. This is an open drain signal and pulls low when any condition exists that would indicate that the output of the supply might be out of regulation. These conditions include:

- V_{FB} is more than ±12.5% from nominal
- soft-start is active
- a short circuit condition has been detected

NOTE

When there is no power to the device, PGOOD is not able to pull close to GND if an auxiliary supply is used for the power good indication. In this case, a built in resistor connected from drain to gate on the PGOOD pull down device makes the PGOOD pin look approximately like a diode to GND.

Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of 145°C, both the high-side FET and low-side FET maintain off status. When the junction cools to the required level (125°C typical), the PWM initiates soft start as during a normal power-up cycle.

DESIGN EXAMPLE

Introduction

This design example describes a 15-A, 12-V to 1.0-V design using the TPS56121 high-current integrated buck converter. The system specifications are listed in Table 1.

Table 1. TPS56121 Design Example Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		8	12	14	V
$V_{IN(ripple)}$	Input ripple	I_{OUT} = 15 A			0.15	V
V_{OUT}	Output voltage	0 A ≤ I_{OUT} ≤ 15 A	0.98	1.00	1.02	V
	Line regulation	8 V ≤ V_{IN} ≤ 14 V			0.1%	
	Load regulation	0 A ≤ I_{OUT} ≤ 15 A			0.5%	
V_{RIPPLE}	Output ripple	I_{OUT}= 15 A		20		mV
V_{OVER}	Output overshoot	I_{TRAN} = 5 A		50		mV
V_{UNDER}	Output undershoot	I_{TRAN} = 5 A		50		mV
I_{OUT}	Output current	8 V ≤ V_{IN} ≤ 14 V	0		15	A
t_{SS}	Soft-start time	V_{IN} = 12 V		2.0		ms
$I_{OUT(max)}$	Short- circuit current trip point		20			A
η	Efficiency	V_{IN} = 12 V, I_{OUT} = 15 A		90		%
f_{SW}	Switching frequency			500		kHz

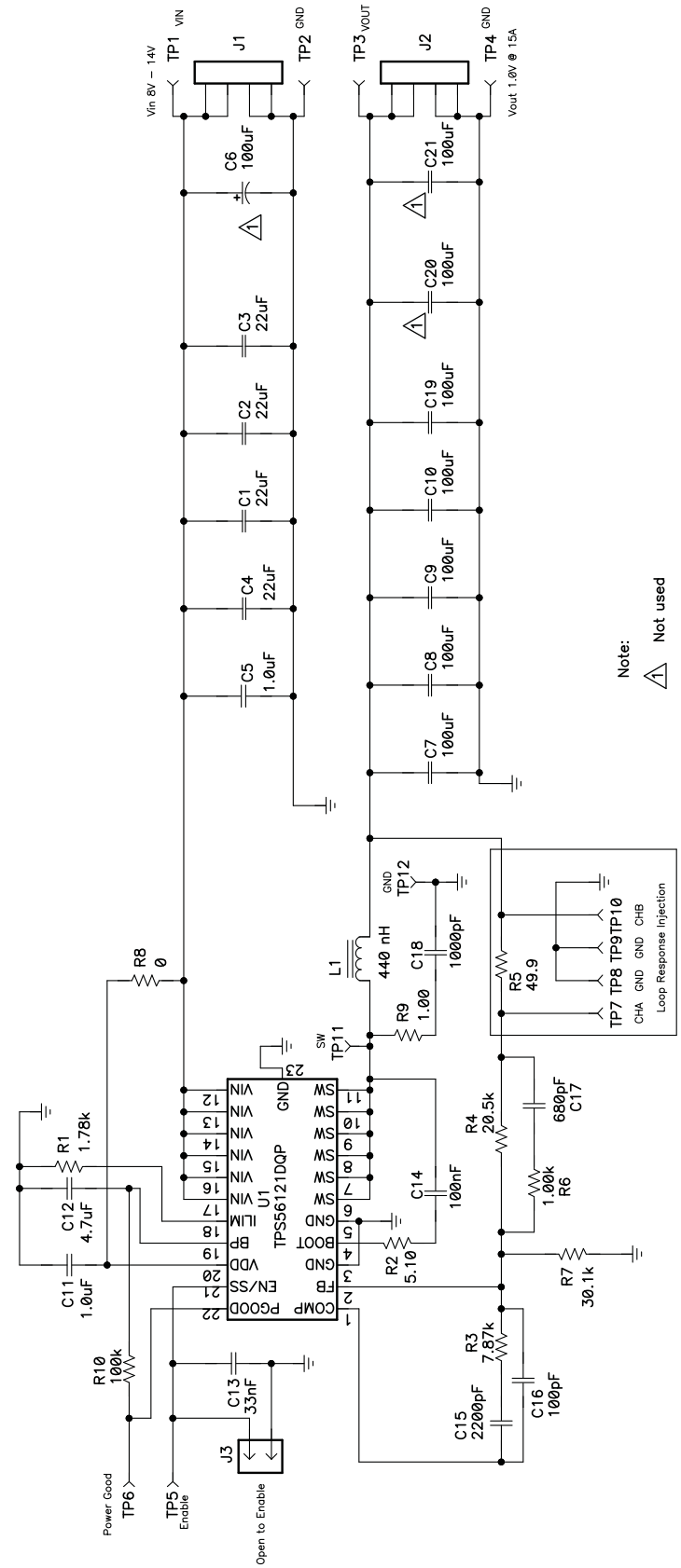


Figure 20. Design Example Schematic

Design Procedure

Switching Frequency Selection

To achieve a balance between small size and high efficiency for this design, use switching frequency of 500 kHz.

Inductor Selection (L1)

Synchronous buck power inductors are typically sized for between approximately 20% and 40% peak-to-peak ripple current (I_{P-P}).

Using this target ripple current, the required inductor size can be calculated as shown in Equation 3.

$$L \approx \frac{V_{IN(max)} - V_{OUT}}{0.3 \times I_{OUT}} \times \frac{V_{OUT}}{V_{IN(max)}} \times \frac{1}{f_{SW}} = \frac{14\,V - 1.0\,V}{0.3 \times 15\,A} \times \frac{1.0\,V}{14\,V} \times \frac{1}{500\,kHz} = 413\,nH \quad (3)$$

Selecting a standard 440-nH inductor value, I_{P-P} = 4.2 A.

The RMS current through the inductor is approximated in Equation 4.

$$I_{L(rms)} = \sqrt{(I_{OUT})^2 + \left(\tfrac{1}{12} \times (I_{P-P})^2\right)} = \sqrt{(15)^2 + \left(\tfrac{1}{12} \times (4.2)^2\right)} = 15.05\,A \quad (4)$$

Output Capacitor Selection

The output transient response typically drives the selection of the output capacitor. For applications where $V_{IN(min)} > 2 \times V_{OUT}$, use overshoot to calculate the minimum output capacitance, as shown in Equation 5.

$$C_{OUT(min)} = \frac{(I_{TRAN})^2 \times L}{(V_{OUT} \times V_{OVER})} = \frac{5^2 \times 440\,nH}{1.0 \times 50\,mV} = 220\,\mu F \quad (5)$$

For applications where $V_{IN(min)} < 2 \times V_{OUT}$, use overshoot to calculate the minimum output capacitance. The equation is shown in Equation 6

$$C_{OUT(min)} = \frac{(I_{TRAN})^2 \times L}{(V_{IN} - V_{OUT}) \times V_{UNDER}} \quad (6)$$

In order to meet the low ESR and high capacitance requirements, this design uses five 100-µF, 1210 ceramic capacitors. With a minimum capacitance, maximum ripple voltage determines the maximum allowable ESR. The ESR is approximated in Equation 7.

$$ESR_{COUT(max)} = \frac{V_{RIPPLE} - V_{RIPPLE(COUT)}}{I_{P-P}} = \frac{V_{RIPPLE} - \left(\frac{I_{P-P}}{8 \times C_{OUT} \times f_{SW}}\right)}{I_{P-P}} = \frac{20\,mV - \left(\frac{4.2\,A}{8 \times 500\,\mu F \times 500\,kHz}\right)}{4.2\,A} = 4.3\,m\Omega \quad (7)$$

Inductor Peak Current Rating

With output capacitance, it is possible to calculate the charge current during start-up and determine the minimum saturation current rating for the inductor. Equation 8 approximates the start-up charging current (I_{CHARGE}).

$$I_{CHARGE} = \frac{V_{OUT} \times C_{OUT}}{t_{SS}} = \frac{1.0\,V \times 500\,\mu F}{2\,ms} = 0.25\,A \tag{8}$$

Equation 9 approximates the peak current in the inductor, $I_{L(peak)}$.

$$I_{L(peak)} = I_{OUT} + \left(\tfrac{1}{2} \times I_{RIPPLE}\right) + I_{CHARGE} = 15\,A + \left(\tfrac{1}{2} \times 4.2A\right) + 0.25\,A = 17.4\,A \tag{9}$$

With the short circuit current trip point $I_{OUT(max)}$ set at 20 A, the maximum allowable peak current $I_{L\_PEAK(max)}$ is shown in Equation 10.

$$I_{L\_PEAK(max)} = I_{OUT(max)} + \left(\tfrac{1}{2} \times I_{RIPPLE}\right) = 20\,A + \left(\tfrac{1}{2} \times 4.2A\right) = 22.1A \tag{10}$$

The selection of output capacitor meets the maximum allowable peak current requirement.

Table 2. Inductor Requirements Summary

PARAMETER		VALUE	UNITS
L	Inductance	440	nH
$I_{L(rms)}$	RMS current (thermal rating)	15.1	A
$I_{L\_PEAK(max)}$	Peak current (saturation rating)	22.1	A

Thie design uses a PA0513.441NLT, 440-nH, 0.32-mΩ, 30-A inductor.

Input Capacitor Selection

The input voltage ripple is divided between capacitance and ESR. For this design $V_{IN\_RIPPLE(CAP)}$ = 100 mV and $V_{IN\_RIPPLE(ESR)}$ = 50 mV. Use Equation 11 to estimate the minimum capacitance. Use Equation 12 to estimate the maximum ESR.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT} \times \left(V_{IN(min)} - V_{OUT}\right)}{V_{IN\_RIPPLE(CAP)} \times \left(V_{IN(min)}\right)^2 \times f_{SW}} = \frac{15 \times 1.0\,V \times (8\,V - 1.0\,V)}{100\,mV \times (8\,V)^2 \times 500\,kHz} = 32.8\,\mu F \tag{11}$$

$$ESR_{CIN(max)} = \frac{V_{IN\_RIPPLE(ESR)}}{I_{OUT} + \left(\frac{I_{P-P}}{2}\right)} = \frac{50\,mV}{15\,A + \left(\frac{4.2\,A}{2}\right)} = 2.9\,m\Omega \tag{12}$$

Equation 13 estimates the RMS current in the input capacitors.

$$I_{RMS(cin)} = I_{OUT} \times \sqrt{D_{MAX} \times (1 - D_{MAX})} = 15\,A \times \sqrt{\frac{1}{8} \times \left(1 - \frac{1}{8}\right)} = 5.0\,A_{rms} \tag{13}$$

Four 1210, 22-µF, 25-V, X5R, ceramic capacitors with approximately 2.5-mΩ ESR and a 2.5-A RMS current rating are selected. Higher voltage capacitors are selected to minimize capacitance loss at the DC bias voltage to ensure the capacitors will have sufficient capacitance at the working voltage while a 1.0-µF capacitor in smaller case size is used to reduce high frequency noise from the MOSFET switching.

Bootstrap Capacitor (C14)

The bootstrap capacitor maintains power to the high-side driver during the high-side switch ON time. Per the requirements of the integrated MOSFET, the value of C_{BOOT} is 100 nF with a minimum 10-V rating.

Bootstrap Resistor (R2)

The bootstrap resistor slows the rising edge of the SW voltage to reduce ringing and improve EMI. Per the datasheet recommendation a 5.1-Ω resistor is selected.

RC Snubber (R9 and C18)

To effectively limit the switch node ringing, select a 1.0-Ω resistor and a 1000-pF capacitor

VDD Bypass Capacitor (C11)

Per the data sheet recommended pin terminations, bypass VDD to GND with a 1.0-µF capacitor.

BP5 Bypass Capacitor (C12)

Per the data sheet recommended pin functions, bypass BP5 to GND with a capacitor with a value of at least 1.0-µF. For additional filtering and noise immunity, select a 4.7-µF capacitor.

Soft-Start Capacitor (C13)

The soft-start capacitor provides a constant ramp voltage to the error amplifier to provide controlled, smooth start-up. The soft-start capacitor is sized using Equation 14.

$$C_{SS} = \frac{I_{SS}}{V_{FB}} \times t_{SS} = \frac{10\,\mu A}{0.6\,V} \times 2.0\,ms = 33\,nF \tag{14}$$

Current Limit (R1)

The TPS56221 uses the negative drop across the internal low-side FET at the end of the OFF-time to measure the valley of the inductor current. Allowing for a minimum 20-A, or 30% over maximum load, the programming resistor is selected using Equation 15.

$$R_{OCSET} = 95 \times \left(I_{OUT(max)} - \left(\frac{I_{P-P}}{2} \right) \right) + 62.5\ \Omega = 95 \times \left(20\ A - \left(\frac{4.2\ A}{2} \right) \right) + 62.5\ \Omega = 1.76\ k\Omega \tag{15}$$

Select a standard 1.78-kΩ resistor from the E-48 series.

Feedback Divider (R4, R7)

The TPS56121 converter uses a full operational amplifier with an internally fixed 0.600-V reference. R4 is selected between 10 kΩ and 50 kΩ for a balance of feedback current and noise immunity. With R4 set to 20.5 kΩ, program the output voltage with a resistor divider as calculated in Equation 16.

$$R7 = \frac{V_{FB} \times R4}{(V_{OUT} - V_{FB})} = \frac{0.600\,V \times 20.5\,k\Omega}{(1.0\,V - 0.600\,V)} = 30.8\,k\Omega \tag{16}$$

Select a standard 30.1-kΩ resistor from the E-48 series.

Compensation (C15, C16, C17, R3, R6)

Using the *TPS40k Loop Stability Tool* for 50 kHz of bandwidth and 60 degrees of phase margin with an R4 value of 20.5 kΩ, the design yields the following values.

- C17 = C_1 = 680 pF
- C15 = C_2 = 2200 pF
- C16 = C_3 = 100 pF
- R6 = R_2 = 1.00 kΩ
- R3 = R_3 = 7.87 kΩ

DESIGN EXAMPLE PERFORMANCE CHARACTERISTICS

Output voltage 12 V to 1.0 V at 0-A to 15-A input current.

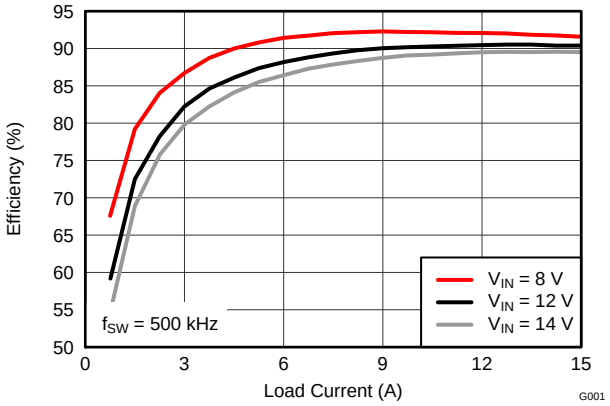


Figure 21. Efficiency vs Load Current

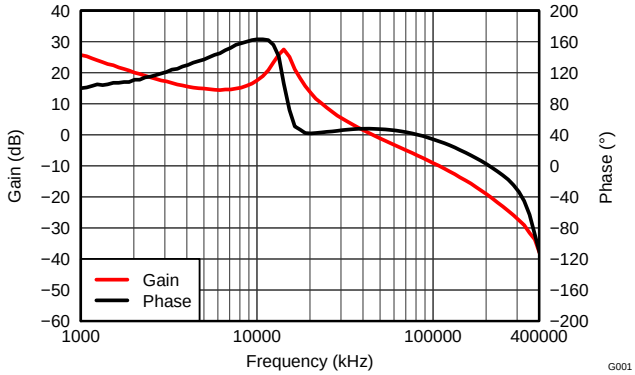


Figure 22. Loop Response, 47-kHz Bandwidth, 48° Phase Margin

Figure 23. Output Ripple 20 mV/div, 1.0 µs/div, 20 MHz Bandwidth, AC Coupled

Table 3. List of Materials for TPS56121 Design Example

REFERENCE DESIGNATOR	QTY	VALUE	DESCRIPTION	SIZE	PART NUMBER	MANUFACTURER
C1, C2, C3, C4	4	22 µF	Capacitor, Ceramic, 25 V, X5R, 20%	1210	Std	Std
C5, C11	2	1.0 µF	Capacitor, Ceramic, 25V, X7R, 20%	0805	Std	Std
C6	0	100 µF	Capacitor, Aluminum, 16 VDC, ±20%	Code D8	EEEFP1C101AP	Panasonic
C7, C8, C9, C10, C19	5	100 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	1210	Std	Std
C12	1	4.7 µF	Capacitor, Ceramic, 10 V, X5R, 20%	0805	Std	Std
C13	1	33 nF	Capacitor, Ceramic, 16 V, X7R, 20%	0603	Std	Std
C14	1	100 nF	Capacitor, Ceramic, 50 V, X7R, 20%	0603	Std	Std
C15	1	2200 pF	Capacitor, Ceramic, 50 V, X7R, 10%	0603	Std	Std
C16	1	100 pF	Capacitor, Ceramic, 50 V, C0G, 5%	0603	Std	Std
C17	1	680 pF	Capacitor, Ceramic, 50 V, C0G, 5%	0603	Std	Std
C18	1	1000 pF	Capacitor, Ceramic, 50 V, X7R, 20%	0603	Std	Std
C20, C21	0	100 µF	Capacitor, Ceramic, 6.3 V, X5R, 20%	1210	Std	Std
J1, J2	2		Terminal Block, 4-pin, 15 A, 5.1 mm	0.80 x 0.35 inch	ED120/4DS	OST
J3	1		Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
L1	1	440 nH	Inductor, 440 nH, 30A, 0.32 mΩ	0.530 x 0.510 inch	PA0513.441NLT	Pulse
R1	1	1.78 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R2	1	5.10 Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R3	1	7.87 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R4	1	20.5 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R5	1	49.9 Ω	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R6	1	1.00 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R7	1	30.1 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R8	1	0 Ω	Resistor, Chip, 1/16 W, 1%	0603	Std	Std
R9	1	1.00 Ω	Resistor, Chip, 1/8 W, 1%	0805	Std	Std
R10	1	100 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
TP1, TP3, TP11	3		Test Point, Red, Thru Hole	0.125 x 0.125 inch	5010	Keystone
TP2, TP4, TP8, TP9, TP12	5		Test Point, Black, Thru Hole	0.125 x 0.125 inch	5011	Keystone
TP5, TP6	2		Test Point, Yellow, Thru Hole	0.125 x 0.125 inch	5014	Keystone
TP7, TP10	2		Test Point, White, Thru Hole	0.125 x 0.125 inch	5012	Keystone
U1	1		4.5-V to 14-V input, 15-A, synchronous buck converter	QFN-22 6 × 5 mm	TPS56121DQP	TI

Layout Recommendations

- Place input capacitors next to the VIN pin and on the same side as the device. Use wide and short traces or copper planes for the connection from the VIN pin to the input capacitor and from the input capacitor to the power pad of the device.
- Place the BP decoupling capacitor close to the BP pin and on the same side as the device in order to avoid the use of vias. Use wide and short traces for the connection from the BP pin to the capacitor and from the capacitor to the power pad. If vias are not evitable, use at least three vias to reduce the parasitic inductance.
- Include a Kelvin VDD connection, or separate from VIN connection (bypass input capacitors); add a placeholder for a filter resistor between the VDD pin and the input bus. Place the VDD decoupling capacitor near the VDD pin and on the same side as the device to avoid the use of vias. Use wide and short traces for the connection from the VDD pin to the capacitor and from the capacitor to the power pad of the device. If

vias are not avoidable, use at least three vias to reduce the parasitic inductance.

- Maintain the FB trace away from BOOT and SW traces.
- Minimize the area of switch node.
- Use a single ground.Do not use separate signal and power ground.
- Use 3 × 7 thermal vias as suggested in the LAND PATTERN DATA section of this datasheet.

EVM Layout

The TPS56121EVM-601 layout is shown in Figure 24 through Figure 29 for reference.

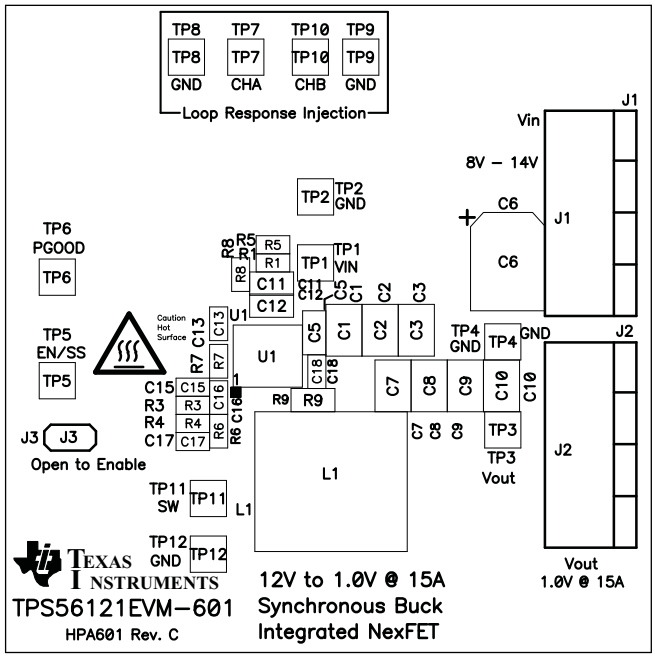


Figure 24. TPS56121EVM-601 Top Assembly Drawing (Top view)

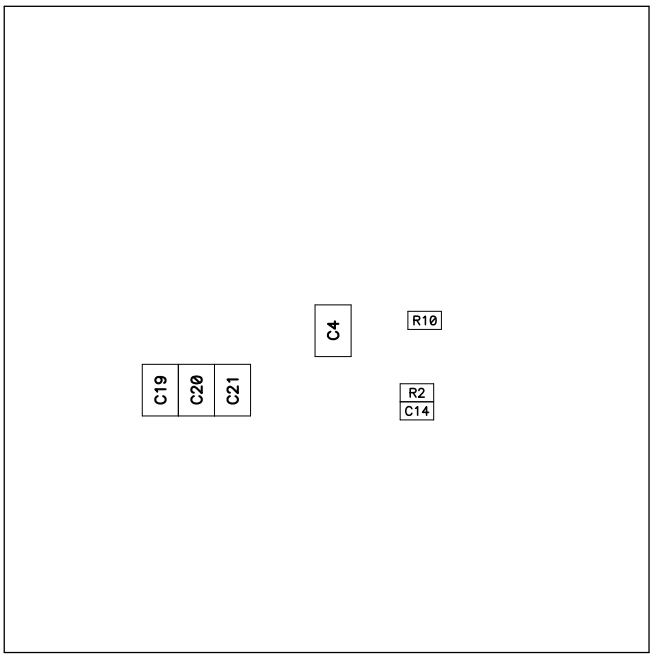


Figure 25. TPS56121EVM-601 Bottom Assembly Drawing (Bottom view)

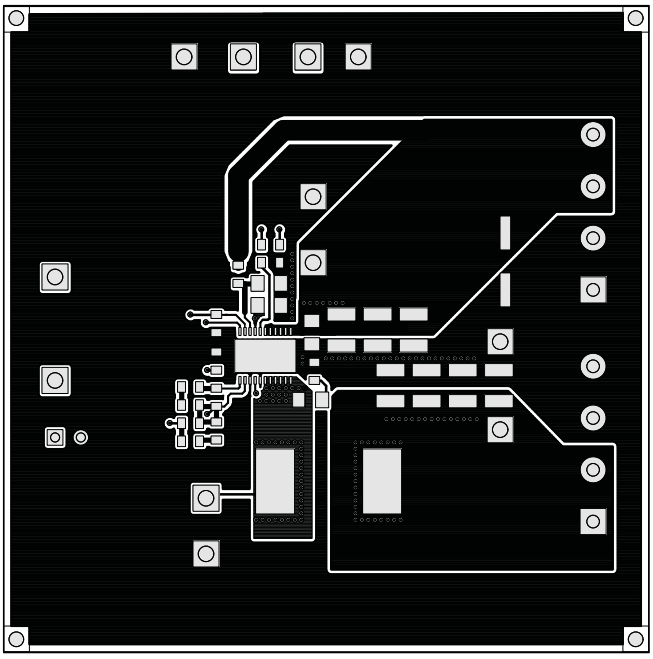


Figure 26. TPS56121EVM-601 Top Copper (Top View)

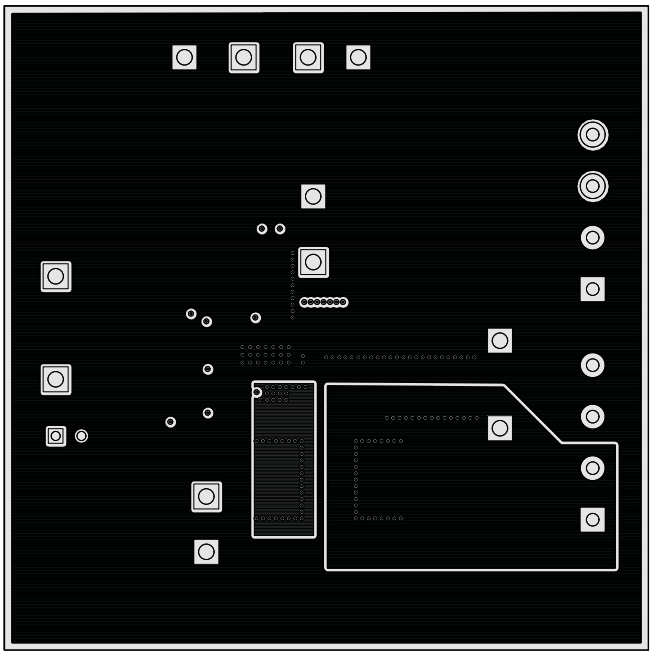


Figure 27. TPS56121EVM-601 Internal 1 (Top View)

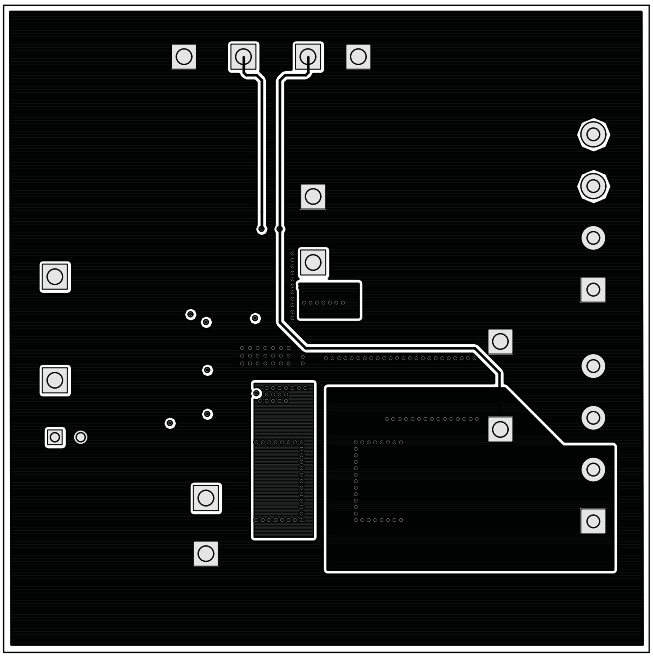


Figure 28. TPS56121EVM-601 Internal 2 (Top View)

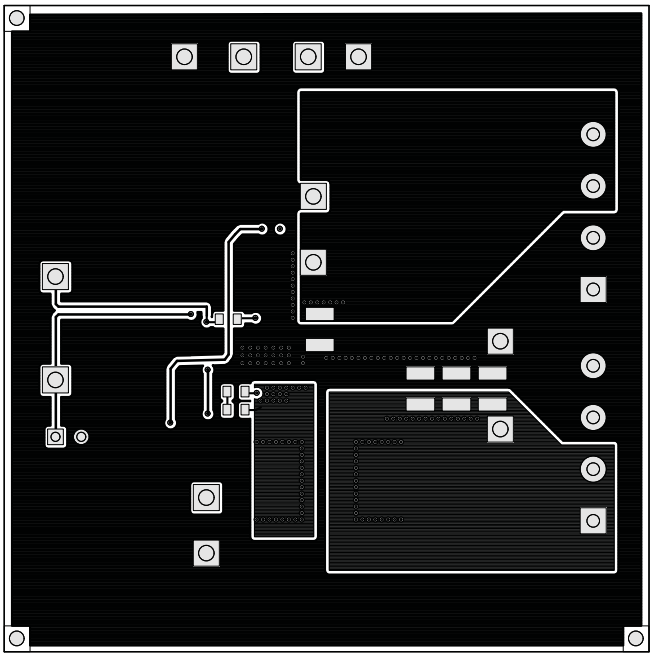


Figure 29. TPS56121EVM-601 Bottom Copper (Top View)

REVISION HISTORY

Changes from Original (March 2011) to Revision A **Page**

- Changed characterization conditions 9
- Changed corrected typographical error in Equation 2 11
- Added Switching Node (SW) section 12
- Added clarity to Thermal Shutdown section 13
- Deleted old Design example 14
- Added new Design example 14
- Added Layout Recomendations section 20
- Added EVM Layout section 21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS56121DQPR	ACTIVE	LSON-CLIP	DQP	22	2500	RoHS-Exempt & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	TPS56121	Samples
TPS56121DQPT	ACTIVE	LSON-CLIP	DQP	22	250	RoHS-Exempt & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	TPS56121	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

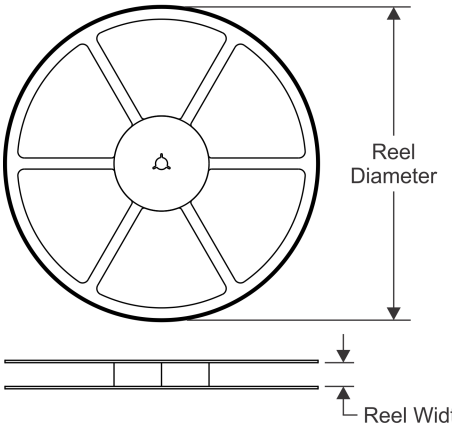
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

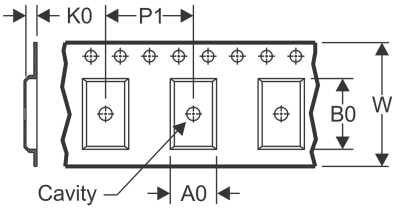
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

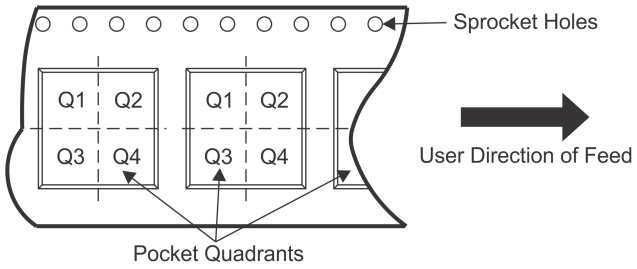


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

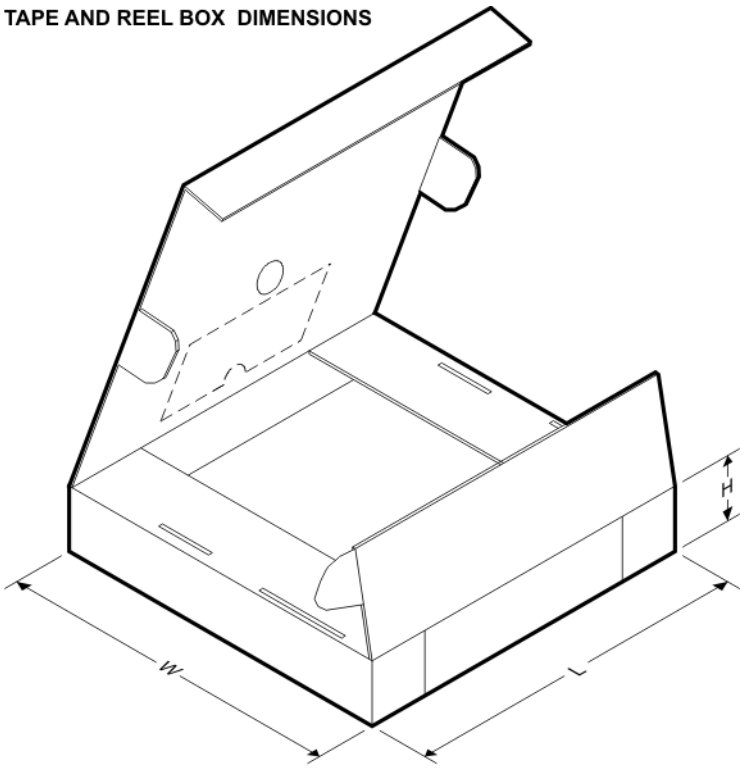
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS56121DQPR	LSON-CLIP	DQP	22	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1
TPS56121DQPT	LSON-CLIP	DQP	22	250	180.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1

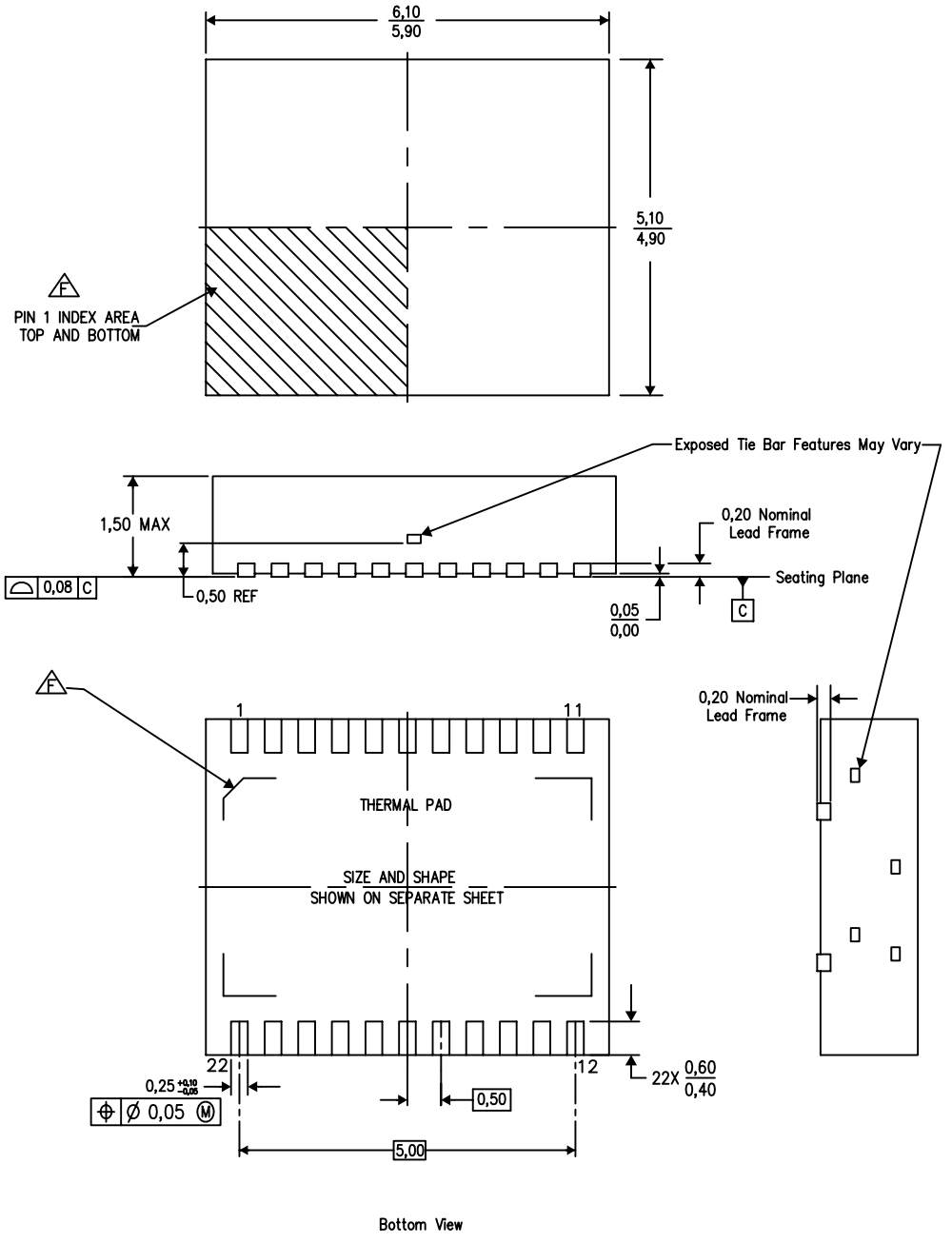
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS56121DQPR	LSON-CLIP	DQP	22	2500	367.0	367.0	35.0
TPS56121DQPT	LSON-CLIP	DQP	22	250	210.0	185.0	35.0

DQP (R–PSON–N22) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

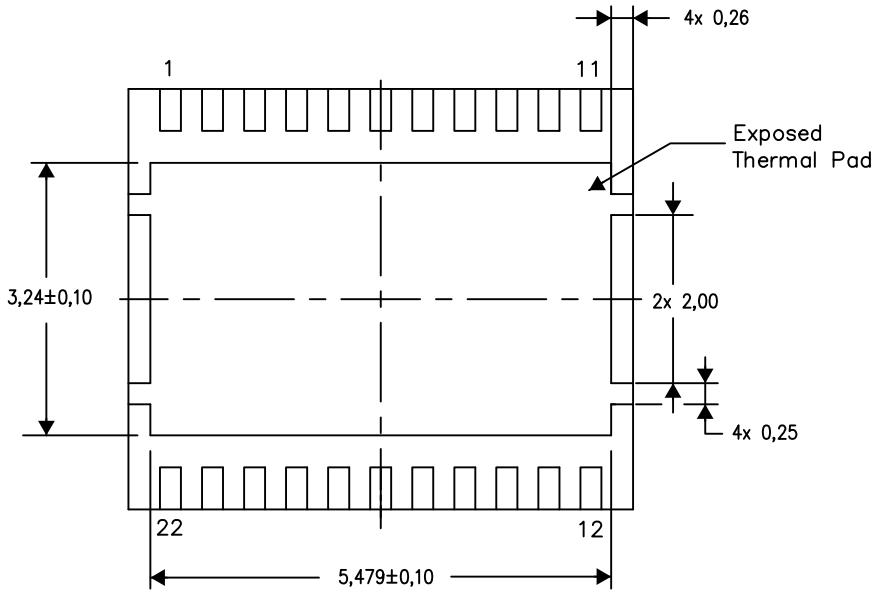
DQP (R–PSON–N22) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



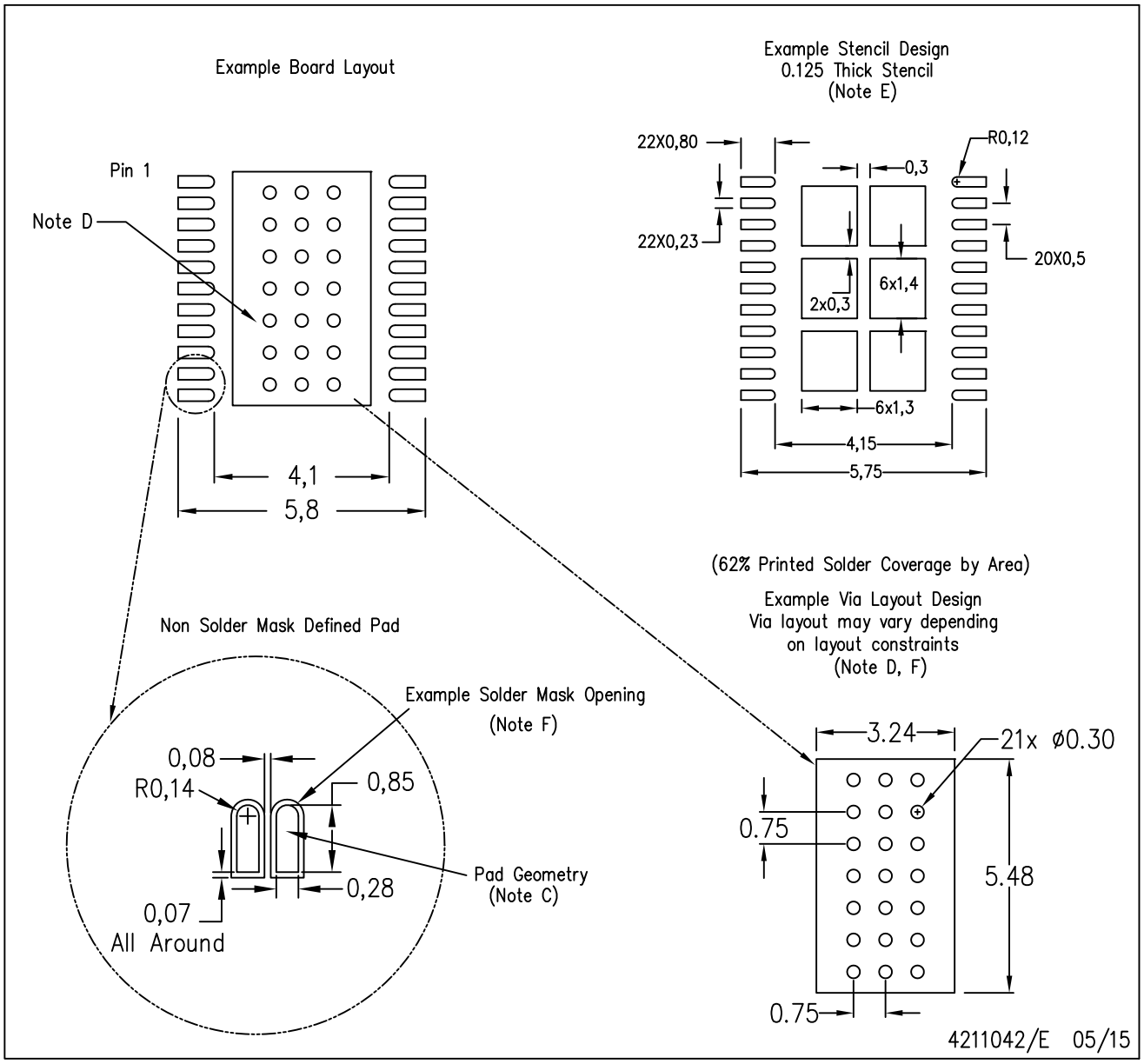
Bottom View

Exposed Thermal Pad Dimensions

4211024–3/H 08/15

NOTE: All linear dimensions are in millimeters

DQP (R–PSON–N22) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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