TPS63020-Q1 具有 4A 开关电流的高效单电感升压/降压转换器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 的下列结果：
  - 器件温度等级：运行结温范围为 -40°C 至 125°C
  - 器件人体放电模型 (HBM) 静电放电 (ESD) 分类等级 H1B
  - 器件充电器件模型 (CDM) ESD 分类等级 C4B
- 输入电压范围：1.8V 至 5.5V
- 效率高达 96%
- 3.3V 降压模式下的输出电流为 3A (V_{IN} > 3.6V)
- 3.3V 升压模式下的输出电流高于 2A (V_{IN} > 2.5V)
- 在降压和升压模式之间实现自动转换
- 动态输入电流限制
- 器件的静态电流小于 50μA
- 可调节输出电压范围：1.2V 至 5.5V
- 用于改进低输出功率效率的节能模式
- 2.4MHz 强制固定运行频率并可实现同步
- 智能电源正常状态输出
- 关机期间负载断开
- 过温保护
- 过压保护
- 采用 3mm × 4mm 超薄小外形尺寸无引线 (VSON)-14 封装

2 应用范围

- 信息娱乐
- 远程信息处理/紧急呼叫 (eCall)

3 说明

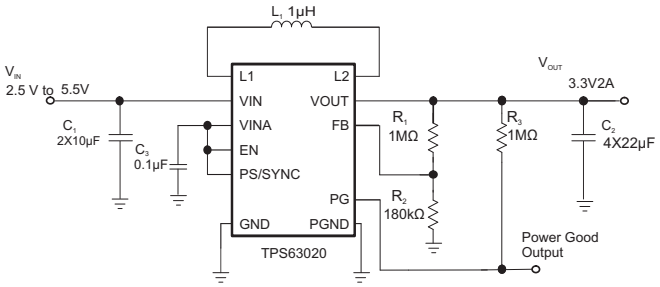
TPS63020-Q1 器件是一款电源解决方案，广泛应用于由 2-3 节碱性电池、镍镉 (NiCd) 电池、镍氢 (NiMH) 电池以及单节锂离子电池或锂聚合物电池供电的产品。当使用单节锂离子电池或锂聚合物电池供电时，该器件提供高达 3A 的输出电流并可对电池进行放电，使其电压降至 2.5V 或更低水平。 此升压/降压转换器基于一个频率固定的脉宽调制 (PWM) 控制器。该控制器可通过同步整流实现效率最大化。 在负载电流较低的情况下，该转换器会进入节能模式，以在宽负载电流范围内保持高效率。 禁用省电模式则会强制转换器以固定开关频率运行。 开关的最大平均电流为 4A（典型值）。输出电压可通过外部电阻分频器进行编程。 转换器可被禁用以最大限度地减少电池消耗。 在关机期间，负载从电池上断开。 该器件采用 3mm × 4mm 14 引脚 VSON PowerPAD™ 封装 (DSJ)。

器件信息(1)

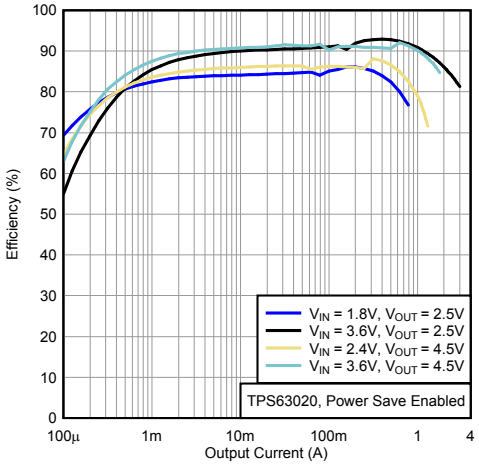
部件号	封装	封装尺寸（标称值）
TPS63020-Q1	VSON (14)	3.00mm x 4.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 典型应用电路原理图



效率与输出电流间的关系



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5 修订历史记录

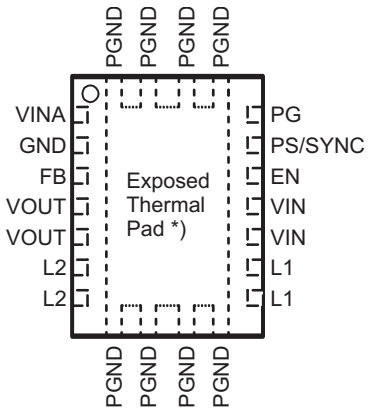
日期	修订版本	注释
2015 年 10 月	*	最初发布版本。

6 Device Comparison Table

PART NUMBER	V_{OUT}
TPS63020-Q1	Adjustable

7 Pin Configuration and Functions

DSJ Package
14-Pin VSON (QFN)
(Top View)



NOTE: *) The exposed thermal pad is connected to PGND.

See *TPS63020-Q1 Pin FMEA* Application Report SLVA736

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	12	I	Enable input (1 enabled, 0 disabled), must not be left open
FB	3	I	Voltage feedback of adjustable versions.
GND	2		Control/logic ground
L1	8, 9	I	Connection for inductor
L2	6, 7	I	Connection for inductor
PG	14	O	Output power good (1 good, 0 failure; open drain)
PGND			Power ground
PS/SYNC	13	I	Enable/disable power save mode (1 disabled, 0 enabled, clock signal for synchronization), must not be left open
VIN	10, 11	I	Supply voltage for power stage
VINA	1	I	Supply voltage for control stage
VOUT	4, 5	O	Buck-boost converter output
Exposed Thermal Pad			The exposed thermal pad is connected to PGND.

8 Specifications

8.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage (2)	VIN, VINA, L1, L2, VOUT, PS/SYNC, EN, FB, PG	–0.3	7	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

8.2 ESD Ratings

			Value	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human body model (HBM), per AEC Q100-002(2)	±1000	V
		Charged device model (CDM), per AEC Q100-011	±500	

(1) Electrostatic discharge (ESD) measures device sensitivity and immunity to damage caused by assembly line electrostatic discharges
(2) JAEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification

8.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage at VIN, VINA	1.8		5.5	V
Operating junction temperature range, T_J	–40		125	°C

8.4 Thermal Information

THERMAL METRIC(1)		TPS63020-Q1 DSJ (VSON) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

V_{IN} = 1.8 V to 5.5 V, T_J = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC/DC STAGE							
V_{IN}	Input voltage range			1.8		5.5	V
	Minimum input voltage for startup		0°C ≤ T_A ≤ 85°C	1.5	1.8	1.9	V
	Minimum input voltage for startup			1.5	1.8	2.0	V
V_{OUT}	TPS63020 output voltage range			1.2		5.5	V
	Duty cycle in step down conversion			20%			
V_{FB}	TPS63020 feedback voltage		PS/SYNC = VIN	495	500	505	mV
V_{FB}	TPS63020 feedback voltage		PS/SYNC = GND referenced to 500 mV	0.6%		5%	
	Maximum line regulation				0.5%		
	Maximum load regulation				0.5%		
f	Oscillator frequency			2200	2400	2600	kHz
	Frequency range for synchronization		2.0 V ≤ V_{IN} ≤ 5.5 V	2200	2400	2600	kHz
I_{SW}	Average switch current limit		V_{IN} = V_{INA} = 3.6 V, T_J = 25°C	3500	4000	4500	mA
	High side switch on resistance		V_{IN} = V_{INA} = 3.6 V		50		mΩ
	Low side switch on resistance		V_{IN} = V_{INA} = 3.6 V		50		mΩ
I_q	Quiescent current	VIN and VINA	I_O = 0 mA, V_{EN} = V_{IN} = V_{INA} = 3.6 V, V_{OUT} = 3.3 V, -40°C ≤ T_J ≤ 85°C		25	50	µA
		VOUT			5	10	µA
I_S	Shutdown current		V_{EN} = 0 V, V_{IN} = V_{INA} = 3.6 V, –40°C ≤ T_J ≤ 85°C		0.1	1	µA
CONTROL STAGE							
UVLO	Under voltage lockout threshold		V_{INA} voltage decreasing	1.4	1.5	1.6	V
	Under voltage lockout hysteresis				200		mV
V_{IL}	EN, PS/SYNC input low voltage					0.4	V
V_{IH}	EN, PS/SYNC input high voltage			1.2			V
	EN, PS/SYNC input current		Clamped to GND or VINA		0.01	0.2	µA
	PG output low voltage		V_{OUT} = 3.3 V, I_{PGL} = 10 µA		0.04	0.4	V
	PG output leakage current				0.01	0.1	µA
	Output overvoltage protection			5.5		7	V
	Overtemperature protection				140		°C
	Overtemperature hysteresis				20		°C

8.6 Typical Characteristics

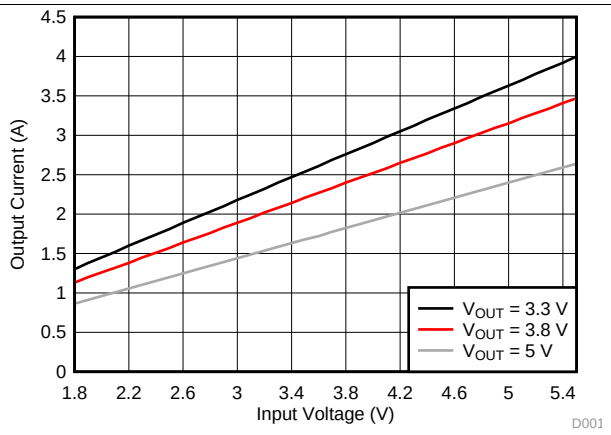


Figure 1. Output Current vs Input Voltage at T_J= 125 °C

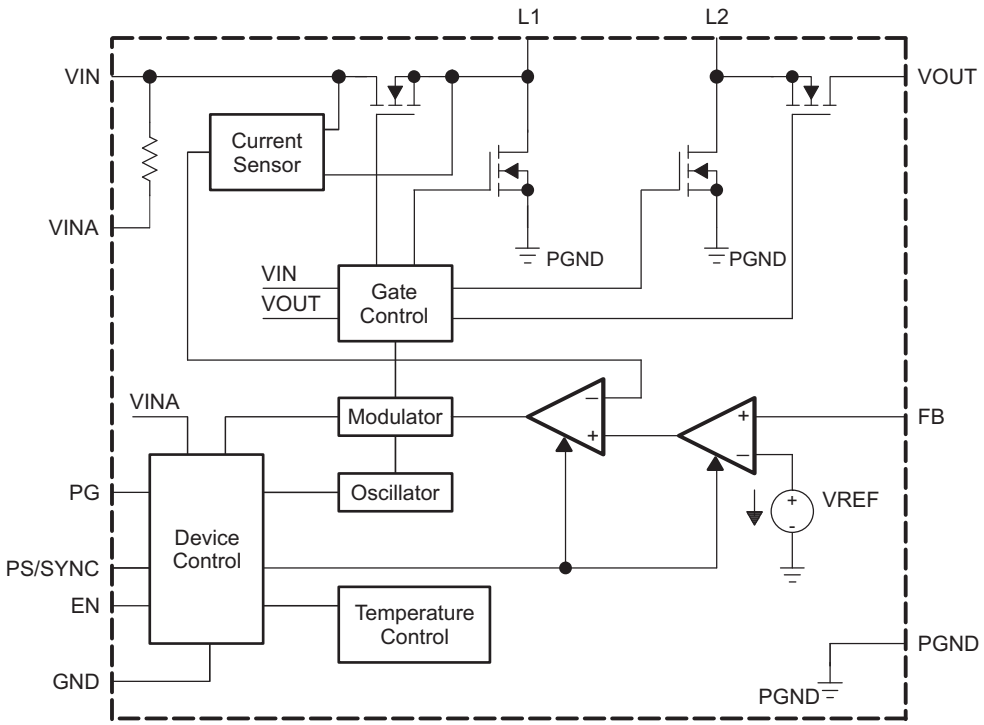
9 Detailed Description

9.1 Overview

The controller circuit of the device is based on an average current mode topology. The controller also uses input and output voltage feedforward. Changes of input and output voltage are monitored and immediately can change the duty cycle in the modulator to achieve a fast response to those errors. The voltage error amplifier gets its feedback input from the FB pin. At adjustable output voltages, a resistive voltage divider must be connected to that pin. At fixed output voltages, FB must be connected to the output voltage to directly sense the voltage. Fixed output voltage versions use a trimmed internal resistive divider. The feedback voltage will be compared with the internal reference voltage to generate a stable and accurate output voltage.

The device uses 4 internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over a wide input voltage and output power range. To avoid ground shift problems due to the high currents in the switches, two separate ground pins GND and PGND are used. The reference for all control functions is the GND pin. The power switches are connected to PGND. Both grounds must be connected on the PCB at only one point, ideally, close to the GND pin. Due to the 4-switch topology, the load is always disconnected from the input during shutdown of the converter. To protect the device from overheating an internal temperature sensor is implemented.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Dynamic Voltage Positioning

As detailed in Figure 3, the output voltage is typically 3% above the nominal output voltage at light load currents, as the device is in power save mode. This gives additional headroom for the voltage drop during a load transient from light load to full load. This allows the converter to operate with a small output capacitor and still have a low absolute voltage drop during heavy load transient changes. See Figure 3 for detailed operation of the power save mode.

Feature Description (continued)

9.3.2 Dynamic Current Limit

To protect the device and the application, the average inductor current is limited internally on the IC. At nominal operating conditions, this current limit is constant. The current limit value can be found in the electrical characteristics table. If the supply voltage at VIN drops below 2.3 V, the current limit is reduced. This can happen when the input power source becomes weak. Increasing output impedance, when the batteries are almost discharged, or an additional heavy pulse load is connected to the battery can cause the VIN voltage to drop. The dynamic current limit has its lowest value when reaching the minimum recommended supply voltage at VIN. At this voltage, the device is forced into burst mode operation trying to stay active as long as possible even with a weak input power source.

If the die temperature increases above the recommended maximum temperature, the dynamic current limit becomes active. Similar to the behavior when the input voltage at VIN drops, the current limit is reduced with temperature increasing.

9.3.2.1 Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is disconnected from the input. This means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents flowing from the input.

9.3.2.2 Power Good

The device has a built in power good function to indicate whether the output voltage is regulated properly. As soon as the average inductor current gets limited to a value below the current the voltage regulator demands for maintaining the output voltage the power good output gets low impedance. The output is open drain, so its logic function can be adjusted to any voltage level the connected logic is using, by connecting a pull up resistor to the supply voltage of the logic. By monitoring the status of the current control loop, the power good output provides the earliest indication possible for an output voltage break down and leaves the connected application a maximum time to safely react.

9.3.2.3 Overvoltage Protection

If, for any reason, the output voltage is not fed back properly to the input of the voltage amplifier, control of the output voltage will not work anymore. Therefore overvoltage protection is implemented to avoid the output voltage exceeding critical values for the device and possibly for the system it is supplying. The implemented overvoltage protection circuit monitors the output voltage internally as well. In case it reaches the overvoltage threshold the voltage amplifier regulates the output voltage to this value.

9.3.2.4 Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage at VINA is lower than approximately its threshold (see electrical characteristics table). When in operation, the device automatically enters the shutdown mode if the voltage at VINA drops below the undervoltage lockout threshold. The device automatically restarts if the input voltage recovers to the minimum operating input voltage.

9.3.2.5 Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC temperature. If the temperature exceeds the programmed threshold (see electrical characteristics table) the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. There is a built-in hysteresis to avoid unstable operation at IC temperatures at the overtemperature threshold.

9.4 Device Functional Modes

9.4.1 Softstart and Short Circuit Protection

After being enabled, the device starts operating. The average current limit ramps up from an initial 400 mA following the output voltage increasing. At an output voltage of about 1.2 V, the current limit is at its nominal value. If the output voltage does not increase, the current limit will not increase. There is no timer implemented. Thus, the output voltage overshoot at startup, as well as the inrush current, is kept at a minimum. The device ramps up the output voltage in a controlled manner even if a large capacitor is connected at the output. When the output voltage does not increase above 1.2 V, the device assumes a short circuit at the output, and keeps the current limit low to protect itself and the application. At a short on the output during operation, the current limit also is decreased accordingly.

9.4.2 Buck-Boost Operation

To regulate the output voltage at all possible input voltage conditions, the device automatically switches from step down operation to boost operation and back as required by the configuration. It always uses one active switch, one rectifying switch, one switch permanently on, and one switch permanently off. Therefore, it operates as a step down converter (buck) when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all 4 switches are permanently switching. Controlling the switches this way allows the converter to maintain high efficiency at the most important point of operation, when input voltage is close to the output voltage. The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses. For the remaining 2 switches, one is kept permanently on and the other is kept permanently off, thus causing no switching losses.

9.4.3 Control Loop

The controller circuit of the device is based on an average current mode topology. The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. Figure 2 shows the control loop.

The non inverting input of the transconductance amplifier, gmv, is assumed to be constant. The output of gmv defines the average inductor current. The inductor current is reconstructed by measuring the current through the high side buck MOSFET. This current corresponds exactly to the inductor current in boost mode. In buck mode the current is measured during the on time of the same MOSFET. During the off time, the current is reconstructed internally starting from the peak value at the end of the on time cycle. The average current and the feedback from the error amplifier gmv forms the correction signal gmc. This correction signal is compared to the buck and the boost sawtooth ramp giving the PWM signal. Depending on which of the two ramps the gmc output crosses either the Buck or the Boost stage is initiated. When the input voltage is close to the output voltage, one buck cycle is always followed by a boost cycle. In this condition, no more than three cycles in a row of the same mode are allowed. This control method in the buck-boost region ensures a robust control and the highest efficiency.

The Buck-Boost Overlap Control™ makes sure that the classical buck-boost function, which would cause two switches to be on every half a cycle, is avoided. Thanks to this block whenever all switches becomes active during one clock cycle, the two ramps are shifted away from each other, on the other hand when there is no switching activities because there is a gap between the ramps, the ramps are moved closer together. As a result the number of classical buck-boost cycles or no switching is reduced to a minimum and high efficiency values has been achieved.

Device Functional Modes (continued)

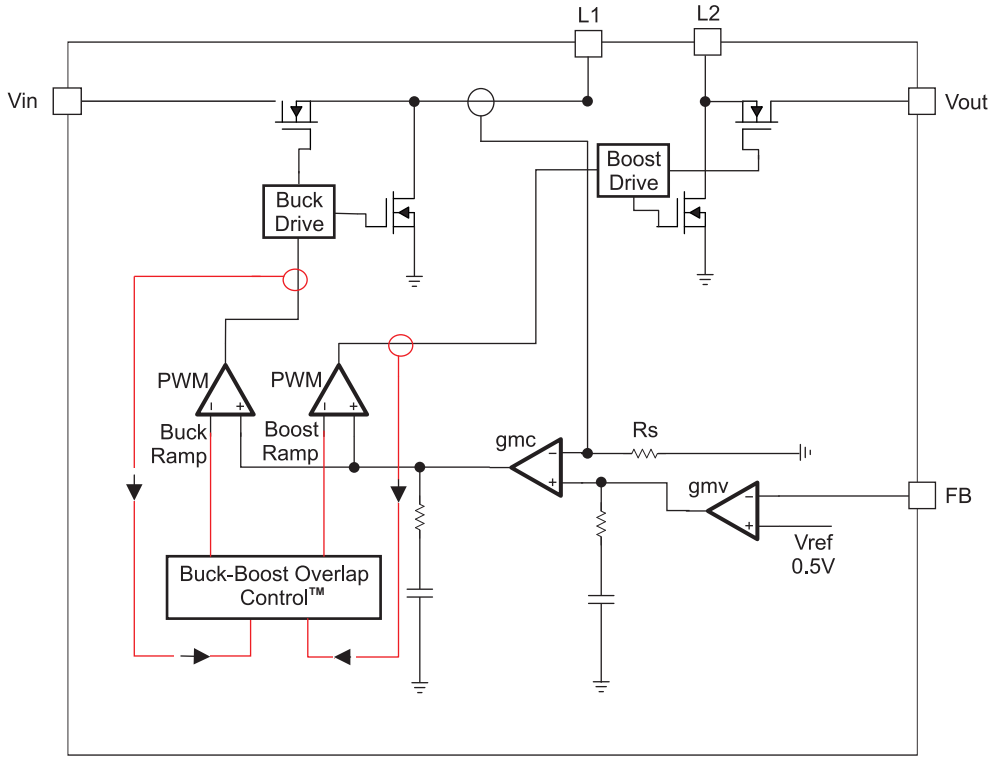


Figure 2. Average Current Mode Control

9.4.4 Power Save Mode and Synchronization

The PS/SYNC pin can be used to select different operation modes. Power save mode is used to improve efficiency at light load. To enable power-save, PS/SYNC must be set low. If PS/SYNC is set low then power save mode is entered when the average inductor current gets lower then about 100 mA. At this point the converter operates with reduced switching frequency and with a minimum quiescent current to maintain high efficiency.

During the power save mode, the output voltage is monitored with a comparator by the threshold comp low and comp high. When the device enters power save mode, the converter stops operating and the output voltage drops. The slope of the output voltage depends on the load and the value of output capacitance. As the output voltage falls below the comp low threshold set to 2.5% typical above V_{OUT}, the device ramps up the output voltage again, by starting operation using a programmed average inductor current higher than required by the current load condition. Operation can last one or several pulses. The converter continues these pulses until the comp high threshold, set to typically 3.5% above V_{OUT} nominal, is reached and the average inductance current gets lower than about 100 mA. When the load increases above the minimum forced inductor current of about 100 mA, the device will automatically switch to PWM mode.

The power save mode can be disabled by programming high at the PS/SYNC. Connecting a clock signal at PS/SYNC forces the device to synchronize to the connected clock frequency.

Synchronization is done by a PLL, so synchronizing to lower and higher frequencies compared to the internal clock works without any issues. The PLL can also tolerate missing clock pulses without the converter malfunctioning. The PS/SYNC input supports standard logic thresholds.

Device Functional Modes (continued)

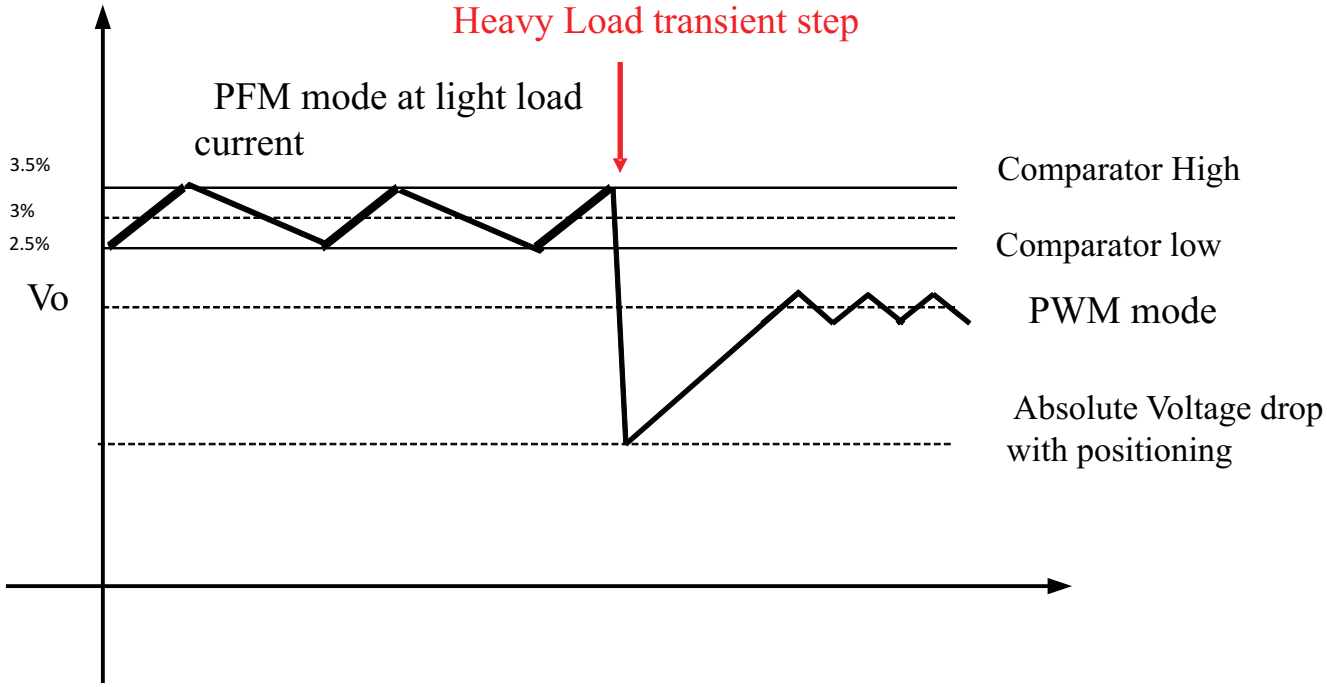


Figure 3. Power Save Mode Thresholds and Dynamic Voltage Positioning

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS63020-Q1 is a high efficiency, low quiescent current buck-boost converter suitable for applications where the input voltage is higher or lower than the output voltage. Continuous output current can go as high as 2 A in boost mode and as high as 4 A in buck mode. The maximum average current in the switches is limited to a typical value of 4 A.

10.2 Typical Application

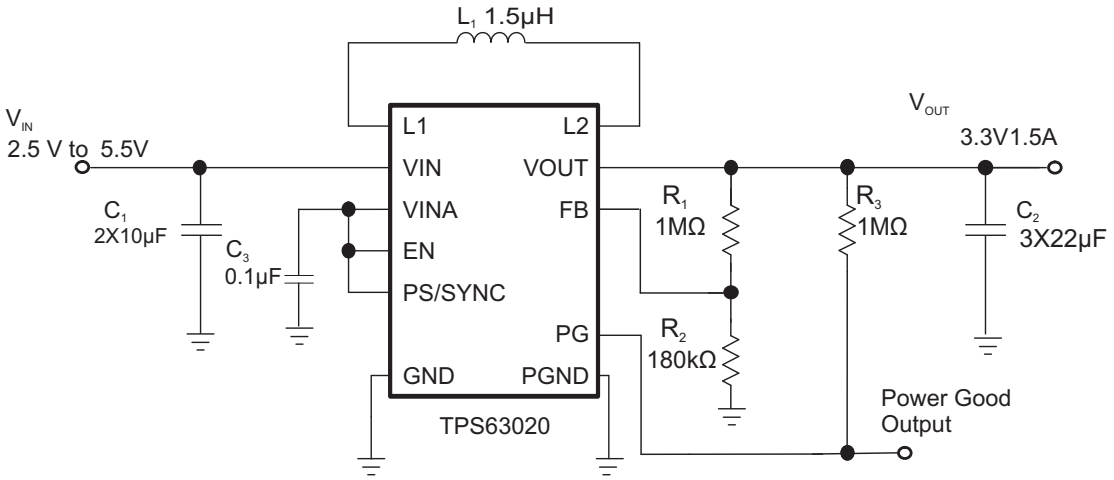


Figure 4. Application Circuit

10.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the operating conditions specified on the Application Circuit schematic.

Table 1 shows the list of components for the Application Characteristic Curves.

Table 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
	TPS63020	Texas Instruments
L1	1.5 µH, 4 mm x 4 mm x 2 mm	XFL4020-152ML, Coilcraft
C1	2 × 10 µF 6.3V, 0603, X5R ceramic	GRM188R60J106ME84D, Murata
C2	3 × 22 µF 6.3V, 0603, X5R ceramic	GRM188R60J226MEAOL Murata
C3	0.1 µF, X5R or X7R ceramic	
R1	Depending on the output voltage at TPS63020	
R2	Depending on the output voltage at TPS63020	
R3	1 MΩ	

10.2.2 Detailed Design Procedure

The TPS63020-Q1 series of buck-boost converter has internal loop compensation. Therefore, the external L-C filter has to be selected to work with the internal compensation. As a general rule of thumb, the product L x C should not move over a wide range when selecting a different output filter. However, when selecting the output filter a low limit for the inductor value exists to avoid subharmonic oscillation which could be caused by a far too fast ramp up of the amplified inductor current. For the TPS63020-Q1 series the minimum inductor value should be kept at 1 uH.

In particular either 1 µH or 1.5 µH is recommended working at output current between 1.5 A and 2 A. If operating with lower load current is also possible to use 2.2 µH.

Selecting a larger output capacitor value is less critical because the corner frequency moves to lower frequencies.

10.2.2.1 Inductor Selection

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady state operation is calculated using Equation 6. Only the equation which defines the switch current in boost mode is shown, because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \qquad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{1}$$

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L} \tag{2}$$

where

- D =Duty Cycle in Boost mode
- f = Converter switching frequency (typical 2.5MHz)
- L = Inductor value
- η = Estimated converter efficiency (use the number from the efficiency curves or 0.90 as an assumption)
- **Note:** The calculation must be done for the minimum input voltage possible in boost mode

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It's recommended to choose an inductor with a saturation current 20% higher than the value calculated using Equation 2. Possible inductors are listed in Table 2.

Table 2. Inductor Selection(1)

VENDOR	INDUCTOR SERIES
Coilcraft	XFL4020
Toko	FDV0530S

(1) See Third-party Products Disclaimer

10.2.2.2 Capacitor Selection

10.2.2.2.1 *Input Capacitor*

At least a 10 µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended.

10.2.2.2.2 *Output Capacitor*

For the output capacitor, use of a small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC is recommended. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor should be placed as close as possible to the VOUT and PGND pins of the IC. The recommended typical output capacitor value is 30 µF with a variance that depends on the specific application requirements.

There is also no upper limit for the output capacitance value. Larger capacitors will cause lower output voltage ripple as well as lower output voltage drop during load transients.

When choosing input and output capacitors, it needs to be kept in mind, that the value of capacitance experiences significant losses from their rated value depending on the operating temperature and the operating DC voltage. It is not uncommon for a small surface mount ceramic capacitor to lose 50% and more of its rated capacitance. For this reason it could be important to use a larger value of capacitance or a capacitor with higher voltage rating in order to ensure the required capacitance at the full operating voltage.

10.2.2.2.3 *Bypass Capacitor*

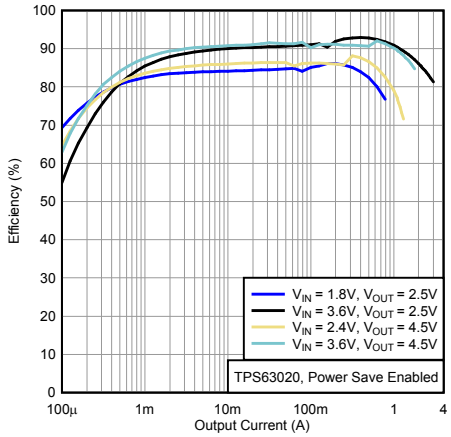
To make sure that the internal control circuits are supplied with a stable low noise supply voltage, a capacitor can be connected between VINA and GND. Using a ceramic capacitor with a value of 0.1 µF is recommended. The value of this capacitor should not be higher than 0.22 µF.

10.2.2.3 Setting the Output Voltage

The feedback resistor divider must be connected between VOUT, FB and GND. When the output voltage is regulated, the typical value of the voltage at the FB pin is 500 mV. The maximum recommended value for the output voltage is 8 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 µA, and the voltage across the resistor between FB and GND, R_2, is typically 500 mV. Based on these two values, the recommended value for R2 should be lower than 500 kΩ, in order to set the divider current at 1 µA or higher. It is recommended to keep the value for this resistor in the range of 200 kΩ. From that, the value of the resistor connected between VOUT and FB, R_1, depending on the needed output voltage (V_{OUT}), can be calculated using Equation 3:

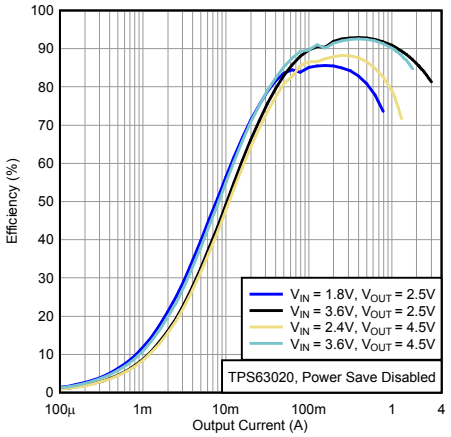
$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (3)$$

10.2.3 Application Curves



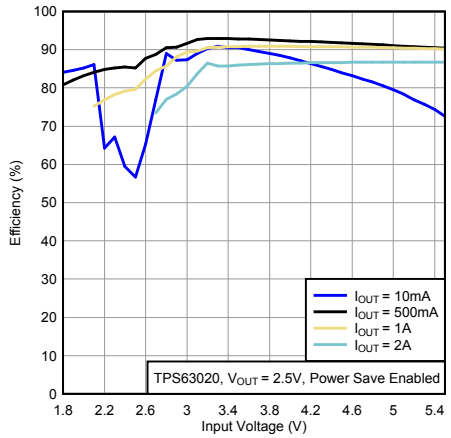
PS/SYNC = Low V_{OUT} = 2.5 V, 4.5 V

Figure 5. Efficiency vs Output Current, Power Save Enabled



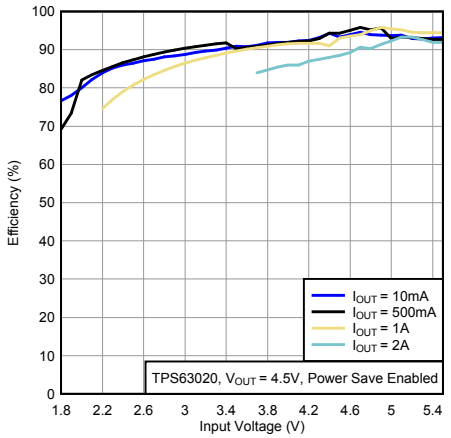
PS/SYNC = High V_{OUT} = 2.5 V, 4.5 V

Figure 6. Efficiency vs Output Current, Power Save Disabled



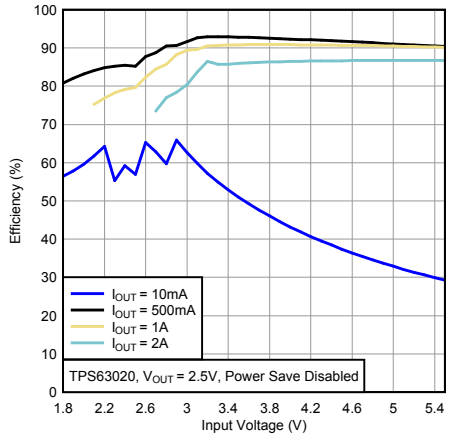
PS/SYNC = Low V_{OUT} = 2.5 V

Figure 7. Efficiency vs Input Voltage, Power Save Enabled



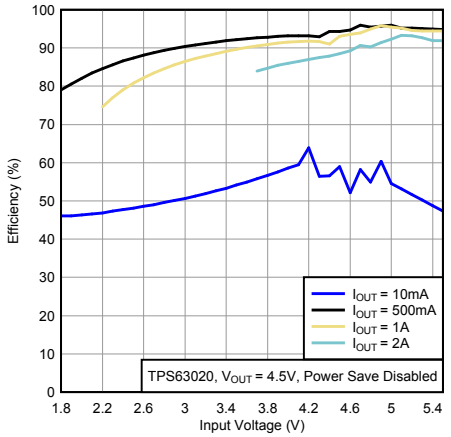
PS/SYNC = Low V_{OUT} = 4.5 V

Figure 8. Efficiency vs Input Voltage, Power Save Enabled



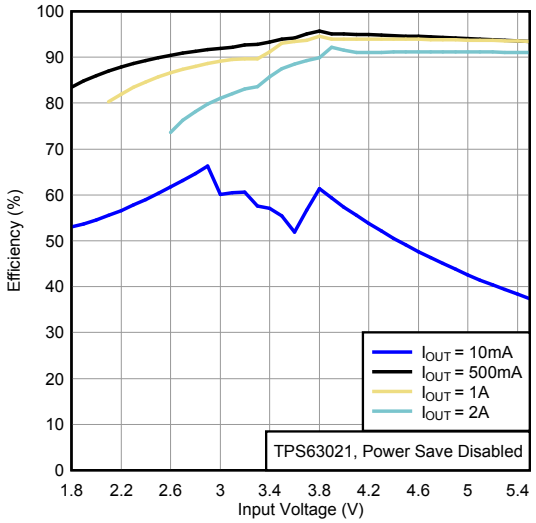
PS/SYNC = High V_{OUT} = 2.5 V

Figure 9. Efficiency vs Input Voltage, Power Save Disabled



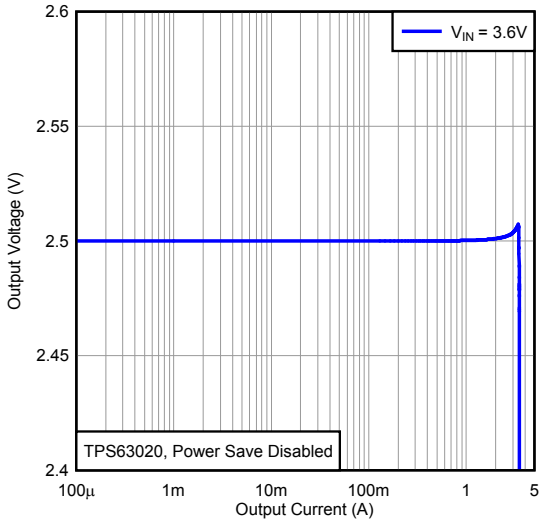
PS/SYNC = High V_{OUT} = 4.5 V

Figure 10. Efficiency vs Input Voltage, Power Save Disabled



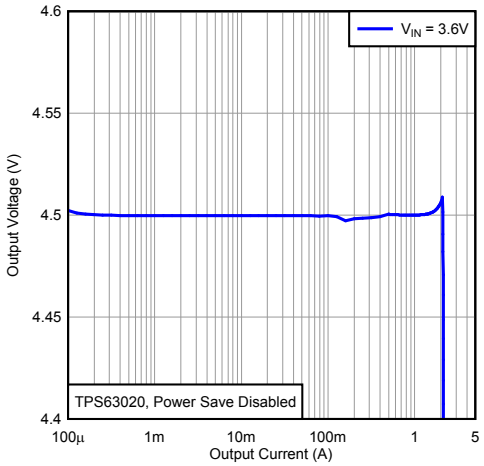
PS/SYNC = High V_{OUT} = 2.5 V, 4.5 V

Figure 11. Efficiency vs Input Voltage, Power Save Disabled



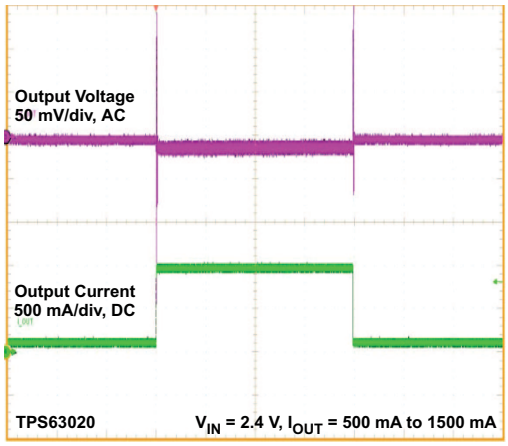
PS/SYNC = High V_{OUT} = 2.5 V

Figure 12. Load Transient Response



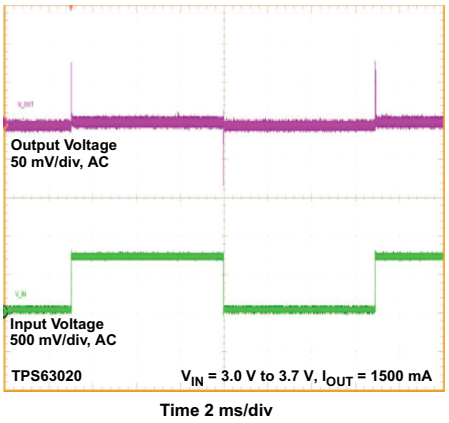
PS/SYNC = High V_{OUT} = 4.5 V

Figure 13. Load Transient Response



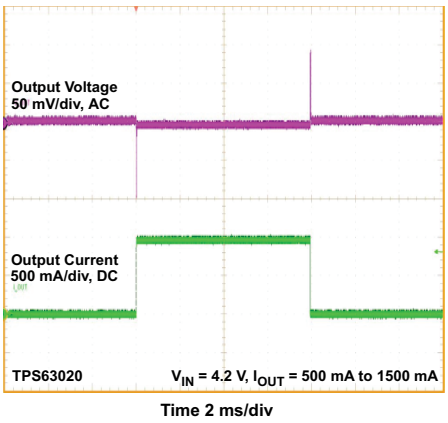
PS/SYNC = High V_{OUT} = 3.3V

Figure 14. Load Transient Response



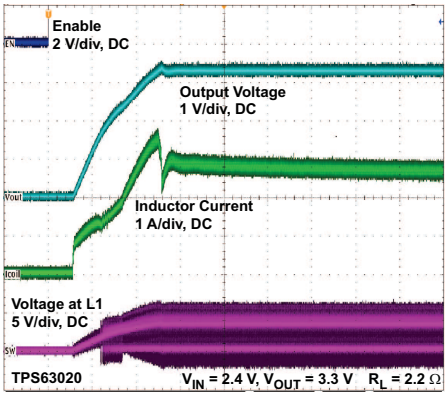
PS/SYNC = High V_{OUT} = 3.3V

Figure 15. Load Transient Response



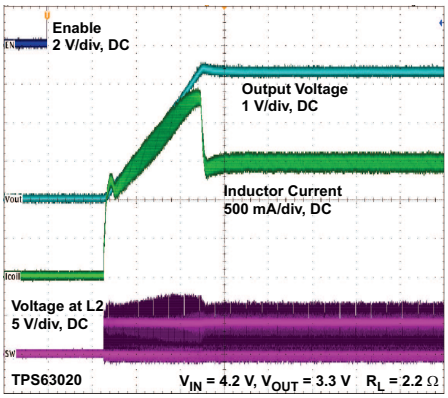
PS/SYNC = High V_{OUT} = 3.3V

Figure 16. Line Transient Response



PS/SYNC = High V_{OUT} = 3.3V

Figure 17. Startup After Enable



PS/SYNC = High V_{OUT} = 3.3V

Figure 18. Startup After Enable

10.3 System Examples

10.3.1 2-A Load Current

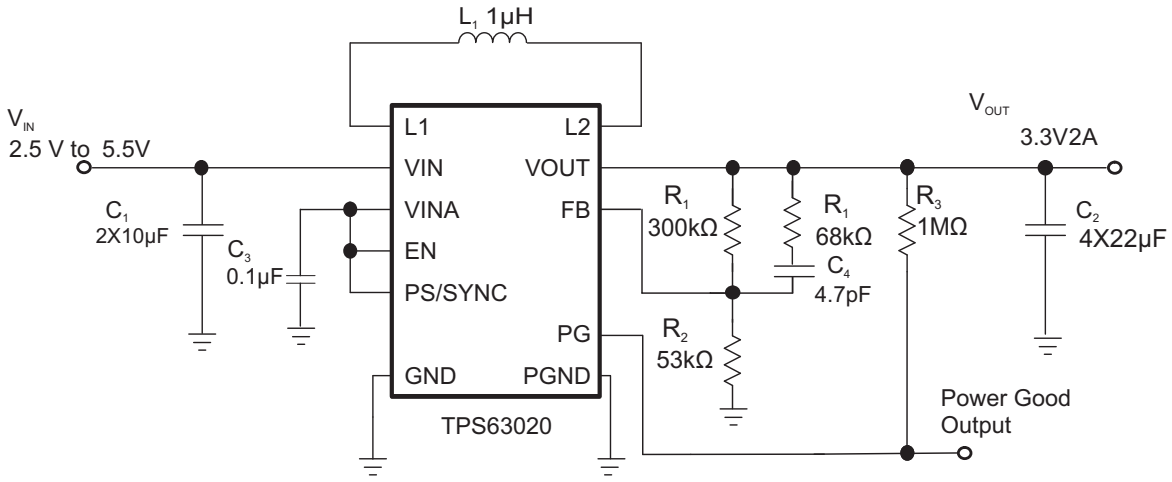


Figure 19. Application Circuit for 2A Load Current

Capacitor C4 and resistor R1 are added for improved load transient performance..

11 Power Supply Recommendations

The TPS63020-Q1 device has no special requirements for its input power supply.

The output current of the power supply must be rated according to the supply voltage, output voltage and output current of the TPS63020-Q1.

12 Layout

12.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, short traces are recommended as well, separation from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

12.2 Layout Example

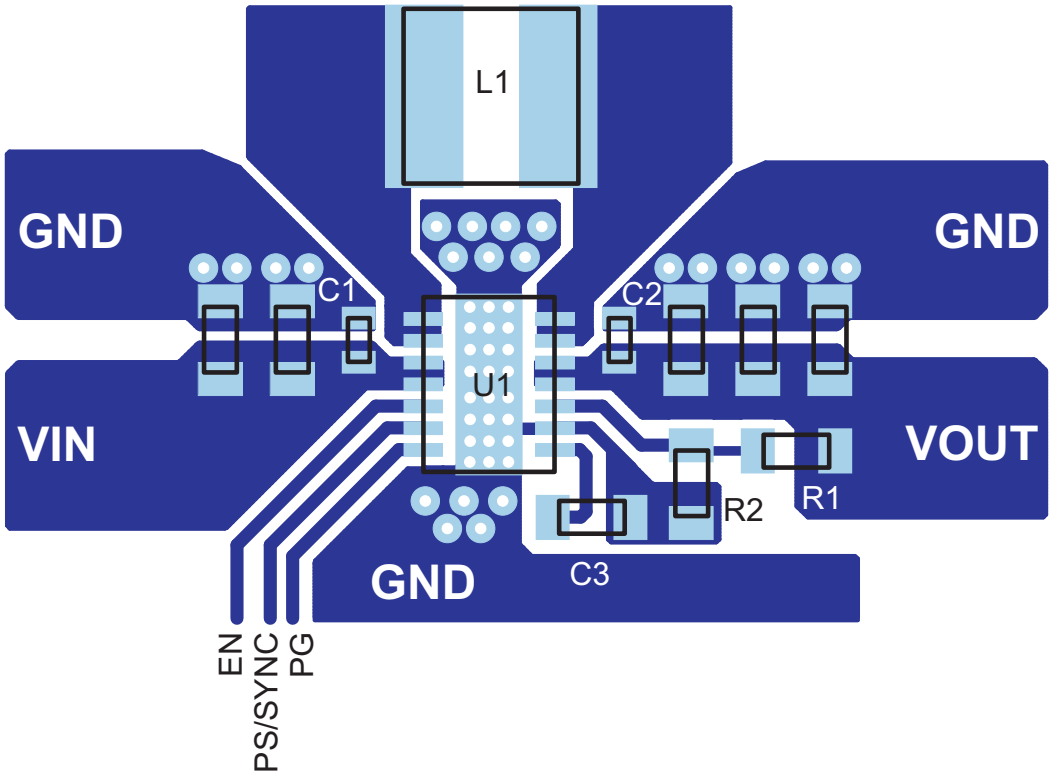


Figure 20. PCB Layout Suggestion

12.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the exposed thermal pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: *Thermal Characteristics Application Note* (SZZA017), and *Semiconductor and IC Package Thermal Metrics Application Note* (SPRA953).

13 器件和文档支持

13.1 器件支持

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13.2 文档支持

13.2.1 相关文档

相关文档请参见以下部分：

- *《散热特性数据应用手册》*（文献编号：SZZA017）
- *《IC 封装热指标应用手册》*（文献编号：SPRA953）

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13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS63020QDSJRQ1	ACTIVE	VSON	DSJ	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	63020Q	Samples
TPS63020QDSJTQ1	ACTIVE	VSON	DSJ	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	63020Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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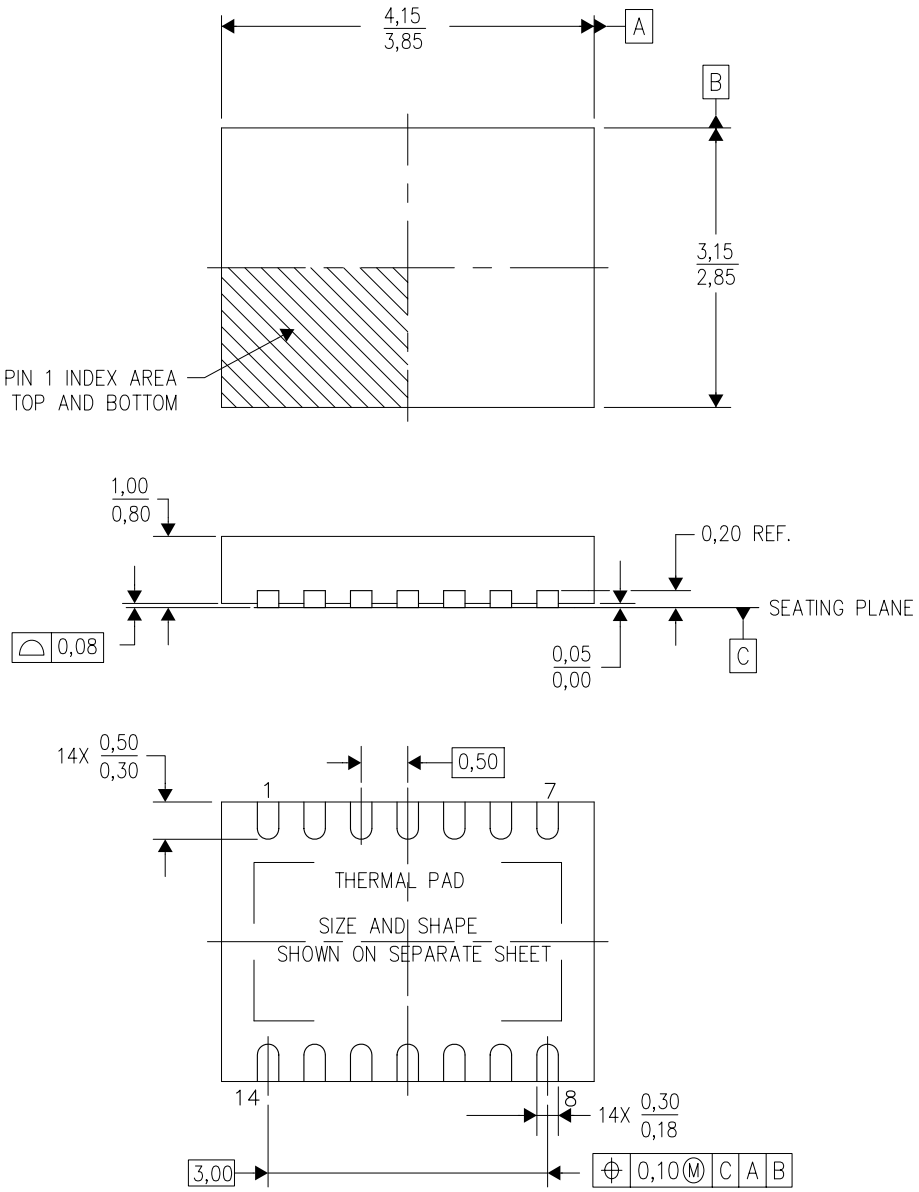
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

DSJ (R–PVSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

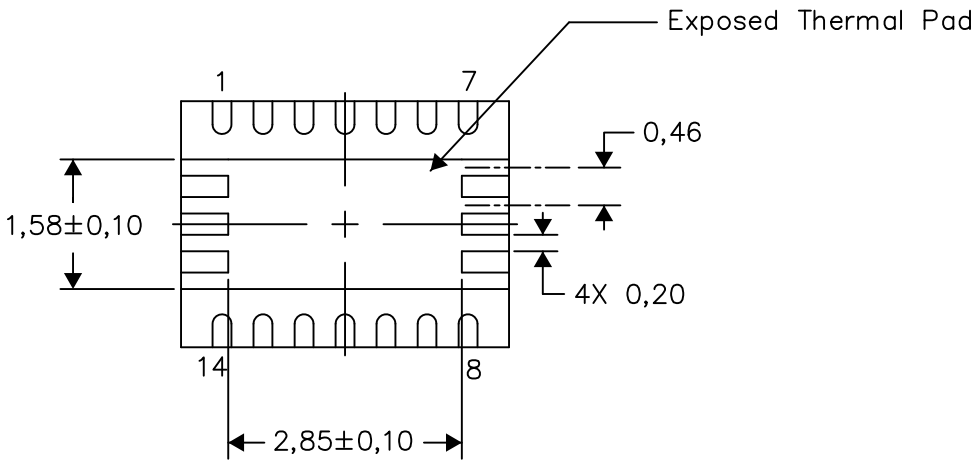
DSJ (R–PVSON–N14) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



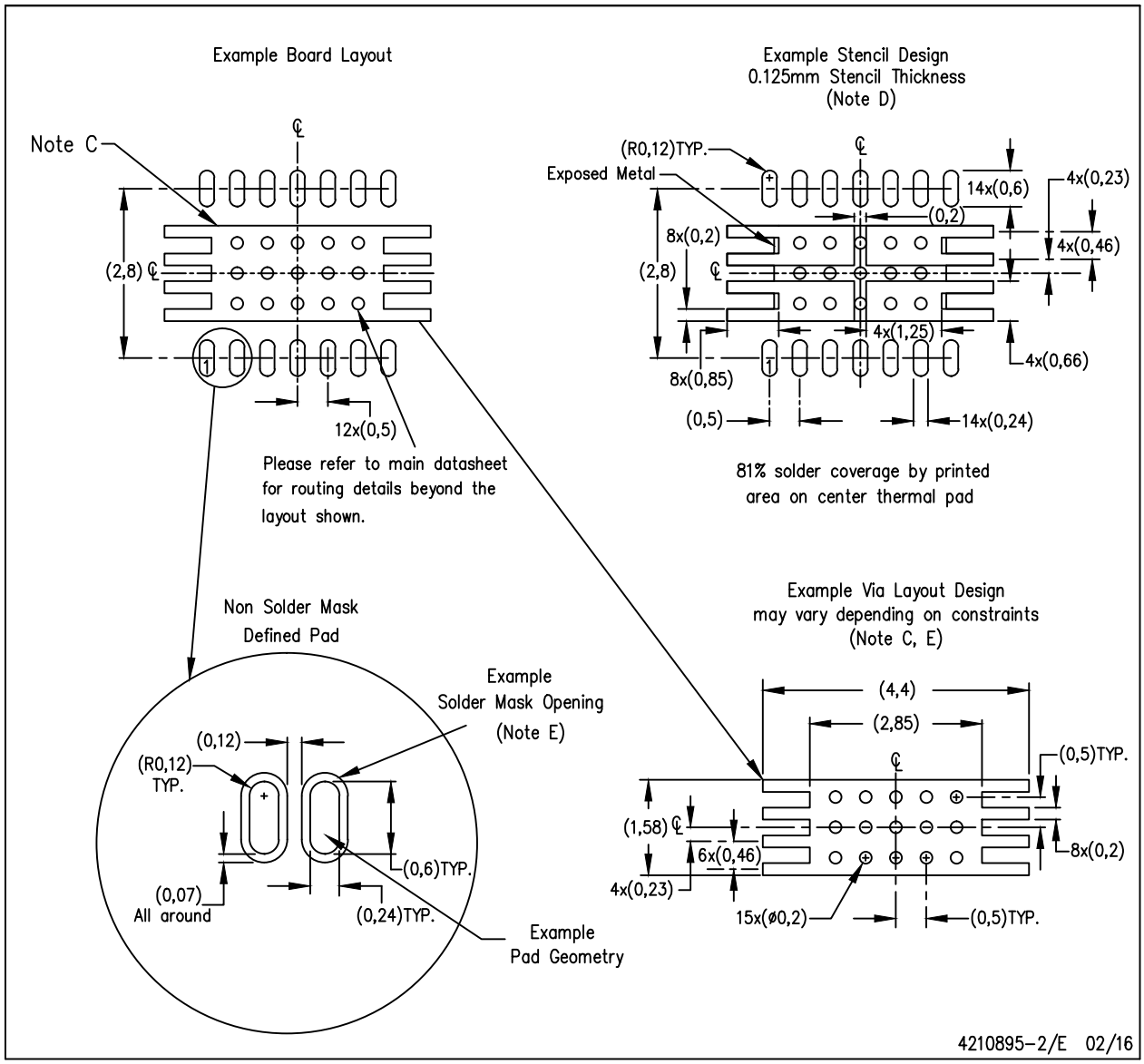
Bottom View

Exposed Thermal Pad Dimensions

4208549–3/G 04/15

NOTE: All linear dimensions are in millimeters

DSJ (R–PVSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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