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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

$T_A$	PACKAGE MARKING	PACKAGE <sup>(1)</sup>	PART NUMBER
-35°C to 85°C	BPR	16-pin QFN	TPS65560RGT

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

			UNIT
$V_{SS}$	Supply voltage	VCC	-0.6 V to 6 V
		VBAT	-0.6 V to 13 V
$V_{(SW)}$	Switch terminal voltage		-0.6 V to 50 V
$I_{(SW)}$	Switch current between SW and PGND, ISW		3 A
$V_I$	Input voltage of CHG, I_PEAK, F_ON		-0.3 V to $V_{CC}$
$T_{stg}$	Storage temperature		-40°C to 150°C
$T_J$	Maximum junction temperature		125°C
	ESD rating	HBM (Human Body Model) JEDEC JES22-A114	1 kV

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
$V_{SS}$	Supply voltage, VCC	2.7		4	V
	Supply voltage, VBAT	1.6		12	V
$V_{(SW)}$	Switch terminal voltage,	-0.3		45	V
$I_{(SW)}$	Switch current between SW and PGND			2	A
	Operating free-air temperature range	-35		85	°C
$V_{IH}$	High-level digital input voltage at CHG and F_ON	2			V
$V_{IL}$	Low-level digital input voltage at CHG and F_ON			0.5	V

## DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$ <sup>(1)</sup>	POWER RATING $T_A < 25^\circ\text{C}$	POWER RATING $T_A = 70^\circ\text{C}$	POWER RATING $T_A = 85^\circ\text{C}$
QFN	47.4 °C/W	2.11 W	1.16 W	844 mW

(1) The thermal resistance,  $R_{\theta JA}$ , is based on a soldered PowerPAD™ on a 2S2P JEDEC board using thermal vias.

## ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_{BAT} = 4.2\text{ V}$ ,  $V_{CC} = 3\text{ V}$ ,  $V_{(SW)} = 4.2\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
R <sub>(ONL)</sub>	ON resistance of XFULL	I <sub>(XFULL)</sub> = -1 mA	1.5	3	kΩ	
V <sub>(PKH)</sub> <sup>(1)</sup>	Upper threshold voltage of I <sub>_PEAK</sub>	V <sub>CC</sub> = 3 V	2.4		V	
V <sub>(PKL)</sub> <sup>(1)</sup>	Lower threshold voltage of I <sub>_PEAK</sub>	V <sub>CC</sub> = 3 V		0.6	V	
I <sub>CC1</sub>	Supply current from VBAT	CHG = H, V <sub>(SW)</sub> = 0 V (free run by t <sub>MAX</sub> )	17	50	μA	
I <sub>CC2</sub>	Supply current from VCC	CHG = H, V <sub>(SW)</sub> = 0 V (free run by t <sub>MAX</sub> )	1.3	3	mA	
I <sub>CC3</sub>	Supply current from VCC and VBAT	CHG = L		1	μA	
I <sub>lk1</sub>	Leakage current of SW terminal			2	μA	
I <sub>lk2</sub>	Leakage current of XFULL terminal	V <sub>(XFULL)</sub> = 5 V		1	μA	
I <sub>(sink)</sub>	Sink current at I <sub>_PEAK</sub>	V <sub>(I<sub>_PEAK</sub>)</sub> = 3 V, CHG: High		2	μA	
		V <sub>(I<sub>_PEAK</sub>)</sub> = 3 V, CHG: Low		0.1		
R <sub>(ONSW)</sub>	SW ON resistance between SW and PGND	I <sub>(SW)</sub> = 1 A, V <sub>CC</sub> = 3 V	0.4	0.9	Ω	
R <sub>(IGBT1)</sub>	G_IGBT pullup resistance	V <sub>(G_IGBT)</sub> = 0 V, V <sub>CC</sub> = 3 V	8	12	19.4	Ω
R <sub>(IGBT2)</sub>	G_IGBT pulldown resistance	V <sub>(G_IGBT)</sub> = 3 V, V <sub>CC</sub> = 3 V	36	53	70	Ω
I <sub>(PEAK1)</sub>	Upper peak of I <sub>(SW)</sub>	V <sub>(I<sub>_IPEAK</sub>)</sub> = 3 V	1.58	1.68	1.78	A
I <sub>(PEAK2)</sub>	Lower peak of I <sub>(SW)</sub>	V <sub>(I<sub>_IPEAK</sub>)</sub> = 0 V	0.7	0.8	0.9	A
V <sub>(FULL)</sub>	Charge completion detect voltage at V <sub>(SW)</sub>	VBAT = 1.6V, V <sub>CC</sub> = 3 V	28	28.7	29.4	V
		V <sub>CC</sub> = 3 V	28.6	29	29.4	
V <sub>(ZERO)</sub>	Zero current detection at V <sub>(SW)</sub>		1	20	60	mV
T <sub>(SD)</sub> <sup>(1)</sup>	Thermal shutdown temperature		150	160	170	°C
	Over V <sub>DS</sub> detection at V <sub>(SW)</sub>		0.95	1.2	1.45	V
t <sub>MIN</sub>	MAX OFF time		25	50	80	μs
t <sub>MAX</sub>	MAX ON time		50	100	160	μs
R <sub>(INPD)</sub>	Pulldown resistance of CHG, F_ON	VCHG = V <sub>(F_ON)</sub> = 4.2 V		100		kΩ

(1) Specified by design.

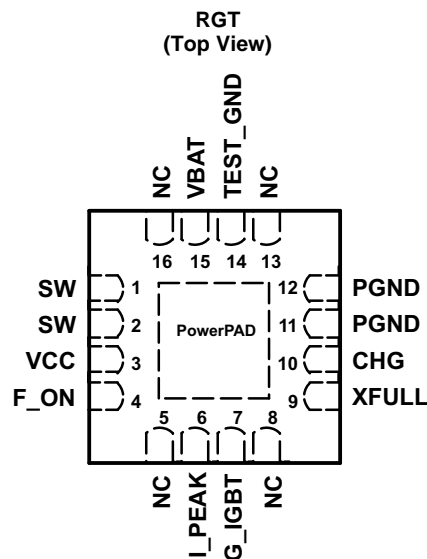
## SWITCHING CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_{BAT} = 4.2\text{ V}$ ,  $V_{CC} = 3\text{ V}$ ,  $V_{(SW)} = 4.2\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD}^{(1)}$	Propagation delay				
	F_ON $\uparrow$ - G_IGBT $\uparrow$		50		ns
	SW ON after $V_{(SW)}$ dips from $V_{(ZERO)}$		45		ns
	SW OFF after $I_{(SW)}$ exceeds $I_{(PEAK)}$		270		ns
	XFULL $\downarrow$ after $V_{(SW)}$ exceeds $V_{(FULL)}$		400		ns
	SW ON after CHG $\uparrow$		12		$\mu\text{s}$
	SW OFF after CHG $\downarrow$		20		ns

(1) Specified by design.

## PIN ASSIGNMENT



## TERMINAL FUNCTIONS

PIN NUMBER	SIGNAL	I/O	DESCRIPTION
1, 2	SW	O	Primary side switch. Connect SW to the switched side of the transformer
3	VCC	I	Power supply input. Connect VCC to an input supply from 2.7 V to 4 V. Bypass VCC to GND with a 1- $\mu$ F ceramic capacitor as close as possible to the IC.
4	F_ON	I	G_IGBT control input. Drives F_ON with the flash discharge signal. A logic high on F_ON drives G_IGBT high when CHG is Low. See the <i>IGBT Driver Control</i> section for details.
5, 8, 13, 16	NC		No internal connection
6	I_PEAK	I	Primary side peak current control input. The voltage at I_PEAK sets the peak current into SW. See the <i>Programming Peak Current</i> section for details on selecting $V_{(I\_PEAK)}$ .
7	G_IGBT	O	IGBT gate driver output. G_IGBT swings from PGND to VCC to drive external IGBT devices.
9	XFULL	O	Charge completion indicator output. XFULL is an open-drain output that pulls low once the output is fully charged. XFULL is high impedance during charging and all fault conditions. XFULL is reseted when CHG turns Low from High. See the <i>Indicating Charging Status</i> section for details.
10	CHG	I	Charge control input. Drive CHG high to initiate charging of the output. Drive CHG low to terminate charging.
11, 12	PGND		Power ground. Connect to the ground plane.
14	TEST_GND		Used by TI, should be connected to PGND and ground plane.
15	VBAT	I	Battery voltage monitor input. Connect VBAT to an input supply from 1.6 V to 12 V. Bypass VBAT to GND with a 10- $\mu$ F ceramic capacitor (C1 in <a href="#">Figure 1</a> , as close as possible to the battery) and a 1- $\mu$ F ceramic capacitor (C2 in <a href="#">Figure 1</a> , as close as possible to the IC).

## FUNCTIONAL BLOCK DIAGRAM

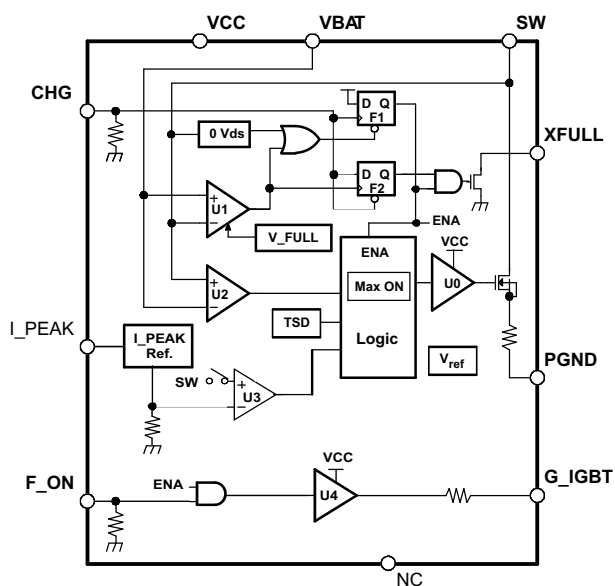


Figure 2. Functional Block Diagram

## I/O Equivalent Circuits

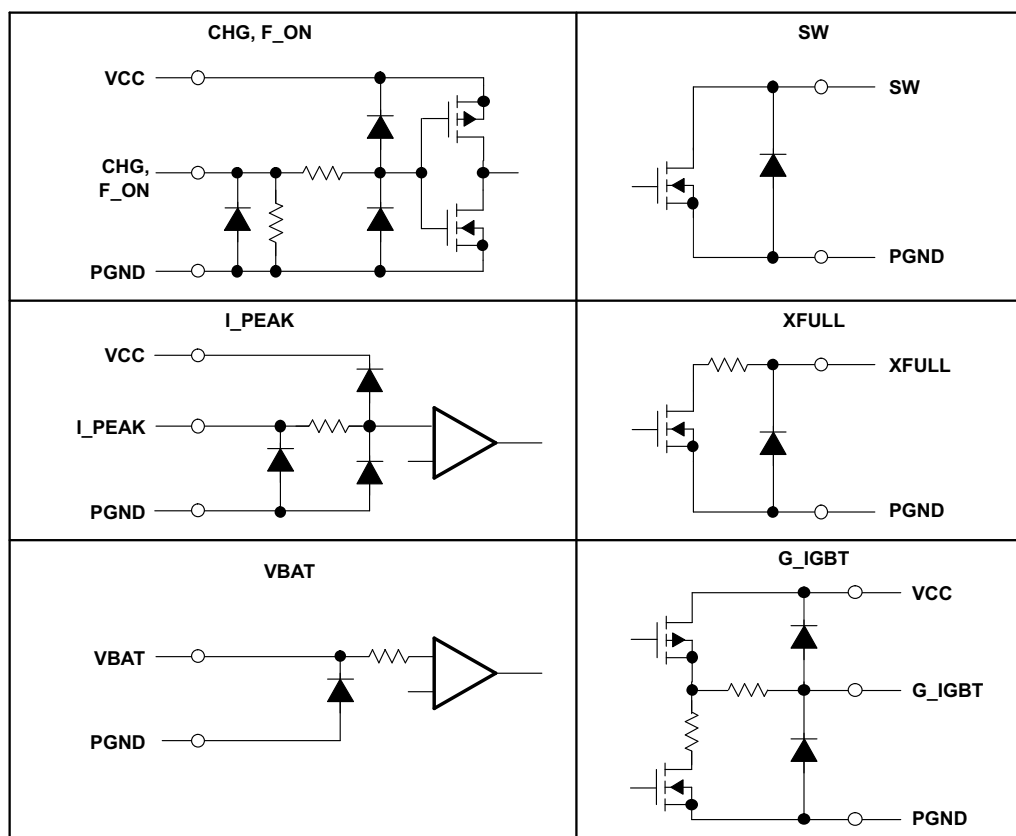


Figure 3. I/O Equivalent Circuits

## PRINCIPLES OF OPERATION

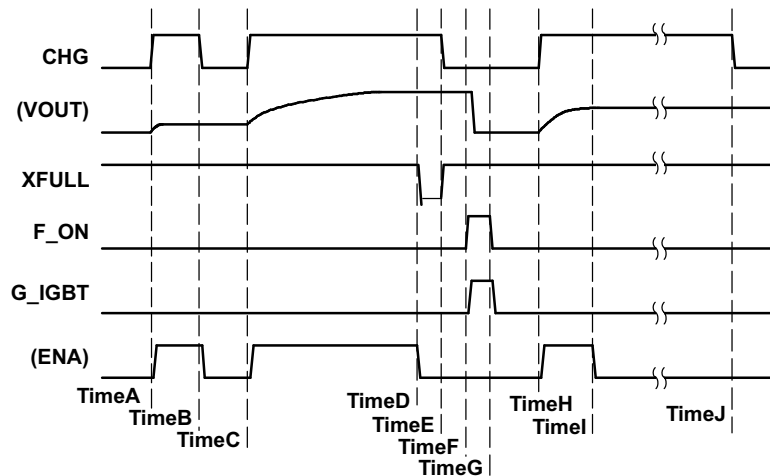


Figure 4. Whole Operation Sequence Chart

### Start/Stop Charging

TPS65560 has one internal enable latch, F1, that holds the charge enable (*ON/OFF* status) of the device. See [Figure 2](#).

The only way to *start* charging is to input  $\text{CHG}\uparrow$  (see time A/C/H in [Figure 4](#)). Each time  $\text{CHG}\uparrow$  is applied, the TPS65560 starts charging.

There are three trigger events to *stop* charging:

1. Forced *stop* by inputting  $\text{CHG} = \text{L}$  from the controller (see timeB in [Figure 4](#)).
2. Automatic *stop* by detecting a full charge. VOUT reaches the target value (see TimeD in [Figure 4](#)).
3. Protected *stop* by detecting an over current function ( $\text{OV}_{\text{DS}}$ ) trigger at SW pin (see TimeI in [Figure 4](#)).

### Indicating Charging Status

When the charging operation is complete, the TPS65560 drives the charge completion indicator pin, XFULL, to GND. A controller can detect the status of the device as a logic signal when connected through a pullup resistor, R1 (see [Figure 1](#)).

The XFULL output enables the controller to detect the  $\text{OV}_{\text{DS}}$  protection status. If  $\text{OV}_{\text{DS}}$  protection occurs, XFULL never goes L during  $\text{CHG} = \text{H}$ . Therefore, the controller detects  $\text{OV}_{\text{DS}}$  protection by measuring the time from CHG high to XFULL low. If the time to XFULL low is longer than the maximum designed charge time, then an  $\text{OV}_{\text{DS}}$  protection occurred.

The device starts charging at *timeH*, and  $\text{OV}_{\text{DS}}$  protection occurs at *TimeI* (see [Figure 4](#)). At *TimeI*, XFULL stays H. At *TimeJ*, the controller detects  $\text{OV}_{\text{DS}}$  protection through the expiration of a timer ends and then sets CHG to low to terminate the operation.

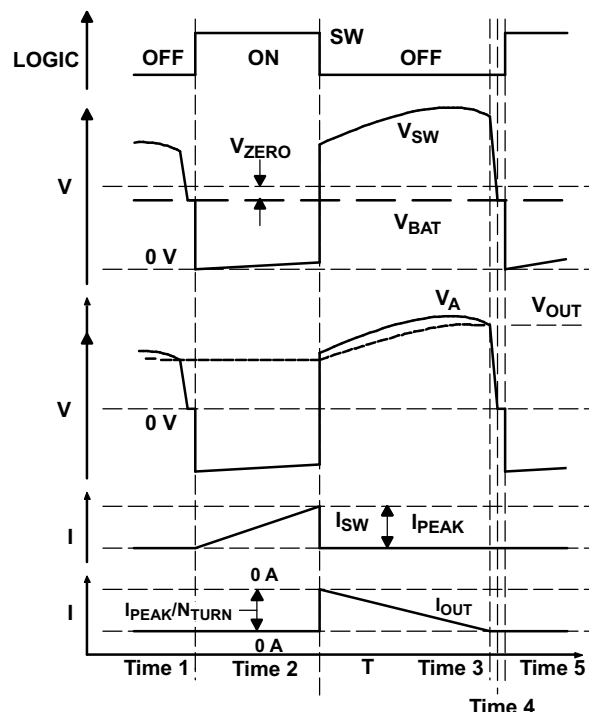


Figure 5. Timing Diagram at One Switching Cycle

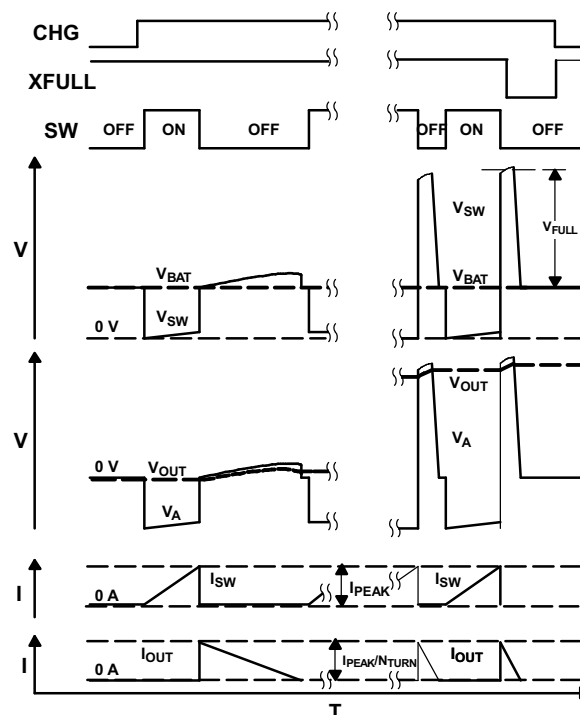


Figure 6. Timing Diagram at Beginning/Ending

## Control Charging

The TPS65560 provides three comparators to control charging. Figure 2 shows the block diagram of TPS65560 and Figure 5 shows a timing diagram of one switch cycle. Note that emphasis is placed on Time1 and Time3 of the waveform in Figure 5.

While SW is ON (Time1 to Time2 in Figure 5), U3 monitors current flow through the integrated power switch from SW pin to GND. When  $I_{(SW)}$  exceeds  $I_{(PEAK)}$ , SW turns OFF (Time2 in Figure 5).

When SW turns OFF (Time2 in Figure 5), the magnetic energy in the transformer starts discharging. Meanwhile, U2 monitors the kickback voltage at the SW terminal. As the energy is discharging, the kickback voltage is increasing according to the increase of  $V_O$  (Time2 to Time3 in Figure 5). When almost all energy is discharged, the system cannot continue rectification via the diode, and the charging current of  $I_O$  goes to zero (Times3 in Figure 5). After rectification stops, the small amount of energy left in the transformer is released via parasitic paths, and the kickback voltage reaches zero (Time3 to Time4 in Figure 5). During this period, U2 makes SW turn ON when  $(V_{(SW)} - V_{BAT})$  dips from  $V_{(ZERO)}$  (Time5 in Figure 5). In the actual circuit, the period between Time4 and Time5 in Figure 5 is small or does not appear dependent on the delay time of the U2 detection to SW ON.

U1 also monitors the kickback voltage. When  $(V_{(SW)} - V_{BAT})$  exceeds  $V_{(FULL)}$ , the TPS65560 stops charging (see Figure 6).

In Figure 5 and Figure 6, ON time is always the same period in every switch cycle. The ON time is calculated by Equation 1.  $L$  and  $I_{(PEAK)}$  are selected to ensure that  $t_{ON}$  does not exceed the MAX ON time ( $t_{MAX}$ ).

$$t_{ON} = L \frac{I_{PEAK}}{V_{BAT}} \quad (1)$$

The *OFF* time is dependant on output voltage. As the output voltage gets higher, the *OFF* time gets shorter (see [Equation 2](#)).

$$t_{\text{OFF}} = N_{\text{TURN}} \times L \frac{I_{\text{PEAK}}}{V_{\text{OUT}}} \quad (2)$$

## Programming Peak Current

The TPS65560 provides a method to program the peak primary current with a voltage applied to the I\_PEAK pin. [Figure 7](#) shows how to program  $I_{(\text{PEAK})}$ .

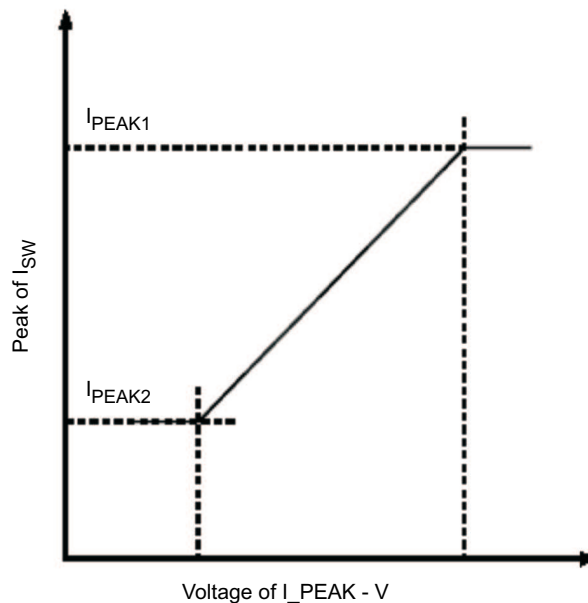
The I\_PEAK input is treated as a logic input below  $V_{(\text{PKL})}$  (0.6 V) and above  $V_{(\text{PKH})}$  (2.4 V). Between  $V_{(\text{PKL})}$  and  $V_{(\text{PKH})}$ , I\_PEAK input is treated as an analog input. Using this characteristic,  $I_{(\text{PEAK})}$  can be set by a logic signal or by an analog input.

Typical usages of this function are:

1. Setting the peak charging currents based on the battery voltage. Larger  $I_{(\text{PEAK})}$  for a fully charged battery and lower  $I_{(\text{PEAK})}$  for a discharged battery.
2. Reducing  $I_{(\text{PEAK})}$  when powering a zooming lens motor. This avoids inadvertent shutdowns due to large current from the battery.

In [Figure 1](#), three optional connections to I\_PEAK are shown.

1. Use the controller to treat I\_PEAK as the logic input pin. This option is the easiest.
2. Use a D/A converter to force  $I_{(\text{PEAK})}$  to follow analog information, such as battery voltage.
3. Use an analog circuit to achieve the same results as the D/A converter.



**Figure 7. I\_PEAK vs  $I_{(\text{SW})}$**



## IGBT Driver Control

The IGBT driver is provided by the TPS65560. The driver voltage depends on VCC. TPS65560 has a mask filter as shown in Figure 8. The mask does not have hysteresis; therefore, there is no wait time from CHG forcing Low after FULL CHARGE to F\_ON turning High.

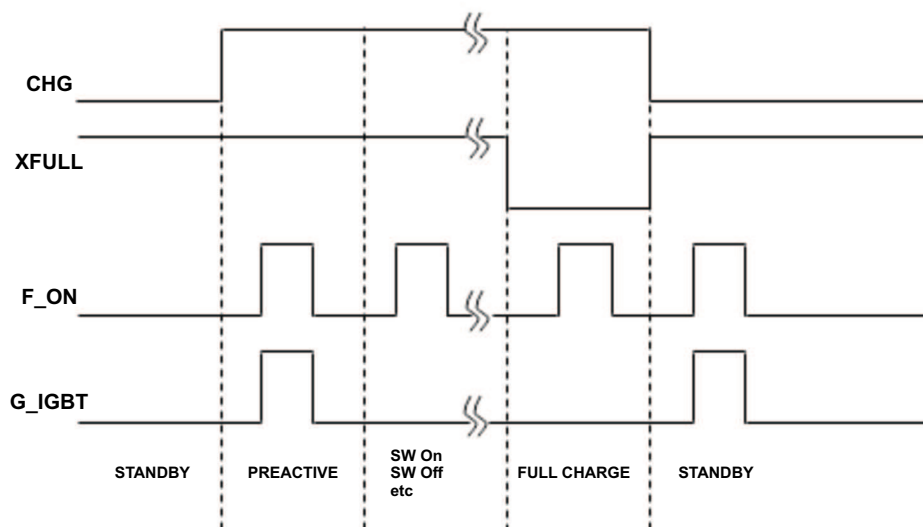


Figure 8. IGBT Timing Diagram

## Protections

TPS65560 provides four protection mechanisms: max on time, max off time, thermal disable, and overcurrent shutdown.

### MAX On Time

To prevent a condition such as pulling current from a poor power source (i.e., an almost empty battery), and never reaching peak current, the TPS65560 provides a maximum ON time function. If the ON time exceeds  $t_{MAX}$ , the TPS5560 is forced OFF regardless of  $I_{(PEAK)}$  detection.

### MAX Off Time

To prevent a condition such as never increasing the voltage at the SW pin when the internal FET is OFF, the TPS65560 provides a maximum OFF time function. If the OFF time exceeds  $t_{MIN}$ , the TPS65560 is forced ON regardless of  $V_{(ZERO)}$  detection.

### Thermal Disable

Once the TPS65560 die temperature reaches 160°C, all functions stop. Once the die cools below 160°C, the TPS65560 restarts charging if CHG remains high during the entire overtemperature condition.

### Overcurrent Shutdown to Monitor $V_{DS}$ at the SW Pin ( $OV_{DS}$ )

The TPS65560 provides an overvoltage monitor function of the SW pin. The TPS65560 is latched off if the voltage on the SW pin is above  $OV_{DS}$  during the switch ON time (see Figure 4 and its descriptions).

This function protects against short-circuits on the primary side of the transformer. A short-circuit of the primary side shorts the battery voltage to GND. SW pin can damage the device if not protected.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65560RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-35 to 85	BPR	<a href="#">Samples</a>
TPS65560RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-35 to 85	BPR	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65560RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65560RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65560RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
TPS65560RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

**RGT 16**

**GENERIC PACKAGE VIEW**

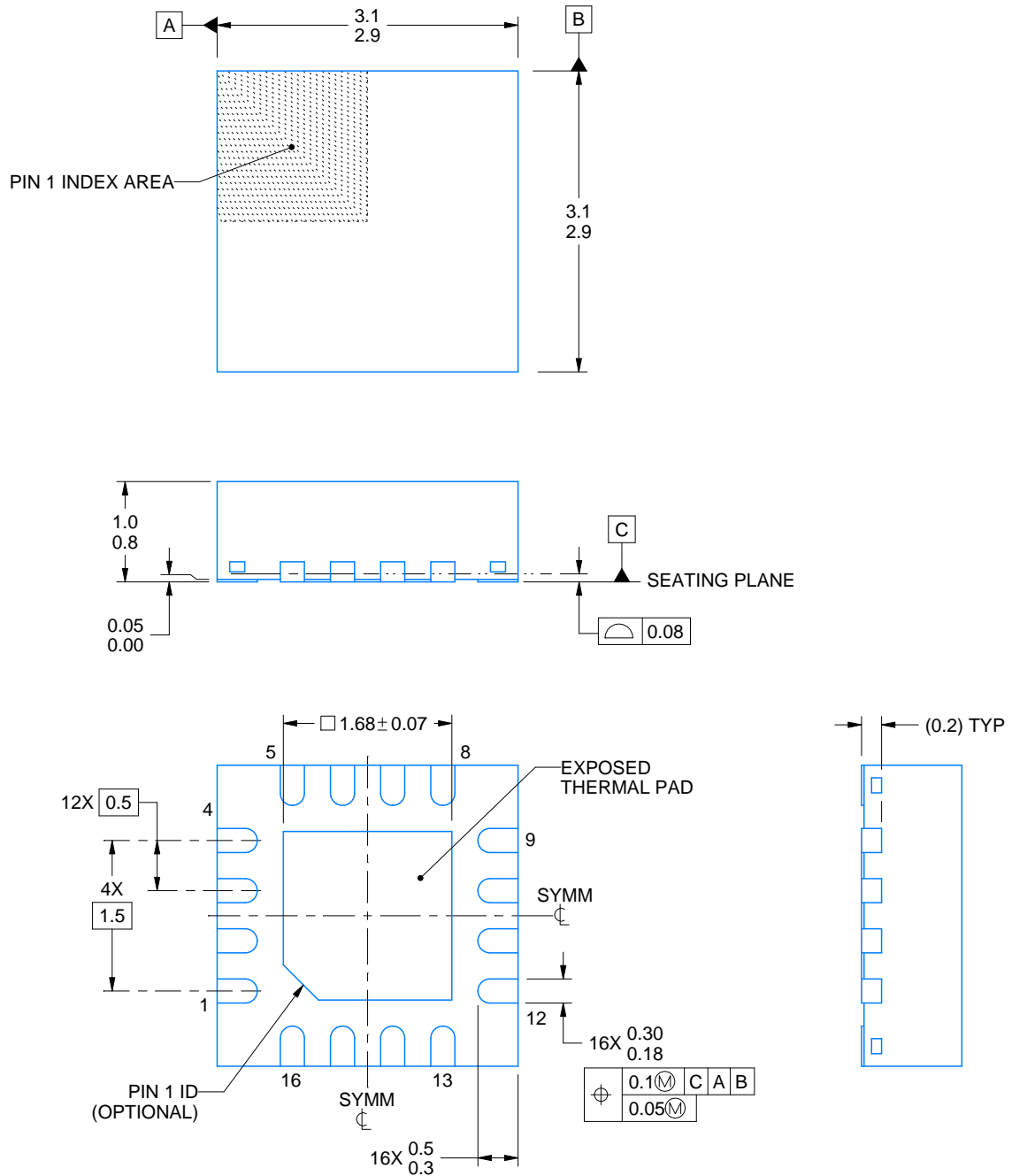
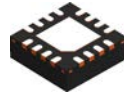
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203495/1



4222419/C 04/2021

## NOTES:

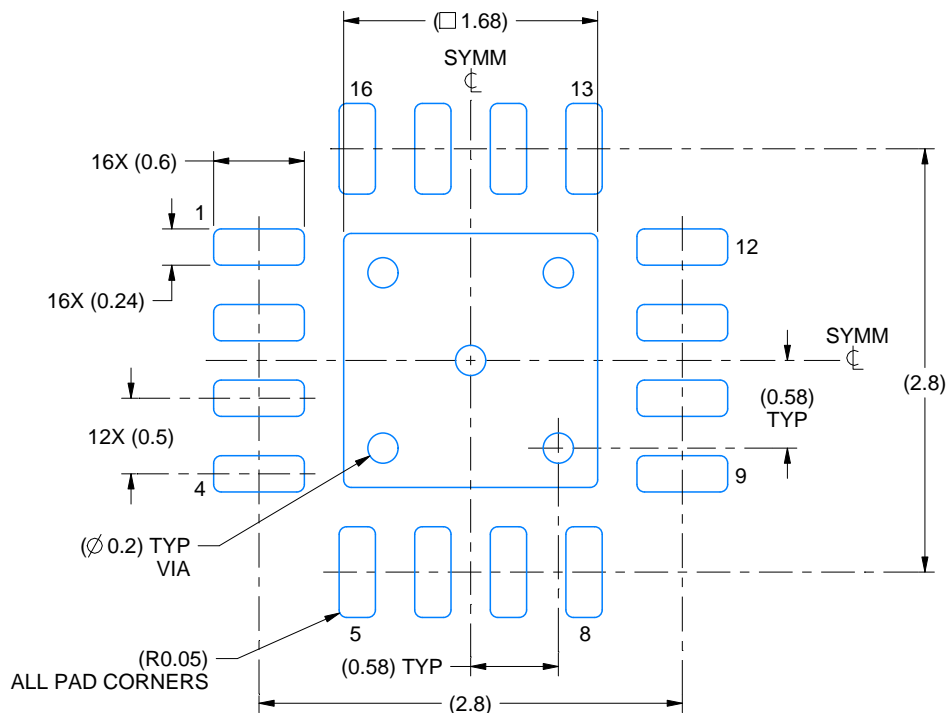
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

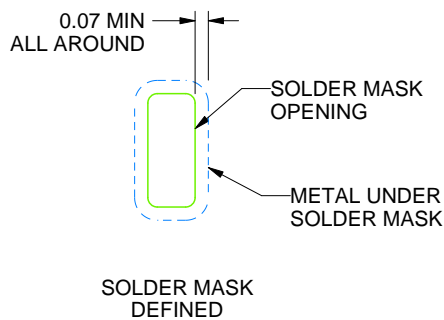
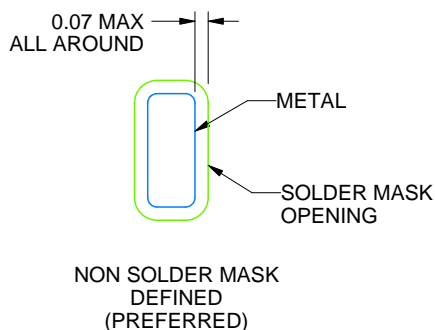
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4222419/C 04/2021

NOTES: (continued)

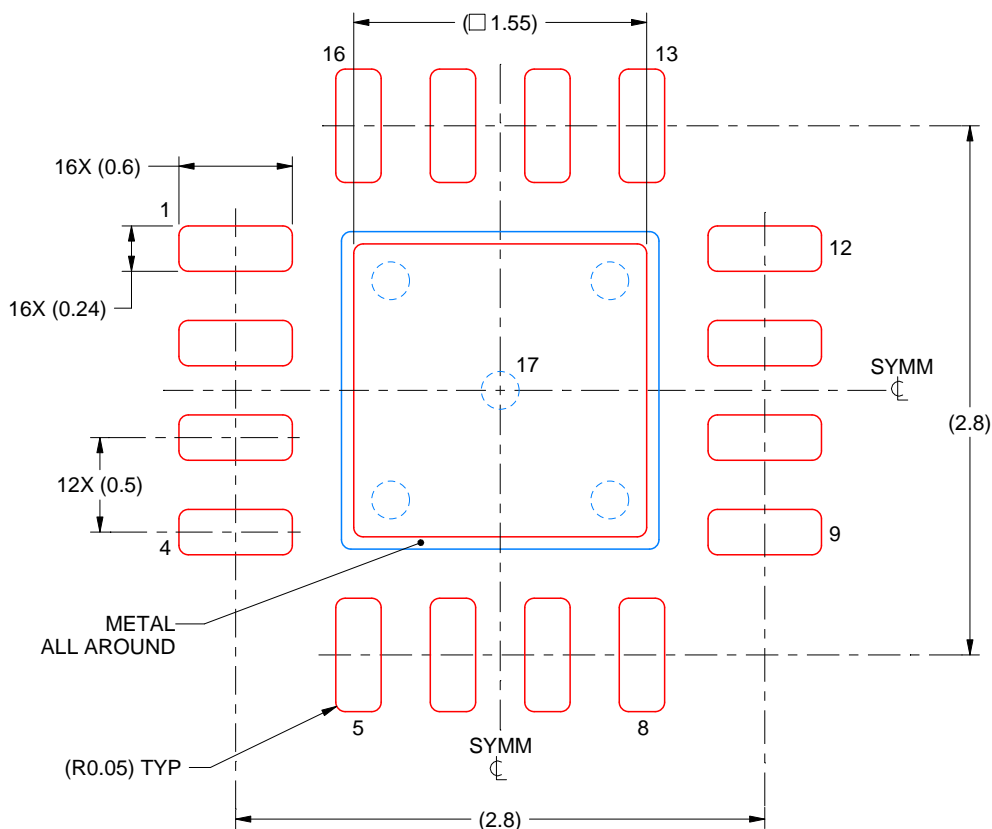
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



**RGT0016C**

### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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