TPS65705x PMU for Embedded Camera Module

1 Features

- Two 400-mA Step-Down Converters
- Up to 92% Efficiency
- V_{IN} Range for DC-DC Converter From 3.3 V to 6 V
- 2.25-MHz Fixed-Frequency Operation
- Power Save Mode at Light Load Current
- Output Voltage Accuracy in PWM Mode ±1.5%
- 100% Duty Cycle for Lowest Dropout
- 180° Out-of-Phase Operation
- 1 General Purpose 200-mA LDO
- V_{IN} Range for LDO From 1.7 V to 6.0 V
- Available in a 16-Ball DSBGA (WCSP) With 0.5-mm Pitch

2 Applications

- Digital Cameras
- Portable Media Players
- Handheld Equipment

3 Description

The TPS65705x devices are small power management units targeted for embedded camera module or other portable low-power consumer-end equipments. The device contains two highly efficient step-down converters, a low dropout linear regulator, and additional supporting functions. The 2.25-MHz step-down converter enters a low-power mode at light load for maximum efficiency across the widest possible range of load currents. For low-noise applications, the device can be forced into fixed-frequency PWM mode using the MODE pin. The device allows the use of small inductors and capacitors to achieve a small sized solution. The TPS65705x provides an output current of up to 400 mA on both DC-DC converters and integrates one 200-mA LDO with different output settings. The LDO operates with an input voltage range from 1.7 V to 6 V, thus allowing it to be supplied from the output of the step-down converter or directly from the system voltage.

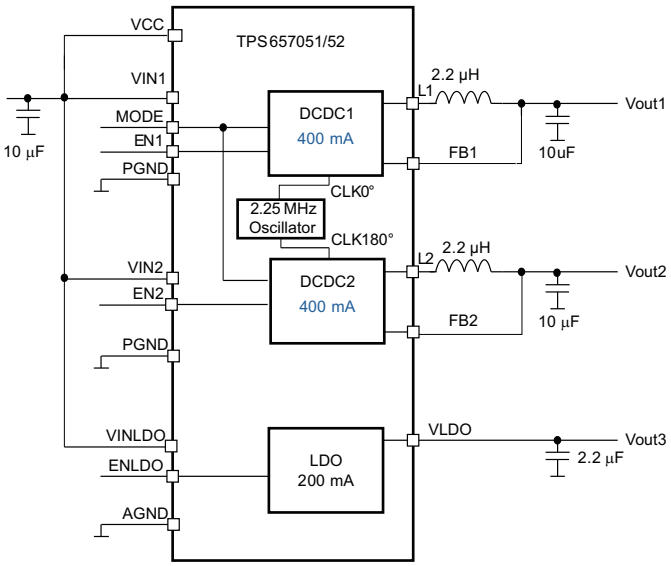
The TPS65705x comes in a small 16-pin wafer chip scale package (WCSP) with 0.5-mm ball pitch.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS657051	DSBGA (16)	2.08 mm × 2.08 mm
TPS657052		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2010) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed footnote error for Device Options table.	3

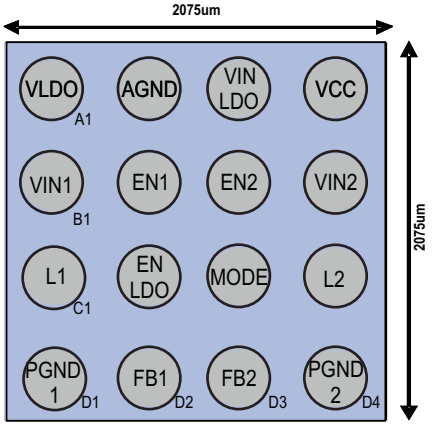
5 Device Options

PART NO.(1)	SIZE FOR DSBGA VERSION	OPTIONS	I²C
TPS657051	D = 2076 µm ± 25 µm E = 2076 µm ± 25 µm	DC-DC1 3.3 V FIX, DC-DC2 1.8 V FIX DC-DC CONVERTERS 400 mA, LDO VOUT 3 V FIX, 200 mA	N/A
TPS657052	D = 2076 µm ± 25 µm E = 2076 µm ± 25 µm	DC-DC1 3.3 V FIX, DC-DC2 1.8 V FIX DC-DC CONVERTERS 400 mA, LDO VOUT 2.8 V FIX, 200 mA	N/A

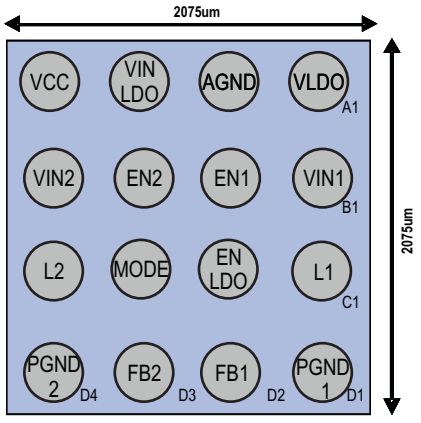
(1) For the most current package and ordering information, see the *Mechanical, Packaging, and Orderable Information* section at the end of this document, or see the TI website at www.ti.com.

6 Pin Configuration and Functions

TPS657051 YZH Package
16-Pin DSBGA
Top View



TPS657052 YZH Package
16-Pin DSBGA
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	VLDO	O	Output voltage from LDO
A2	AGND	—	Analog ground
A3	VINLDO	I	Input voltage pin for LDO
A4 (1)	VCC	I	Supply Input for internal reference, has to be connected to VIN1/ VIN2
B1 (2)	VIN1	I	Input voltage pin for buck converter 1
B2	EN1	I	Actively high enable input voltage for buck converter 1
B3	EN2	I	Actively high enable input voltage for buck converter 2
B4 (2)	VIN2	I	Input voltage pin for buck converter 2
C1	L1	O	Switch output from buck converter 1
C2	ENLDO	I	Actively high enable input voltage for LDO
C3	MODE	I	Set low to enable Power Save Mode. Pulling this PIN to high forces the device to operate in PWM mode over the whole load range.
C4	L2	O	Switch output from buck converter 2
D1	PGND1	—	Power ground
D2	FB1	I	Feedback input from buck converter 1
D3	FB2	I	Feedback input from buck converter 2
D4	PGND2	—	Power ground

(1) VCC must be the highest input for the device to function correctly.
(2) VIN1/VIN2 must be connected to VCC.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage on all pins except A/PGND pins with respect to AGND		–0.3	7	V
Voltage on pin VLDO1 with respect to AGND		–0.3	3.6	V
Current	L1, VLDO1, VINLDO1, PGND		600	mA
	AGND		20	mA
	All other pins		3	mA
Continuous total power dissipation		See *Dissipation Ratings*		
Operating free-air temperature, T_A		–40	85	°C
Maximum junction temperature, T_J			125	°C
Storage temperature, T_{stg}		–65	150	°C

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{IN1/2}$	Input voltage for step-down converter DCDC1 and DCDC2	3.3		6	V
$I_{OUTDCDC1/2}$	Output current at L			400	mA
L	Inductor at L	1.5	2.2	4.7	µH
V_{INLDO}	Input voltage for LDO	1.7		6.0	V
I_{LDO}	Output current at LDO			200	mA
$C_{INDCDC1/2}$	Input Capacitor at V_{IN1} and V_{IN2}	4.7			µF
$C_{OUTDCDC1/2}$	Output Capacitor at V_{OUT1}, V_{OUT2}	4.7	10	22	µF
C_{INLDO}	Input Capacitor at V_{INLDO}	2.2			µF
C_{OUTLDO}	Output Capacitor at V_{LDO}	2.2			µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS65705x YZH (DSBGA) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Unless otherwise noted: $V_{IN1} = V_{IN2} = V_{INLDO} = 3.6$ V, L = LQMP21P 2.2 µH, $C_{OUTDCDCx} = 10$ µF, $C_{OUTLDO} = 2.2$ µF, $T_A = –40°C$ to +85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_Q	Operating quiescent current DCDCx	DCDC1 and DCDC2 enabled, I_{OUT} = 0 mA, MODE =0 (PFM mode), LDO disabled		40		µA
		DCDC1 or DCDC2 enabled, I_{OUT} = 0 mA, MODE =0 (PFM mode), LDO disabled		25		µA
		DCDC1 or DCDC2 enabled, I_{OUT} = 0 mA. MODE =1 (forced PWM mode), LDO disabled		4		mA
	Operating quiescent current LDO	DCDC1 and DCDC2 disabled, LDO enabled. IOUT = 0 mA		25	37	µA
I_{SD}	Shutdown current	DCDC1, DCDC2, and LDO disable		5	12	µA
DIGITAL PINS (EN1, EN2, ENLDO, MODE)						
V_{IH}	High-level input voltage for EN1, EN2, ENLDO, MODE		1.2		VCC	V
V_{IL}	Low-level input voltage for EN1, EN2, ENLDO, MODE				0.4	V
I_{LKG}	Input leakage current	EN1, EN2, ENLDO, MODE tied to GND or $V_{IN} = V_{IN2}$		0.01	0.1	µA
STEP-DOWN CONVERTERS						
V_{IN1}	Input voltage for DCDC1		3.3		6	V

Electrical Characteristics (continued)

Unless otherwise noted: $V_{IN1} = V_{IN2} = V_{INLDO} = 3.6$ V, L = LQMP21P 2.2 µH, $C_{OUTDCDCx} = 10$ µF, $C_{OUTLDO} = 2.2$ µF, $T_A = –40°C$ to +85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN2}	Input voltage for DCDC2		3.3		6	V
UVLO	Internal undervoltage lockout threshold	$V_{IN1} = V_{IN2}$ falling	2.15	2.2	2.25	V
	Internal undervoltage lockout threshold hysteresis	$V_{IN1} = V_{IN2}$ rising		120		mV
POWER SWITCH						
$R_{DS(ON)}$	High-side MOSFET ON-resistance	$V_{IN1} = V_{IN2} = 3.6$ V		350	750	mΩ
	Low-side MOSFET ON-resistance	$V_{IN1} = V_{IN2} = 3.6$ V		350	600	mΩ
I_{LIMF}	Forward current limit	3.3 V ≤ $V_{IN1} = V_{IN2}$ ≤ 6 V	550	650	770	mA
$I_{OUTDCDC1/2}$	DCDC1/DCDC2 output current	$V_{IN1} = V_{IN2}$ > 3.3 V , L = 2.2 µH			400	mA
OSCILLATOR						
f_{SW}	Oscillator frequency		2.03	2.25	2.48	MHz
OUTPUT						
V_{OUT1}	DCDC1 default output voltage	$V_{IN1} = V_{IN2}$ ≥ 3.3 V		3.3		V
V_{OUT2}	DCDC2 default output voltage	$V_{IN1} = V_{IN2}$ ≥ 3.3 V		1.8		V
I_{FB}	FB pin input current	DC-DC converter disabled			0.1	µA
V_{OUT}	DC output voltage accuracy(1)	$V_{IN1} = V_{IN2} = 3.3$ V to 6 V, +1% voltage positioning active; PFM operation, 0 mA < I_{OUT} < I_{OUTMAX}		+1%	+3%	
	DC output voltage accuracy	$V_{IN1} = V_{IN2} = 3.3$ V to 6 V, PWM operation, 0 mA < I_{OUT} < I_{OUTMAX}	–1.5%		+1.5%	
	DC output voltage load regulation	PWM operation		0.5		%/A
t_{Start}	Start-up time	Time from active EN to Start switching		200		µs
t_{Ramp}	V_{OUT} ramp time	Time to ramp from 5% to 95% of V_{OUT}		250		µs
R_{DIS}	Internal discharge resistor at L1 or L2 (TPS657051 Only)	DCDC1 or DCDC2 disabled	250	400	600	Ω
THERMAL PROTECTION SEPARATELY FOR DCDC1, DCDC2 AND LDO1						
T_{SD}	Thermal shutdown	Increasing junction temperature		150		°C
	Thermal shudown hysteresis	Decreasing junction temperature		30		°C
VLDO, LOW DROPOUT REGULATOR						
V_{INLDO}	Input voltage range for LDO		1.7		6	V
V_{LDO}	TPS657051 LDO default output voltage(2)			3		V
V_{LDO}	TPS657052 LDO default output voltage(3)			2.8		V
I_O	Output current for LDO				200	mA
I_{SC}	LDO short circuit current limit	V_{LDO} = GND	340	400	550	mA
	Dropout voltage at LDO	$I_O = 200$ mA			200	mV
	Output voltage accuracy for LDO	$I_O = 100$ mA, $V_{OUT} = 2.8$V	–2%		+2%	
	Line regulation for LDO	$V_{INLDO} = V_{LDO}$ + 0.5 V (min. 1.7 V) to 6 V, $I_O = 50$ mA	–1%		1%	
	Load regulation for LDO	$I_O = 1$ mA to 200 mA for LDO	–1%		1%	
PSRR	Power supply rejection ratio	f_{NOISE} ≤ 10 kHz, C_{OUT} ≥ 2.2 µf Vin = 5 V, Vout = 2.8 V, IOUT = 100 mA		50		dB
Vn	Ouput noise voltage	Vout = 2.8 V, BW = 10Hz to 100kHz		160		µV RMS

(1) In Power Save Mode (PFM), the internal reference voltage is 1.01 × Vref.
(2) VINLDO > 3 V
(3) VINLDO > 2.8 V

Electrical Characteristics (continued)

Unless otherwise noted: $V_{IN1} = V_{IN2} = V_{INLDO} = 3.6$ V, L = LQMP21P 2.2 µH, $C_{OUTDCDCx} = 10$ µF, $C_{OUTLDO} = 2.2$ µF, $T_A = –40°C$ to +85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{Ramp}	V_{OUT} ramp time	Internal soft-start when LDO is enabled; Time to ramp from 5% to 95% of V_{OUT}		200		µs
R_{DIS}	Internal discharge resistor at VLDO	LDO disabled	250	400	550	Ω

7.6 Dissipation Ratings

DEVICE	PACKAGE	$R_{\theta JA}$	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
TPS657051/52 (1)	YZH	185	540 mW	5.4 mW	297 mW	216 mW
TPS657051/52 (2)	YZH	75	1.3 W	13.3 mW	0.7 W	0.5 W

(1) The JEDEC low-K (1s) board used to derive this data was a 3in × 3in, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3in × 3in, multilayer board with 1-ounce internal power and ground.

7.7 Typical Characteristics

Table 1. Table Of Graphs

		FIGURE
Efficiency DC-DC (VDCDC= 3.3 V), L = BRC1608 1.5 µH	vs Load current / PFM mode	Figure 1
Efficiency DC-DC (VDCDC= 3.3 V), L = BRC1608 1.5 µH	vs Load current / PWM mode	Figure 2
Efficiency DC-DC (VDCDC= 1.8 V), L = BRC1608 1.5 µH	vs Load current / PFM mode	Figure 3
Efficiency DC-DC (VDCDC= 1.8 V), L = BRC1608 1.5 µH	vs Load current / PWM mode	Figure 4
Line transient response DC-DC 1.8 V (PWM)	Scope plot	Figure 5
Line transient response DC-DC 1.8 V (PFM)	Scope plot	Figure 6
Line transient response LDO 2.8 V	Scope plot	Figure 7
Load transient response DC-DC 1.8 V (PWM/PFM) 20 mA to 180 mA	Scope plot	Figure 8
Load transient response DC-DC 1.8 V (PWM) 20 mA to 180 mA	Scope plot	Figure 9
Load transient response DC-DC 1.8 V (PFM/PWM) 20 mA to 360 mA	Scope plot	Figure 10
Load transient response DC-DC 1.8 V (PWM) 20 mA to 360 mA	Scope plot	Figure 11
Load transient response LDO 2.8 V	Scope plot	Figure 12
DC-DC PFM to PWM mode transition	Scope plot	Figure 13
DC-DC PWM to PFM mode transition	Scope plot	Figure 14
DC-DC Output voltage ripple in PFM mode	Scope plot	Figure 15
DC-DC Output voltage ripple in PWM mode	Scope plot	Figure 16
Startup timing DC-DC 1.8 V	Scope plot	Figure 22
Startup timing LDO 2.8 V	Scope plot	Figure 23
LDO PSRR	Scope plot	Figure 17
DC-DC Quiescent current	vs VINDCDC	Figure 18
LDO Quiescent current	vs VINDCDC	Figure 19
Shutdown current	vs VINDCDC	Figure 20

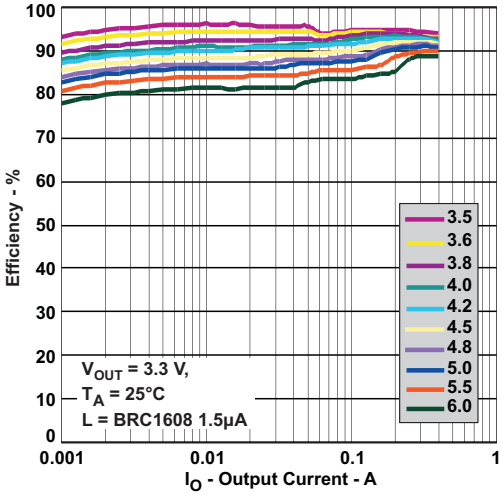


Figure 1. Efficiency DC-DC (VDCDC=3.3 V) vs Load Current PFM Mode

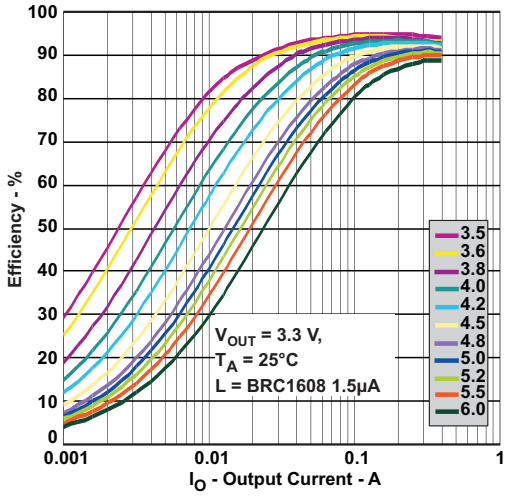


Figure 2. Efficiency DC-DC (VDCDC=3.3 V) vs Load Current PWM Mode

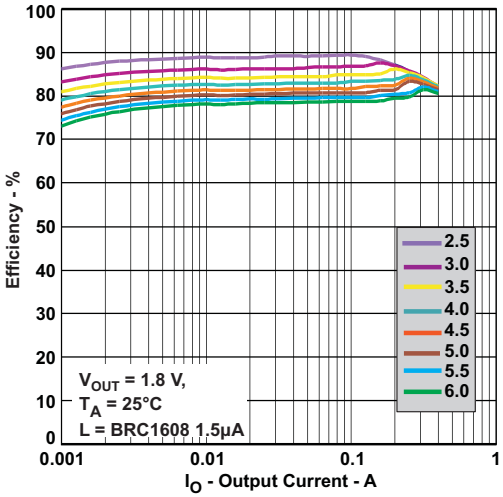


Figure 3. Efficiency DC-DC (VDCDC=1.8 V) vs Load Current PFM mode

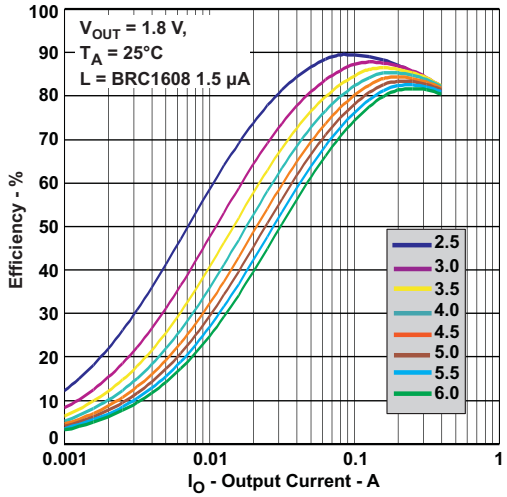


Figure 4. Efficiency DC-DC (VDCDC=1.8 V) vs Load Current PWM mode

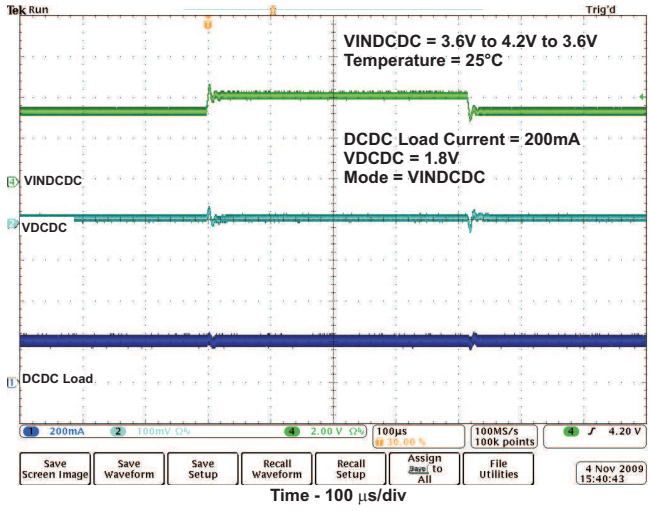


Figure 5. Line Transient Response DC-DC 1.8 V (PWM)

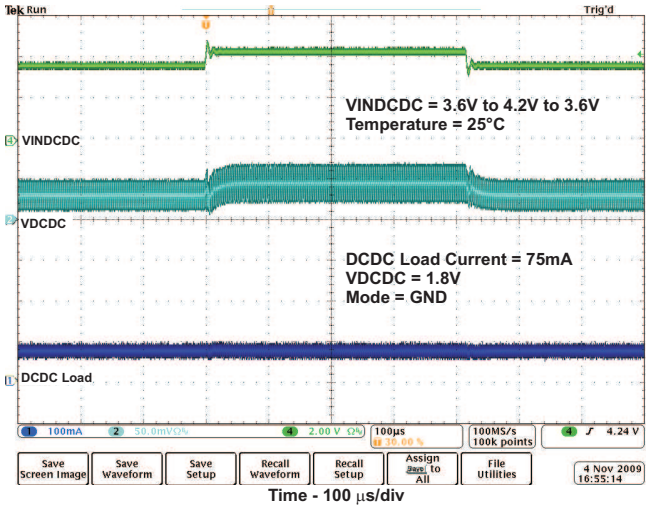


Figure 6. Line Transient Response DC-DC 1.8 V (PFM)

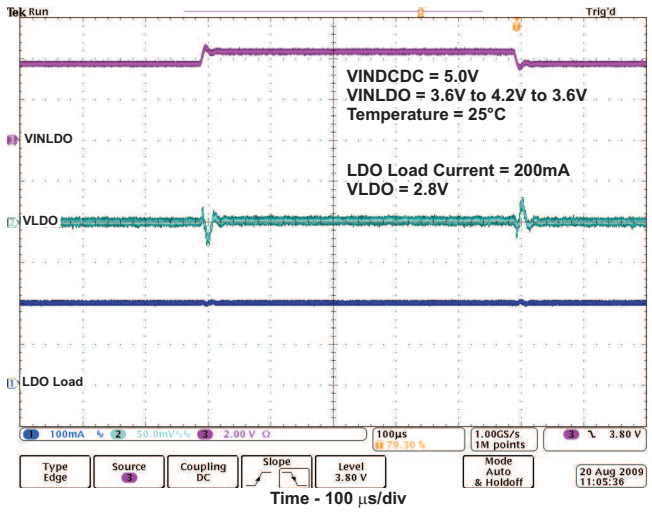


Figure 7. Line Transient Response LDO 2.8 V

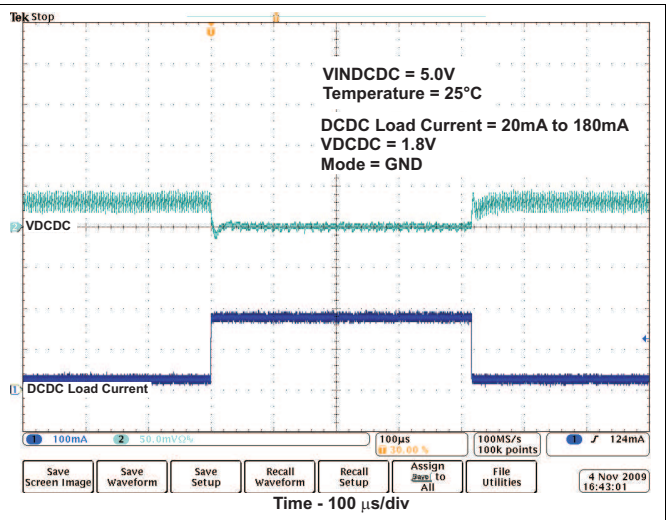


Figure 8. Load Transient Response DC-DC 1.8 V (PWM/PFM) 20 mA to 180 mA

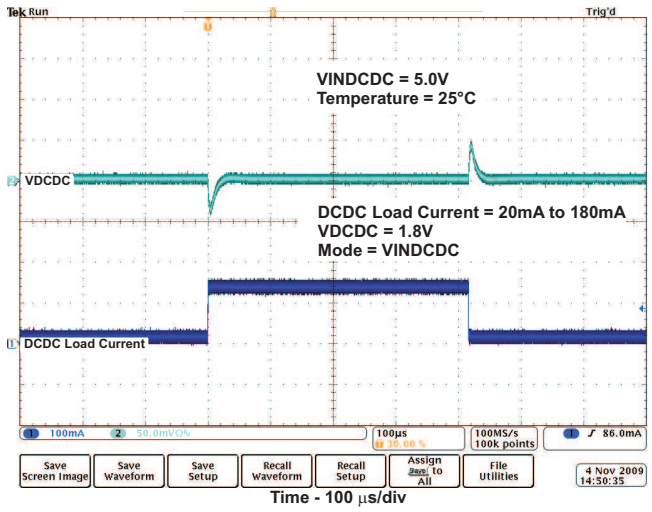


Figure 9. Load Transient Response DC-DC 1.8 V (PWM) 20 mA to 180 mA

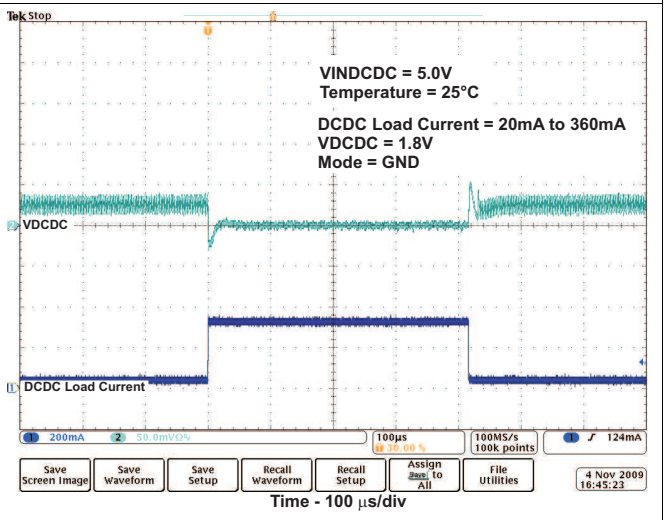


Figure 10. Load Transient Response DC-DC 1.8 V (PFM/PWM) 20 mA to 360 mA

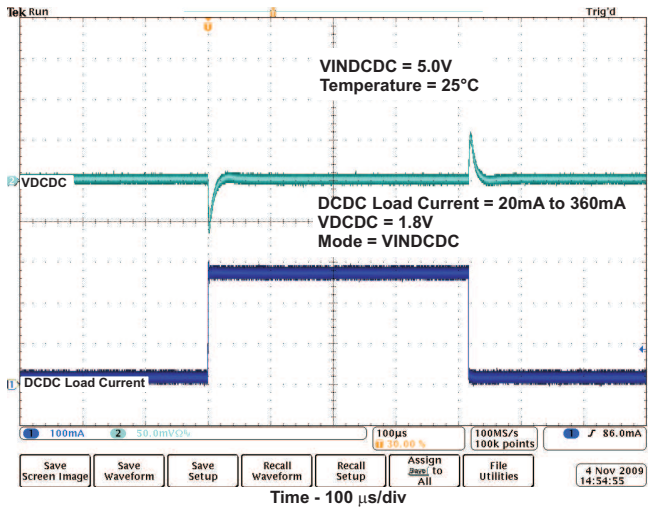


Figure 11. Load Transient Response DC-DC 1.8 V (PWM) 20 mA to 360 mA

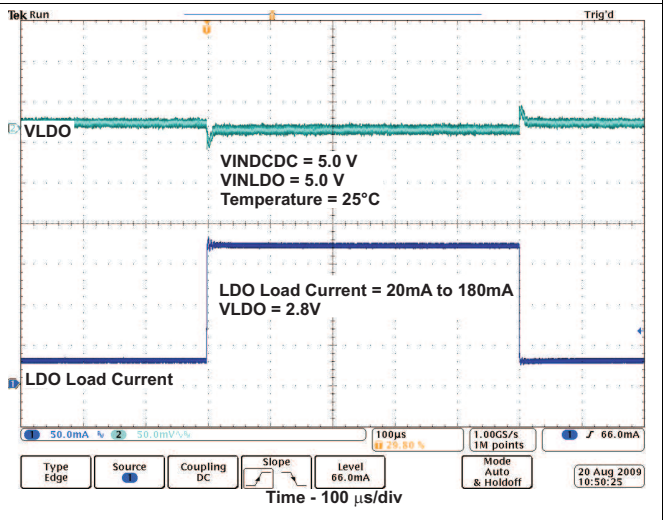


Figure 12. Load Transient Response LDO

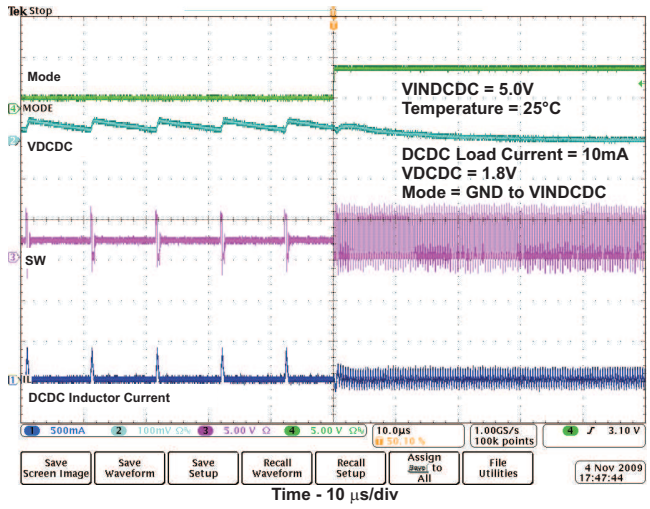


Figure 13. DC-DC PFM to PWM Mode Transition

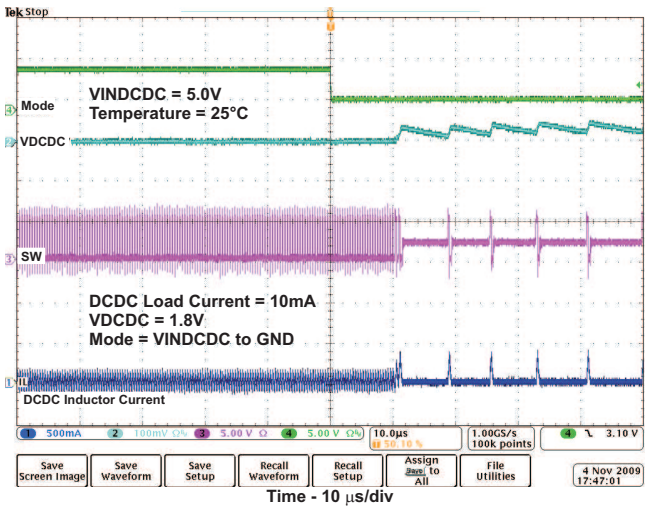


Figure 14. DC-DC PWM to PFM Mode Transition

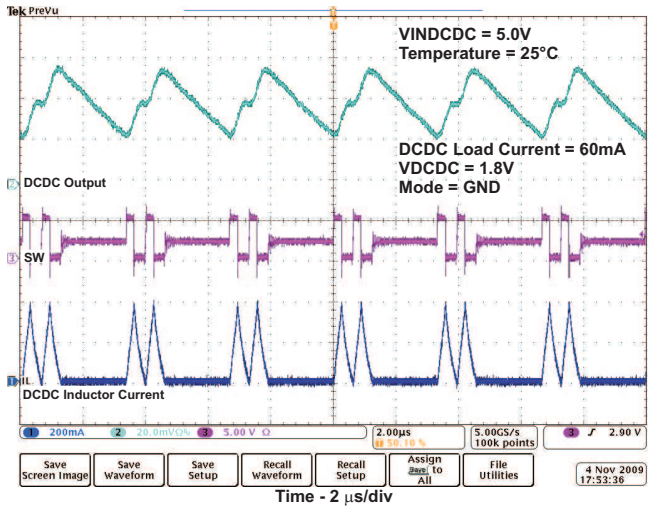


Figure 15. DC-DC Output Voltage Ripple in PFM Mode

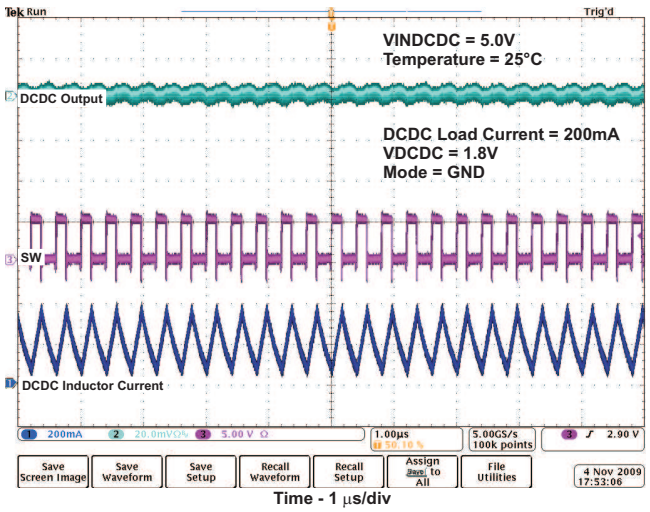


Figure 16. DC-DC Output Voltage Ripple in PWM Mode

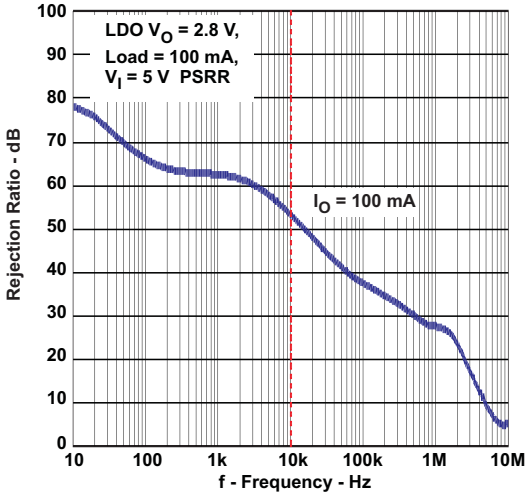


Figure 17. LDO PSRR

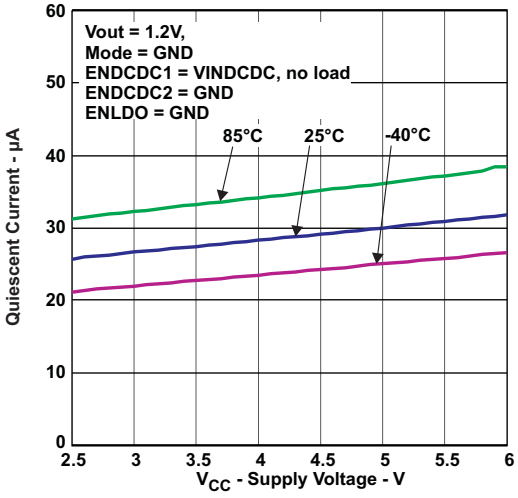


Figure 18. DC-DC Quiescent Current

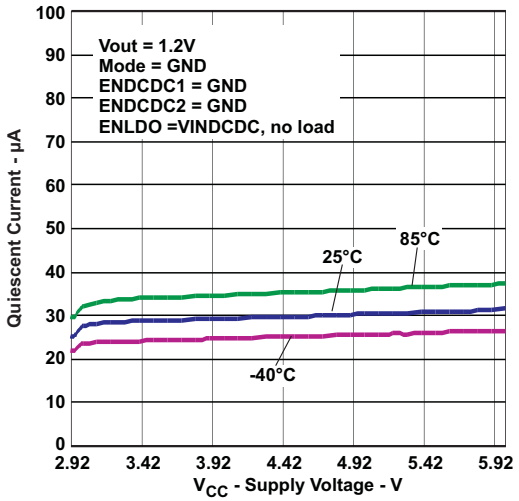


Figure 19. LDO Quiescent Current

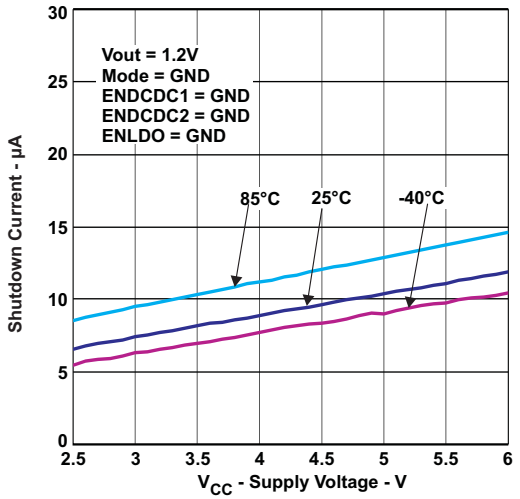


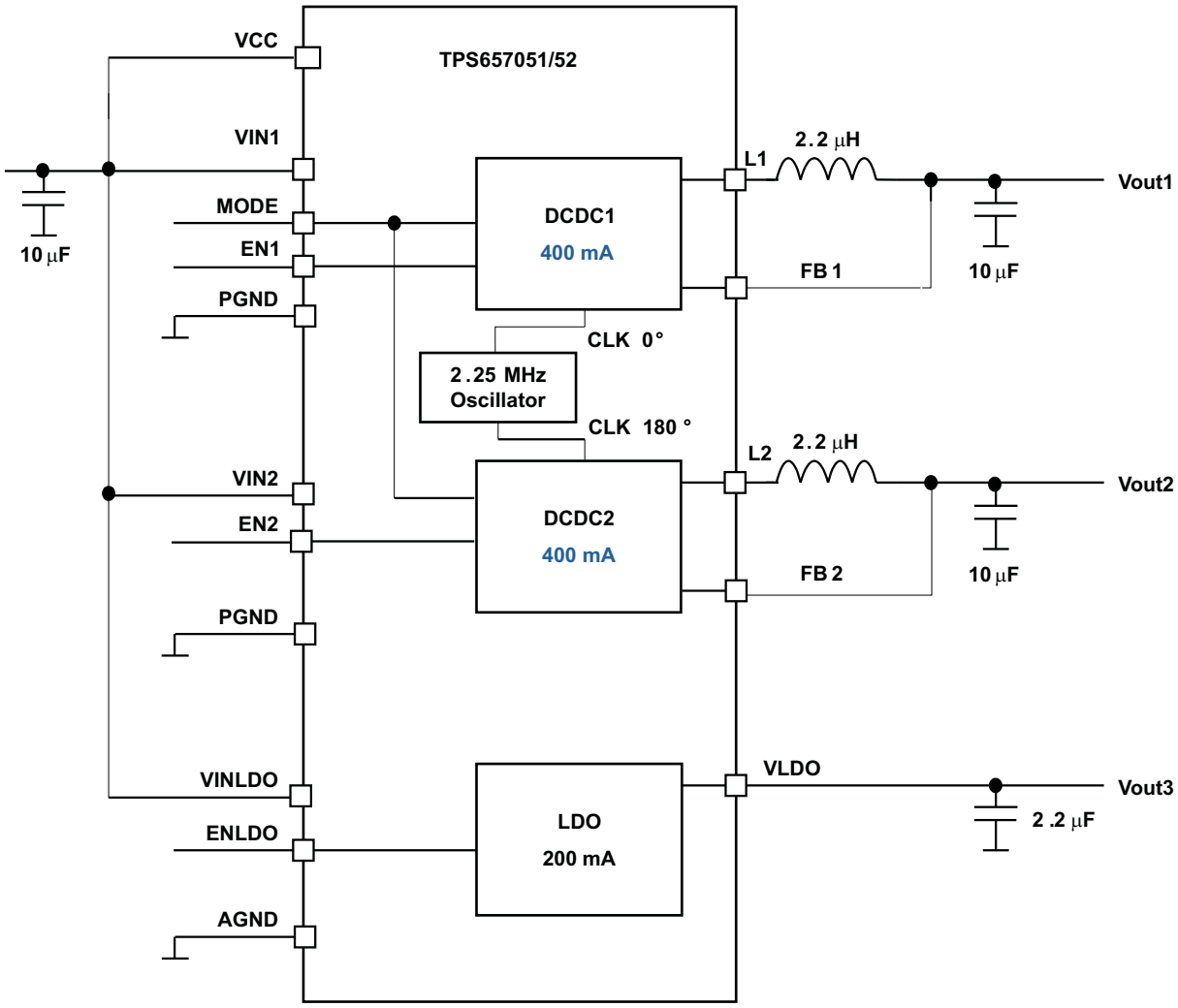
Figure 20. Shutdown Current

8 Detailed Description

8.1 Overview

The TPS65705x integrates fixed-output voltage, two highly efficient step-down converters, along with an LDO. Each regulator has dedicated input pins for easy control.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DC-DC Converter

The TPS65705x step-down converter operates with typically 2.25-MHz fixed-frequency pulse width modulation (PWM) at moderate to heavy load currents. With MODE pin set to low, at light load currents the converter can automatically enter Power Save Mode and operates then in PFM mode.

During PWM operation the converter use a unique fast response voltage mode control scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high-side MOSFET switch is turned on. The current flows now from the input capacitor through the high-side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips

Feature Description (continued)

and the control logic will turn off the switch. The current limit comparator will also turn off the switch in case the current limit of the high-side MOSFET switch is exceeded. After an off time preventing shoot through current, the low-side MOSFET rectifier is turned on and the inductor current will ramp down. The current flows now from the inductor to the output capacitor and to the load. It returns back to the inductor through the low-side MOSFET rectifier.

The next cycle will be initiated by the clock signal again turning off the low-side MOSFET rectifier and turning on the on the high-side MOSFET switch. The DCDC1 converter output voltage is set to 3.3 V and the DCDC2 converter output voltage is set to 1.8 V per default. A 180° phase shift between DCDC1 and DCDC2 decreases the input RMS current and synchronizes the operation of the two DC-DC converts. The FB pin must be directly connected to the output voltage of DC-DC and no external resistor network must be connected.

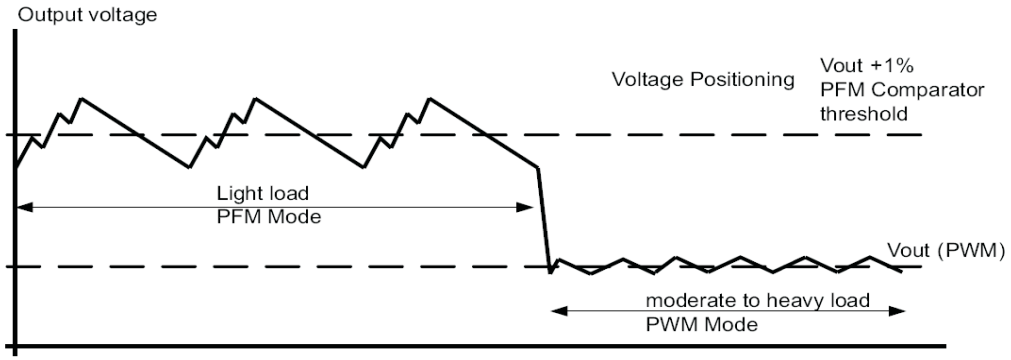
8.3.2 Power Save Mode

The Power Save Mode is enabled with Mode Pin set to low. If the load current decreases, the converter will enter Power Save Mode operation automatically. During Power Save Mode the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency. The converter will position the output voltage typically +1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step. The transition from PWM mode to PFM mode occurs once the inductor current in the low-side MOSFET switch becomes zero, which indicates discontinuous conduction mode. During the Power Save Mode the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of VOUT nominal +1%, the device starts a PFM current pulse. The high-side MOSFET switch will turn on, and the inductor current ramps up. After the ON-time expires, the switch is turned off and the low-side MOSFET switch is turned on until the inductor current becomes zero. The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage will rise. If the output voltage is equal or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typical 25-µA current consumption.

If the output voltage is still below the PFM comparator threshold, a sequence of further PFM current pulses are generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold. With a fast single threshold comparator, the output voltage ripple during PFM mode operation can be kept small. The PFM Pulse is time controlled, which allows to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency depend in first order on the size of the output capacitor and the inductor value. Increasing output capacitor values and inductor values will minimize the output ripple. The PFM frequency decreases with smaller inductor values and increases with larger values. The PFM mode is left and PWM mode is entered in case the output current can not longer be supported in PFM mode. The Power Save Mode can be disabled by setting Mode pin to high. The converter will then operate in fixed-frequency PWM mode.

8.3.2.1 Dynamic Voltage Positioning

This feature reduces the voltage under/overshoots at load steps from light to heavy load and vice versa. It is active in Power Save Mode and regulates the output voltage 1% higher than the nominal value. This provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off.



Feature Description (continued)

8.3.2.2 Soft Start

The step-down converter in TPS657051/52 has an internal soft start circuit that controls the ramp up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within typical 250s. This limits the inrush current in the converter during ramp up and prevents possible input voltage drops when a battery or high impedance power source is used.

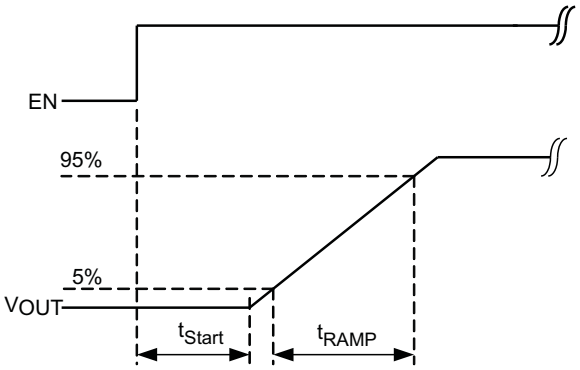


Figure 21. Soft Start

8.3.2.3 100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty cycle mode once the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the high-side MOSFET switch is turned on 100% for one or more cycles. With further decreasing VIN the high-side MOSFET switch is turned on completely. In this case the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{INmin} = V_{Omax} + I_{Omax} (R_{DS(on)}max + R_L) \quad (1)$$

where

- I_{Omax} = maximum output current plus inductor ripple current
- $R_{DS(on)}$max = maximum high-side switch RDSon
- R_L = DC resistance of the inductor
- V_{Omax} = nominal output voltage plus maximum output voltage tolerance

8.3.3 180° Out-of-Phase Operation

In PWM Mode the converters operate with a 180° turn-on phase shift of the PMOS (high-side) transistors. This prevents the high-side switches of both converters from being turned on simultaneously, and therefore smooths the input current. This feature reduces the surge current drawn from the supply.

8.3.3.1 Under-Voltage Lockout

The under voltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the converters and LDOs. The under-voltage lockout threshold is typically 2.2 V.

8.3.4 Short-Circuit Protection

All outputs are short-circuit protected with a maximum output current as defined in the electrical specifications.

8.3.5 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds typically 150°C for the DC-DC converter or LDO, the device goes into thermal shutdown. In this mode, the low-side and high-side MOSFETs are turned-off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis again. A thermal shutdown for the LDO or the DC-DC converter will disable both power supplies simultaneously.

Feature Description (continued)

8.3.6 LDO

The low dropout voltage regulator is designed to operate well with low value ceramic input and output capacitors. It operates with input voltages down to 1.7 V. The LDO offers a maximum dropout voltage of 200 mV at rated output current. The LDO supports a current limit feature.

8.3.7 Enable for DCDC1, DCDC2 and LDO

Disabling the DC-DC converter or LDO, forces the device into shutdown, with a shutdown quiescent current as defined in *Electrical Characteristics*. In this mode, the power FETs are turned-off and the entire internal control circuitry is switched-off.

8.4 Device Functional Modes

DCDC1, DCDC2, and LDO have dedicated enable pins. If all enable pins are pulled low the device will remain shutdown. If any of enable pins are pulled high corresponding regulators are enabled.

9 Application and Implementation

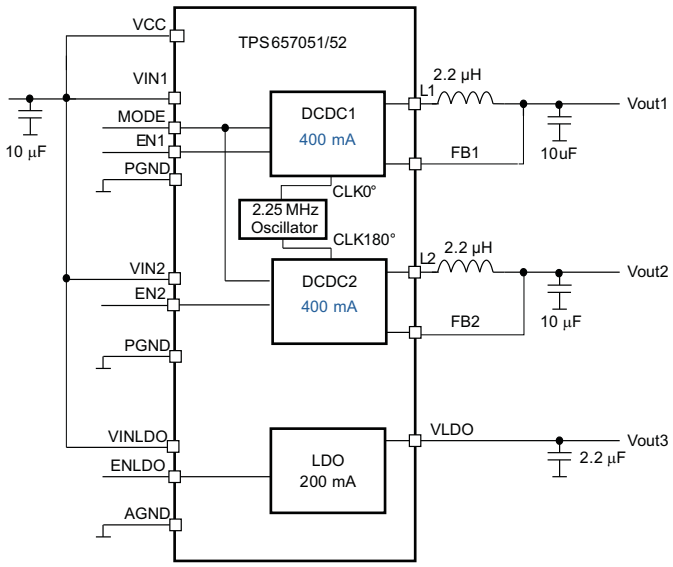
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS65705x device is designed for use as a power supply for embedded camera modules or other portable low-power equipment.

9.2 Typical Application



9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	VALUE
Input Supply Voltage	3.3 V to 6 V
Switching Frequency	2.25 Mhz

9.2.2 Detailed Design Procedure

9.2.2.1 Output Filter Design (Inductor and Output Capacitor)

9.2.2.1.1 Inductor Selection

The converter operates typically with 2.2-µH output inductor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductor will influence directly the efficiency of the converter. Therefore an inductor with lowest DC resistance should be selected for highest efficiency.

Equation 2 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 2. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (2)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (3)$$

where

- f = Switching Frequency (2.25 MHz typical)
- L = Inductor Value
- ΔI_L = Peak-to-Peak inductor ripple current
- I_{Lmax} = Maximum Inductor current

The highest inductor current will occur at maximum Vin.

Open core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. It must be considered, that the core material from inductor to inductor differs and will have an impact on the efficiency especially at high switching frequencies.

Notice that the step-down converter has internal loop compensation. As the internal loop compensation is designed to work with a certain output filter corner frequency calculated as follows:

$$f_c = \frac{1}{2\pi\sqrt{L \times Cout}} \quad \text{with } L = 2.2\ \mu H,\ Cout = 10\ \mu F \quad (4)$$

This leads to the fact the selection of external L-C filter has to be coped with the above formula. As a general rule of thumb the product of LxCout should be constant while selecting smaller inductor or increasing output capacitor value.

Refer to Table 3 and the typical applications for possible inductors.

Table 3. Tested Inductors

INDUCTOR TYPE	INDUCTOR VALUE	SUPPLIER
BRC1608	1.5 µH	Taiyo Yuden
MLP2012	2.2 µH	TDK
MIPSA2520	2.2 µH	FDK
LPS3015	2.2 µH	Coilcraft
LQM21P	2.2 µH	Murata

9.2.2.1.2 Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the step-down converter allows the use of small ceramic capacitors with a typical value of 10 µF, without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values result in lowest output voltage ripple and are therefore recommended. For an inductor value of 2.2 µH, an output capacitor with 10 µF can be used. Refer to Table 4.

If ceramic output capacitors are used, the capacitor RMS ripple current rating will always meet the application requirements. Just for completeness the RMS ripple current is calculated as:

$$I_{RMSCout} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (5)$$

At nominal load current the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta Vout = Vout \times \frac{1-\frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right) \quad (6)$$

Where the highest output voltage ripple occurs at the highest input voltage Vin.

At light load currents the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage

9.2.2.1.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. The converters need a ceramic input capacitor of 10 µF. The input capacitor can be increased without any limit for better input voltage filtering.

Table 4. Tested Capacitors

TYPE	COMPONENT SUPPLIER	VALUE	VOLTAGE RATING	SIZE	MATERIAL
DC-DC Output Capacitor	Murata GRM155R60G475ME47D	4.7 µF	4 V	0402	Ceramic X5R
LDO I/O Capacitor	Murata GRM155R60J225ME15D	2.2 µF	6.3 V	0402	Ceramic X5R
DC-DC Output Capacitor	Murata GRM188R60J475K	4.7 µF	6.3 V	0603	Ceramic X5R
DC-DC I/O Capacitor	Murata GRM188R60J106M69D	10 µF	6.3 V	0603	Ceramic X5R

9.2.3 Application Curves

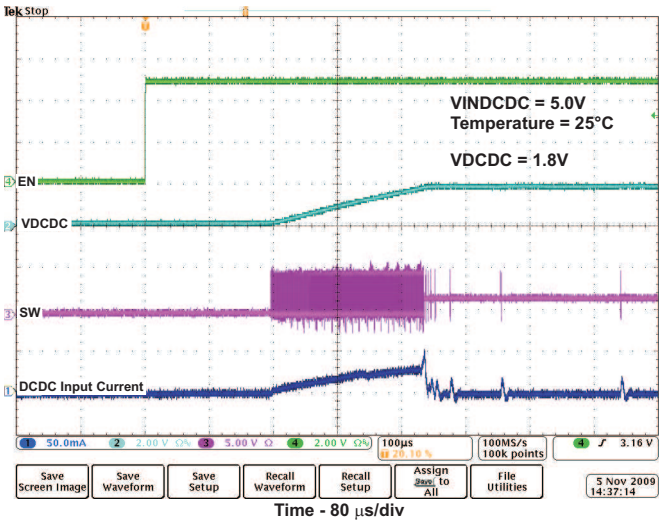


Figure 22. Start-Up Timing DC-DC

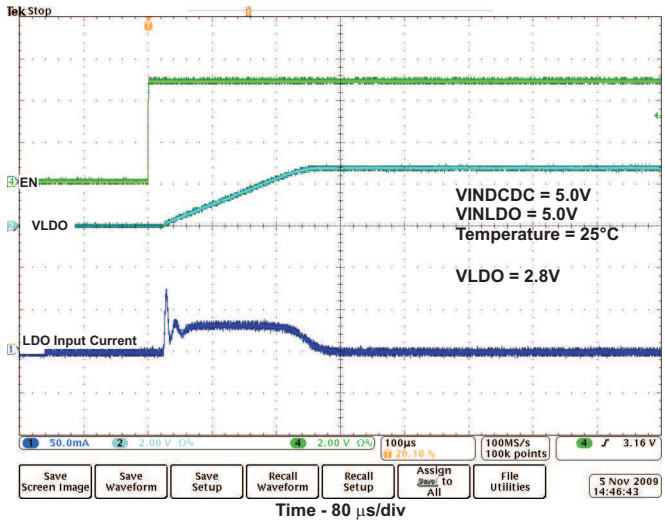


Figure 23. Start-Up Timing LDO

10 Power Supply Recommendations

The device is optimized to be powered from single-cell Lithium battery. The input supply is required to stay above UVLO threshold without shutting down DC-DC converters. Power input pins of each regulator should be properly bypassed through ceramic capacitors that work best when placed close to the input pins as close as possible.

11 Layout

11.1 Layout Guidelines

- All input capacitors should be soldered as close as possible to the device.
- All inductors should be placed as close as possible to switching pins through thick trace.
- All feedback traces should be routed differentially and away from noisy traces such as switching signals.

11.2 Layout Example

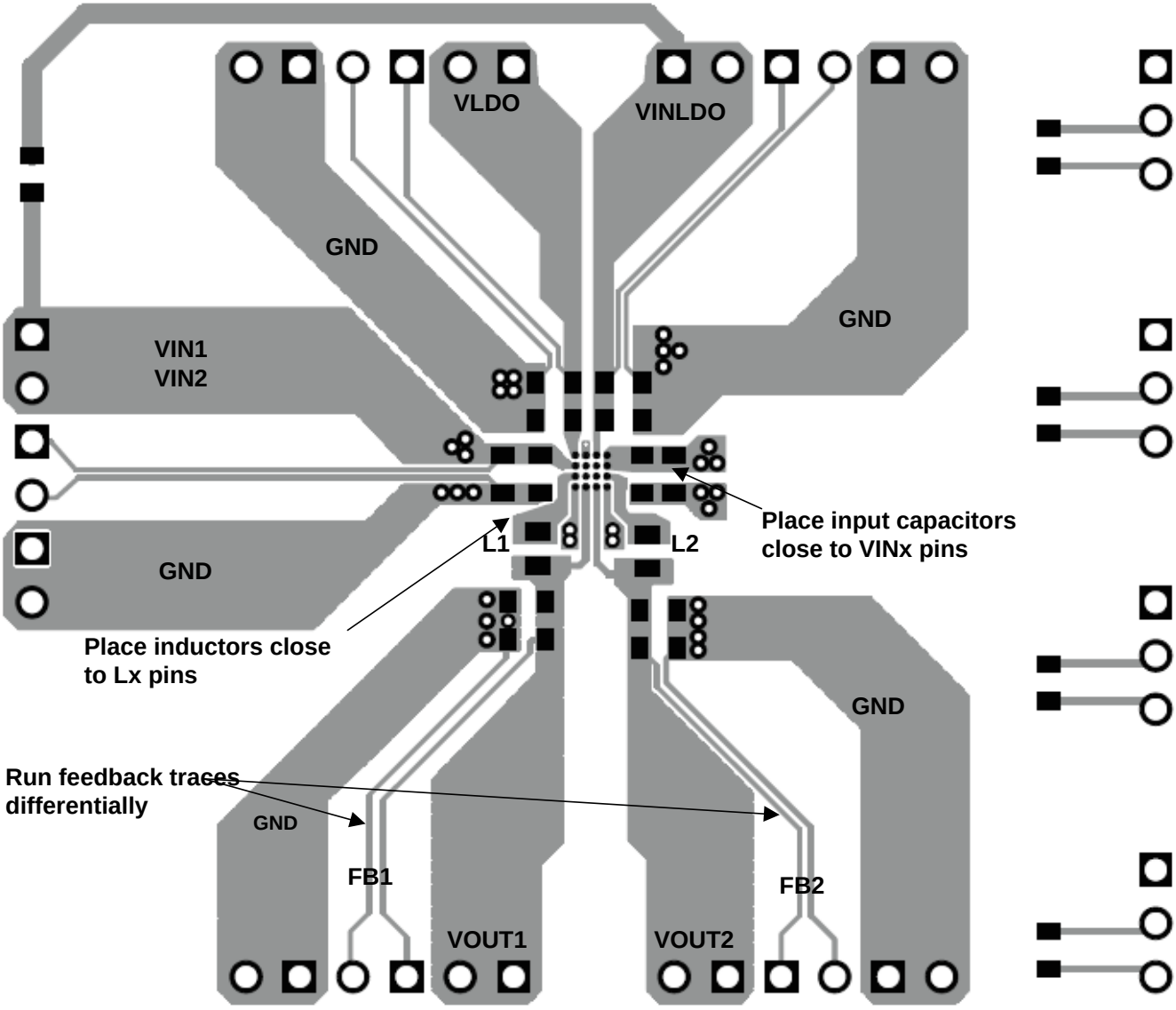


Figure 24. Layout Recommendation

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS657051	Click here	Click here	Click here	Click here	Click here
TPS657052	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS657051YZHT	ACTIVE	DSBGA	YZH	16	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS657051	Samples
TPS657052YZHR	ACTIVE	DSBGA	YZH	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS657052	Samples
TPS657052YZHT	ACTIVE	DSBGA	YZH	16	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS657052	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

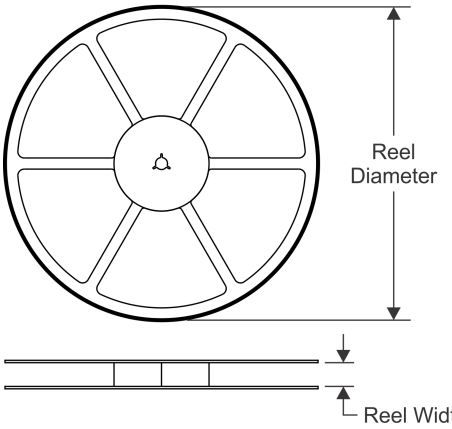
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

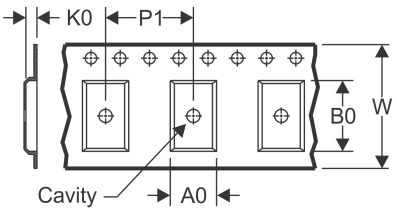
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

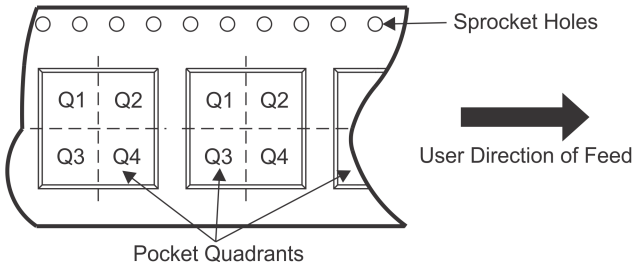


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

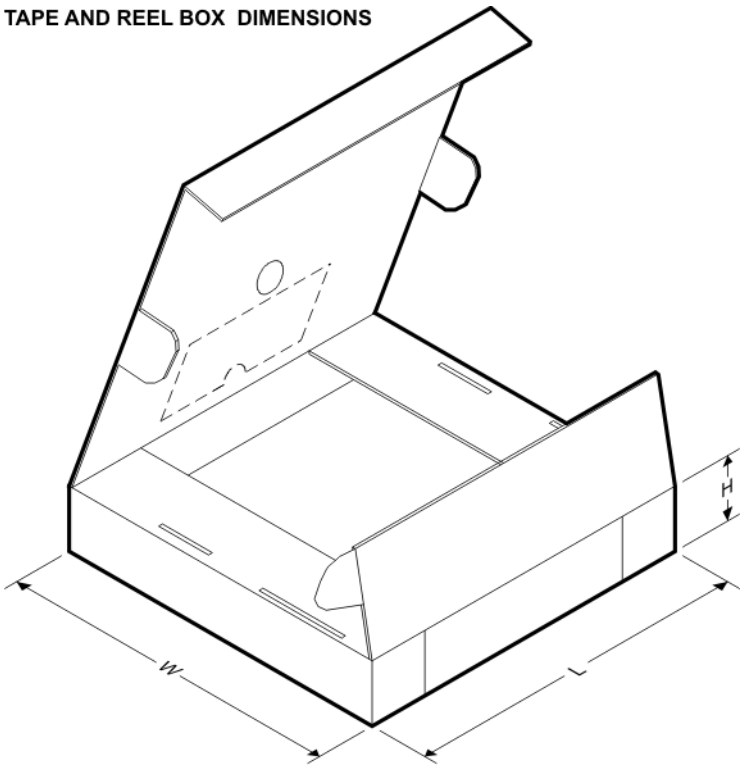
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

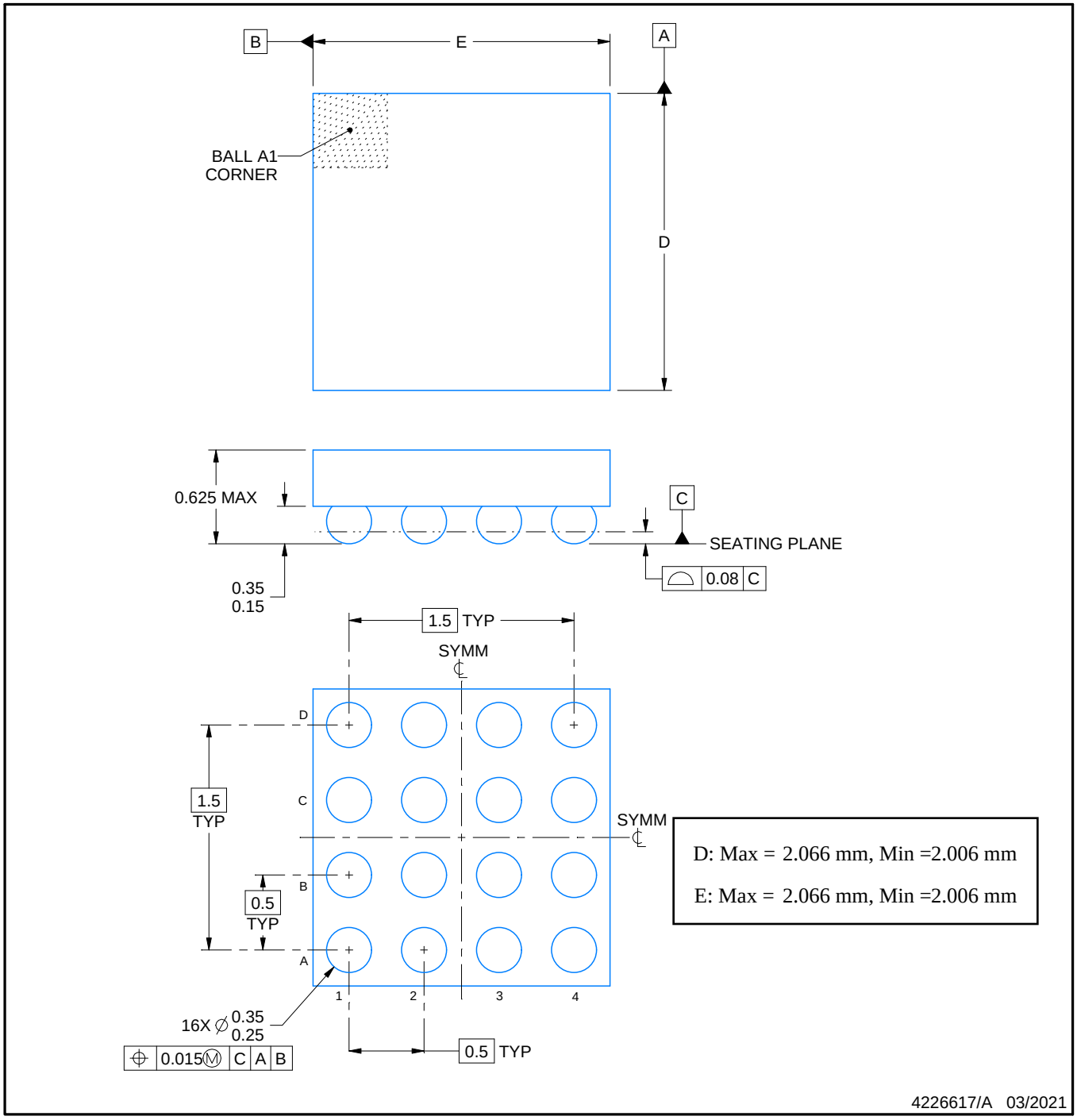
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS657051YZHT	DSBGA	YZH	16	250	180.0	8.4	2.18	2.18	0.81	4.0	8.0	Q1
TPS657052YZHR	DSBGA	YZH	16	3000	180.0	8.4	2.18	2.18	0.81	4.0	8.0	Q1
TPS657052YZHT	DSBGA	YZH	16	250	180.0	8.4	2.18	2.18	0.81	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



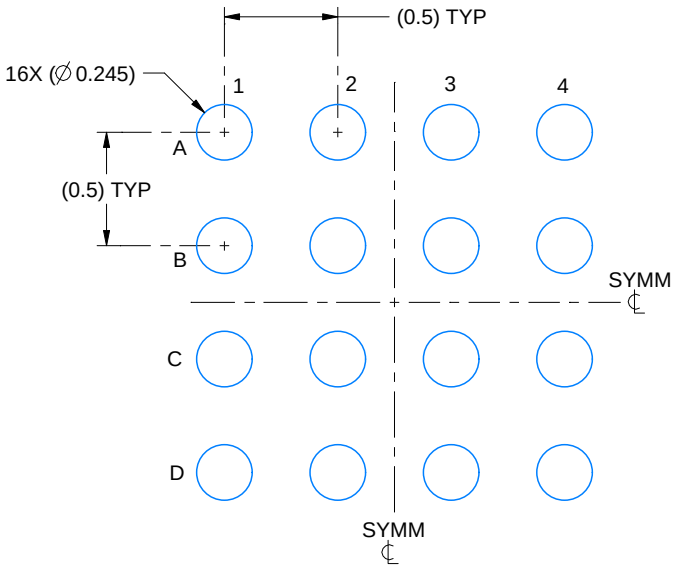
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS657051YZHT	DSBGA	YZH	16	250	182.0	182.0	20.0
TPS657052YZHR	DSBGA	YZH	16	3000	182.0	182.0	20.0
TPS657052YZHT	DSBGA	YZH	16	250	182.0	182.0	20.0

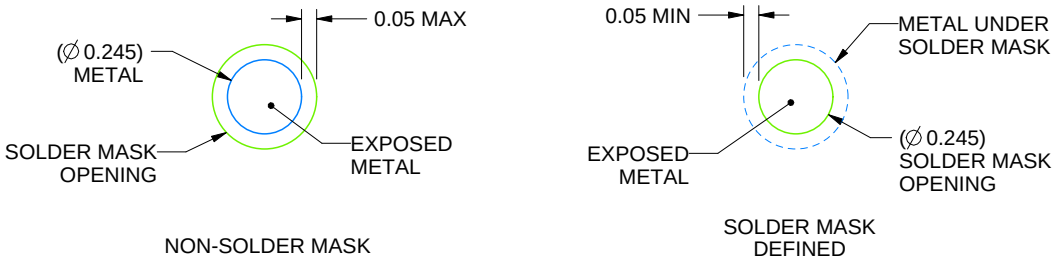


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS
NOT TO SCALE

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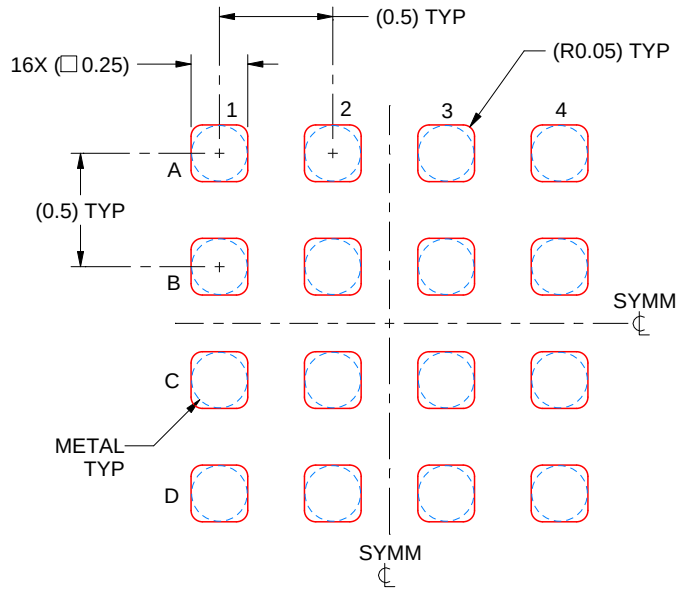
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 30X

4226617/A 03/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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