# TPS717xx 低噪声、高带宽 PSRR、低压降、150mA 线性稳压器

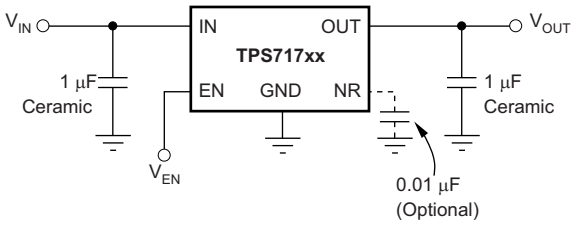
## 1 特性

- 输入电压：+2.5V 至 +6.5V
- 提供多个输出版本：
  - 固定输出电压范围：0.9V 至 5V
  - 可调节输出电压范围为 0.9V 至 6.2V
- 超高 PSRR：
  - 1kHz 时 70dB，100kHz 时 67dB，1MHz 时 45dB
- 出色的负载和线路瞬态响应
- 超低压降：150mA 时为 170mV（典型值）
- 低噪声：30μ$V_{RMS}$ 典型值（100Hz 至 100kHz）
- 小型 5 引脚 SC-70、2mm × 2mm 晶圆级小外形无引线 (WSON)-6 封装和 1.5mm × 1.5mm WSON-6 封装

## 2 应用

- 摄像机传感器电源
- 移动电话耳机
- 掌上电脑 (PDA) 和智能手机
- 无线 LAN， Bluetooth®

针对固定电压版本的典型应用电路




## 3 说明

TPS717xx 系列低压降 (LDO)、低功耗线性稳压器采用超小型 5 引脚小外形尺寸晶体管 (SOT) 封装，其具有非常高的电源抑制比 (PSRR)，同时能够保持 45μA 的超低接地电流。 该系列稳压器采用先进的双极 CMOS (BiCMOS) 工艺和功率金属氧化物半导体场效应晶体管 (PMOSFET) 无源器件，可实现快速启动、超低噪声、优异的瞬态响应以及出色的 PSRR 性能。 TPS717xx 器件与 1μF 陶瓷输出电容一起工作时可保持稳定，并且使用了一个精确的电压基准和反馈环路，以在所有负载、线路、过程和温度变化范围内实现至少 3% 的精度。 该器件系列的额定温度范围为 $T_J$ = -40°C 至 125°C，并且提供小型 SOT (SC70-5) 封装、带有散热焊盘的

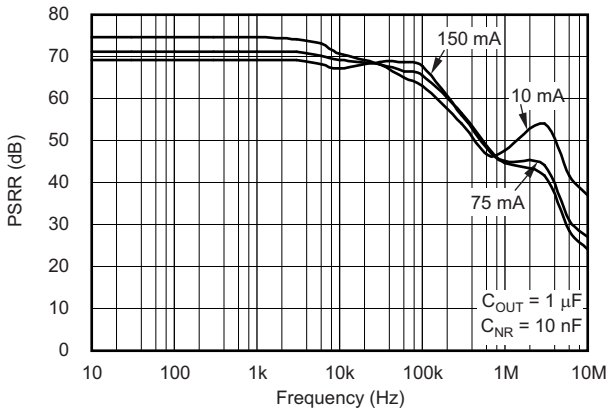
2mm × 2mm WSON-6 封装以及 1.5mm x 1.5mm WSON-6 封装，非常适合小尺寸便携式设备（例如无线手持设备和 PDA）。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TPS717xx | SC70 (5) | 2.00mm × 1.25mm |
| | WSON (6) | 2.00mm x 2.00mm |
| | WSON (6) | 1.50mm x 1.50mm |

(1) 如需了解所有可用封装和电压选项，请见数据表末尾的可订购产品附录。

**PSRR 与频率间的关系**




Power-Supply Rejection Ratio ($V_{IN}$ – $V_{OUT}$ = 1 V)

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Typical Characteristics ... 6
7 **Detailed Description** ... 11
7.1 Overview ... 11
7.2 Functional Block Diagrams ... 11
7.3 Feature Description ... 12
7.4 Device Functional Modes ... 13
8 **Application and Implementation** ... 15
8.1 Application Information ... 15
8.2 Typical Applications ... 16
8.3 Do's and Don'ts ... 18
9 **Power Supply Recommendations** ... 18
10 **Layout** ... 19
10.1 Layout Guidelines ... 19
10.2 Layout Example ... 19
10.3 Power Dissipation ... 20
11 器件和文档支持 ... 22
11.1 器件支持 ... 22
11.2 文档支持 ... 22
11.3 商标 ... 22
11.4 静电放电警告 ... 22
11.5 术语表 ... 22
12 机械封装和可订购信息 ... 22

## 4 修订历史记录

**Changes from Revision G (April 2009) to Revision H** — **Page**

- Changed pin descriptions throughout *Pin Functions* table ... 3
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 4
- Changed load regulation typical specification from 120 µV to 70 µV to better reflect device performance ... 5
- Changed condition for $C_{NR}$ = none for $V_n$ parameter ... 5
- Changed Figure 1, Figure 2, Figure 3, and Figure 4: removed legend, added call-outs for clarity ... 6
- Changed titles of Figure 15, Figure 17, and Figure 25 ... 7
- Corrected input and output symbols in operational amplifiers in *Functional Block Diagrams* ... 11
- Changed *Undervoltage Lockout (UVLO)* section text: reworded for clarity ... 13
- Deleted *Reverse Current Protection* section ... 15

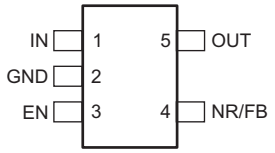
**Changes from Revision F (February 2009) to Revision G** — **Page**

- Changed min and max specs for *Output accuracy,* $V_{OUT} \geq 1.0V$ ... 5

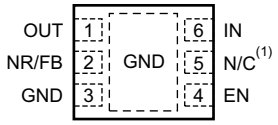

Copyright © 2006–2015, Texas Instruments Incorporated

# 5 Pin Configuration and Functions

**DCK Package**
**SC70-5**
**(Top View)**

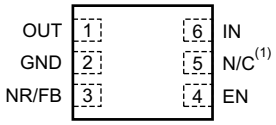



**DRV Package**
**2-mm × 2-mm WSON**
**(Top View)**




(1) N/C = No connection

**DSE Package**
**1.5-mm × 1.5-mm WSON**
**(Top View)**




## Pin Functions

| PIN | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | DCK | DRV | DSE | | |
| EN | 3 | 4 | 4 | I | Driving the enable pin (EN) above $V_{EN(high)}$ turns on the regulator. Driving this pin below $V_{EN(low)}$ puts the regulator into standby mode, thereby disabling the output and reducing operating current. |
| FB | 4 | 2 | 3 | I | Adjustable voltage version only. The voltage at this pin is fed to the error amplifier. A resistor divider from OUT to FB sets the output voltage when in regulation. |
| GND | 2 | 3 | 2 | — | Ground |
| IN | 1 | 6 | 6 | I | Input to the device. A 0.1-µF to 1-µF capacitor is recommended for better performance. |
| N/C | — | 5 | 5 | — | Not connected. This pin can be tied to ground to improve thermal dissipation. |
| NR | 4 | 2 | 3 | — | Fixed voltage versions only. The noise reduction capacitor filters the noise generated by the internal band gap, thus lowering output noise. |
| OUT | 5 | 1 | 1 | O | This pin is the regulated output voltage. A minimum capacitance of 1 µF is required for stability from this pin to ground. |

Copyright © 2006–2015, Texas Instruments Incorporated

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted), all voltages are with respect to GND[1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | $V_{IN}$ | –0.3 | 7 | V |
| | $V_{FB}$ | –0.3 | 3.6 | V |
| | $V_{NR}$ | –0.3 | 3.6 | V |
| | $V_{EN}$ | –0.3 | $V_{IN}$ + 0.3 V[2] | V |
| | $V_{OUT}$ | –0.3 | 7 | V |
| Current | $I_{OUT}$ | Internally limited | | A |
| Continuous total power dissipation | $P_{DISS}$ | See *Thermal Information* | | |
| Operating junction temperature | $T_J$ | –55 | 150 | °C |
| Storage temperature | $T_{stg}$ | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) $V_{EN}$ absolute maximum rating is $V_{IN}$ + 0.3 V or 7 V, whichever is greater.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1] | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2] | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 2.5 | | 6.5 | V |
| $V_{OUT}$ | Output voltage | 0.9 | | 5 | V |
| $I_{OUT}$ | Output current | 0 | | 150 | mA |
| $V_{EN}$ | Enable voltage | 0 | | $V_{IN}$ | V |
| $C_{OUT}$ | Output capacitor | 1 | | 100 | µF |
| $T_J$ | Junction temperature | –40 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TPS717xx | | | UNIT |
|---|---|---|---|---|---|
| | | DCK | DRV | DSE | |
| | | 5 PINS | 6 PINS | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 279.2 | 71.1 | 190.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 57.5 | 96.5 | 94.9 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 74.1 | 40.5 | 149.3 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.8 | 2.7 | 6.4 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 73.1 | 40.9 | 152.8 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | 10.7 | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.


Copyright © 2006–2015, Texas Instruments Incorporated

## 6.5 Electrical Characteristics

Over operating temperature range ($T_J$ = –40°C to 125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; $I_{OUT}$ = 0.5 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1.0 µF, $C_{NR}$ = 0.01 µF, unless otherwise noted. For TPS71701, $V_{OUT}$ = 2.8 V. Typical values are at $T_J$ = 25°C.

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range (1) | | | | 2.5 | | 6.5 | V |
| $V_{FB}$ | Internal reference (TPS71701) | | | | 0.790 | 0.800 | 0.810 | V |
| $V_{OUT}$ | Output voltage range | (TPS717xx) | | | 0.9 | | 5.0 | V |
| | | (TPS71701) | | | 0.9 | | 6.5 – $V_{DO}$ | V |
| $V_{OUT}$ | Output accuracy | Nominal | $T_J$ = 25°C | | | ±2.5 | | mV |
| | Output accuracy ($V_{OUT}$ < 1.0 V) | Over $V_{IN}$, $I_{OUT}$, Temp (2) | $V_{OUT}$ + 0.5 V ≤ $V_{IN}$ ≤ 6.5 V<br>0 mA ≤ $I_{OUT}$ ≤ 150 mA | | –30 | | +30 | mV |
| | Output accuracy ($V_{OUT}$ ≥ 1.0 V) | Over $V_{IN}$, $I_{OUT}$, Temp (2) | $V_{OUT}$ + 0.5 V ≤ $V_{IN}$ ≤ 6.5 V<br>0 mA ≤ $I_{OUT}$ ≤ 150 mA | | –3.0% | | +3.0% | |
| $\Delta V_{OUT(\Delta VIN)}$ | Line regulation (1) | | $V_{OUT(nom)}$ + 0.5 V ≤ $V_{IN}$ ≤ 6.5 V,<br>$I_{OUT}$ = 5 mA | | | 125 | | µV/V |
| $\Delta V_{OUT(\Delta IOUT)}$ | Load regulation | | 0 mA ≤ $I_{OUT}$ ≤ 150 mA | | | 70 | | µV/mA |
| $V_{DO}$ | Dropout voltage (3)<br>($V_{IN}$ = $V_{OUT(nom)}$ – 0.1 V) | | $I_{OUT}$ = 150 mA | | | 170 | 300 | mV |
| $I_{LIM}$ (fixed) | Output current limit (fixed output) | | $V_{OUT}$ = 0.9 × $V_{OUT(nom)}$ | | 200 | 325 | 575 | mA |
| $I_{LIM}$ (adjustable) | Output current limit (TPS71701) | | $V_{OUT}$ = 0.9 × $V_{OUT(nom)}$ | | 200 | 325 | 575 | mA |
| $I_{GND}$ | Ground pin current | | $I_{OUT}$ = 0.1 mA | | | 45 | 80 | µA |
| | | | $I_{OUT}$ = 150 mA | | | 100 | | µA |
| $I_{SHDN}$ | Shutdown current ($I_{GND}$) | | $V_{EN}$ ≤ 0.4 V,<br>$T_J$ = –40°C to 85°C | 2.5 V ≤ $V_{IN}$ < 4.5 V | | 0.20 | 1.5 | µA |
| | | | | 4.5 V ≤ $V_{IN}$ ≤ 6.5 V | | 0.90 | | µA |
| $I_{FB}$ | Feedback pin current (TPS71701) | | | | | 0.02 | 1.0 | µA |
| PSRR | Power-supply rejection ratio | | $V_{IN}$ = 3.8 V,<br>$V_{OUT}$ = 2.8 V,<br>$I_{OUT}$ = 150 mA | f = 100 Hz | | 70 | | dB |
| | | | | f = 1 kHz | | 70 | | dB |
| | | | | f = 10 kHz | | 67 | | dB |
| | | | | f = 100 kHz | | 67 | | dB |
| | | | | f = 1 MHz | | 45 | | dB |
| $V_n$ | Output noise voltage | | BW = 100 Hz to 100 kHz,<br>$V_{IN}$ = 3.8 V,<br>$V_{OUT}$ = 2.8 V,<br>$I_{OUT}$ = 10 mA | $C_{NR}$ = none | | 95 × $V_{OUT}$ | | $\mu V_{RMS}$ |
| | | | | $C_{NR}$ = 0.001 µF | | 25 × $V_{OUT}$ | | $\mu V_{RMS}$ |
| | | | | $C_{NR}$ = 0.01 µF | | 12.5 × $V_{OUT}$ | | $\mu V_{RMS}$ |
| | | | | $C_{NR}$ = 0.1 µF | | 11.5 × $V_{OUT}$ | | $\mu V_{RMS}$ |
| $t_{STR}$ | Startup time | | $V_{OUT}$ = 90% $V_{OUT(nom)}$,<br>$R_L$ = 19 Ω,<br>$C_{OUT}$ = 1 µF | 0.9 V ≤ $V_{OUT}$ ≤ 1.6V, $C_{NR}$ = 0.001 µF | | 0.700 | | ms |
| | | | | 1.6 V < $V_{OUT}$ < $V_{MAX}$, $C_{NR}$ = 0.01 µF | | 0.160 | | ms |
| $V_{EN(high)}$ | Enable high (enabled) | | $V_{IN}$ ≤ 5.5 V | | 1.2 | | 6.5 (4) | V |
| | | | 5.5 V < $V_{IN}$ ≤ 6.5 V | | 1.25 | | 6.5 | V |
| $V_{EN(low)}$ | Enable low (shutdown) | | | | 0 | | 0.4 | V |
| $I_{EN(high)}$ | Enable pin current, enabled | | EN = 6.5 V | | | 0.02 | 1.0 | µA |
| UVLO | Undervoltage lockout | | $V_{IN}$ rising | | 2.41 | 2.45 | 2.49 | V |
| | Hysteresis | | $V_{IN}$ falling | | | 150 | | mV |
| $T_{sd}$ | Thermal shutdown temperature | | Shutdown, temperature increasing | | | 160 | | °C |
| | | | Reset, temperature decreasing | | | 140 | | °C |
| $T_J$ | Operating junction temperature | | | | –40 | | 125 | °C |

(1) Minimum $V_{IN}$ = $V_{OUT}$ + $V_{DO}$ or 2.5 V, whichever is greater.
(2) Does not include external resistor tolerances.
(3) $V_{DO}$ is not measured for devices with $V_{OUT(nom)}$ < 2.6 V because the minimum $V_{IN}$is 2.5 V.
(4) Maximum $V_{EN(high)}$ = $V_{IN}$ + 0.3 or 6.5 V, whichever is smaller.

Copyright © 2006–2015, Texas Instruments Incorporated

## 6.6 Typical Characteristics

Over operating temperature range ($T_J$ = –40°C to 125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; $I_{OUT}$ = 0.5 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, $C_{NR}$ = 0.01 µF, unless otherwise noted. For the adjustable version (TPS71701,) $V_{OUT}$ = 2.8 V. Typical values are at $T_A$ = 25°C.

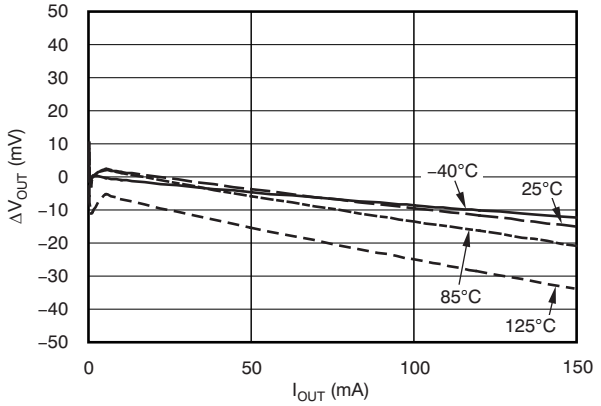



**Figure 1. Load Regulation**

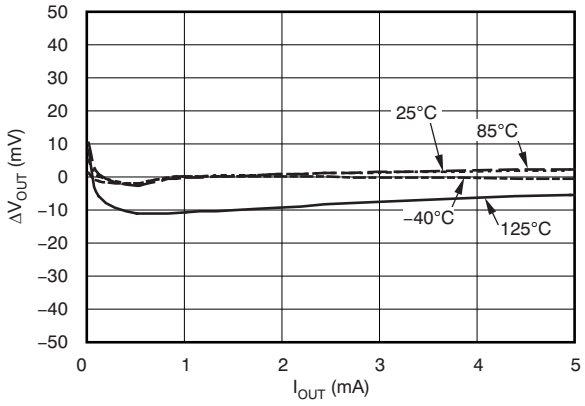



**Figure 2. Load Regulation Under Light Loads**

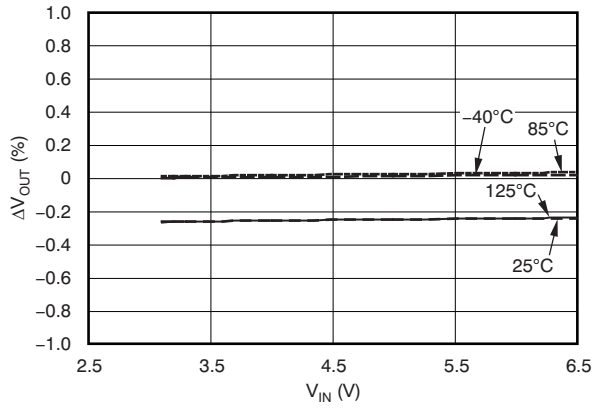



**Figure 3. Line Regulation ($I_{OUT}$ = 5 mA)**

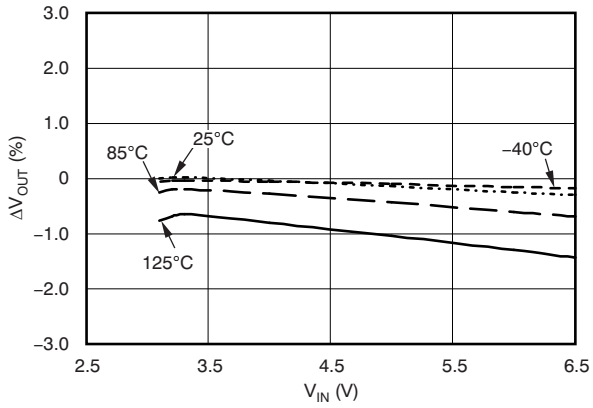



**Figure 4. Line Regulation ($I_{OUT}$ = 150 mA)**

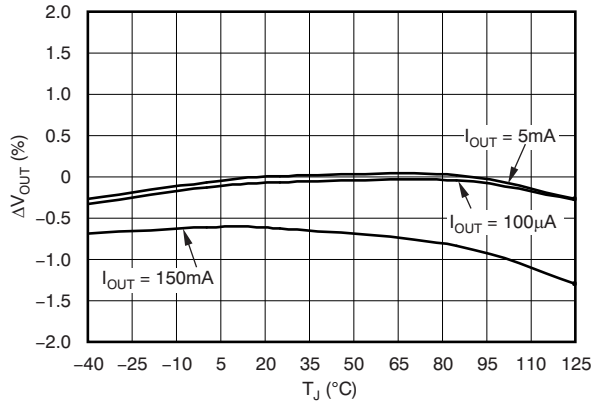



**Figure 5. Output Voltage vs Temperature**

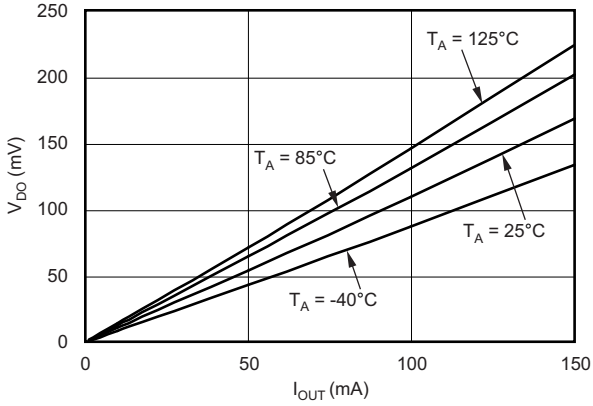



**Figure 6. Dropout Voltage vs Output Current**


Copyright © 2006–2015, Texas Instruments Incorporated

## Typical Characteristics (continued)

Over operating temperature range ($T_J$ = –40°C to 125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; $I_{OUT}$ = 0.5 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, $C_{NR}$ = 0.01 µF, unless otherwise noted. For the adjustable version (TPS71701,) $V_{OUT}$ = 2.8 V. Typical values are at $T_A$ = 25°C.

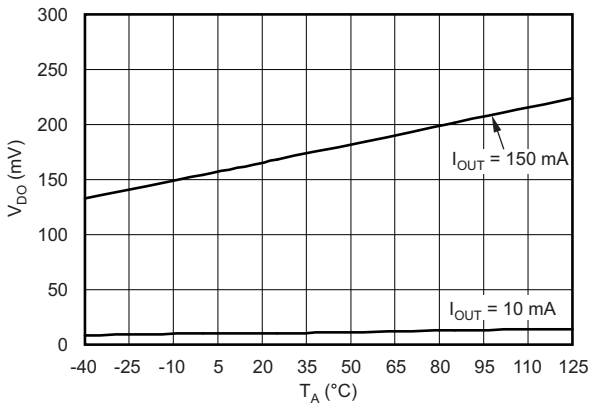



**Figure 7. Dropout Voltage vs Temperature**

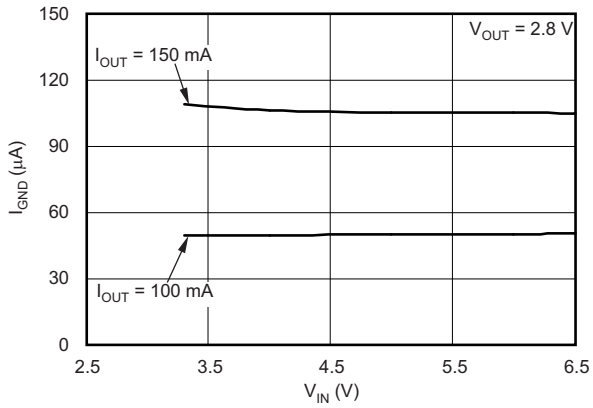



**Figure 8. Ground Pin Current vs Input Voltage**

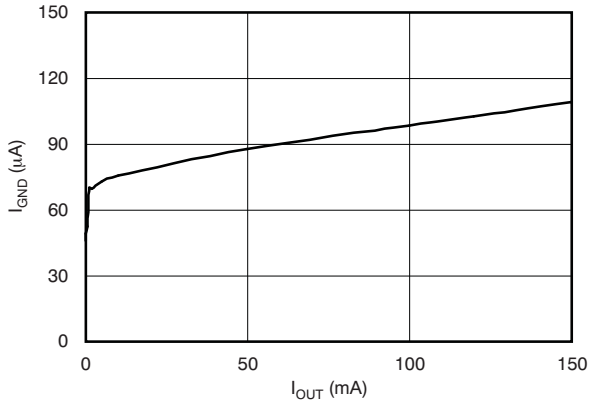



**Figure 9. Ground Pin Current vs Output Current**

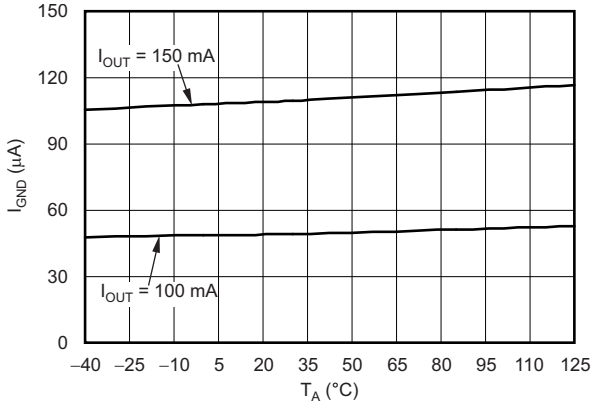



**Figure 10. Ground Pin Current vs Temperature (Enabled)**

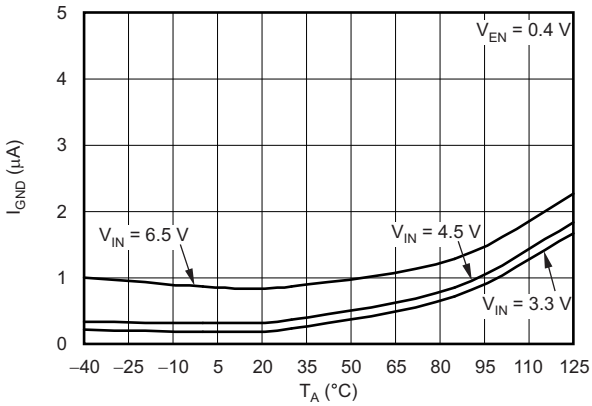



**Figure 11. Ground Pin Current vs Temperature (Disabled)**

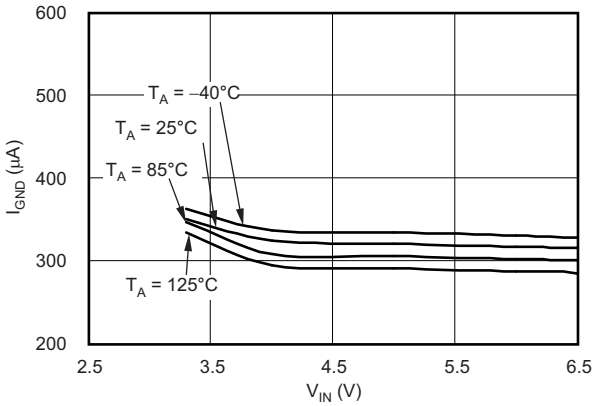



**Figure 12. Current Limit vs Input Voltage**

Copyright © 2006–2015, Texas Instruments Incorporated

## Typical Characteristics (continued)

Over operating temperature range ($T_J$ = –40°C to 125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; $I_{OUT}$ = 0.5 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, $C_{NR}$ = 0.01 µF, unless otherwise noted. For the adjustable version (TPS71701,) $V_{OUT}$ = 2.8 V. Typical values are at $T_A$ = 25°C.

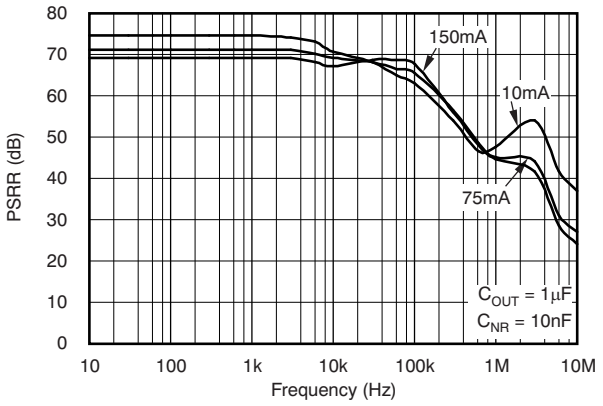



**Figure 13. Power-Supply Ripple Rejection vs Frequency ($V_{IN}$ – $V_{OUT}$ = 1 V)**

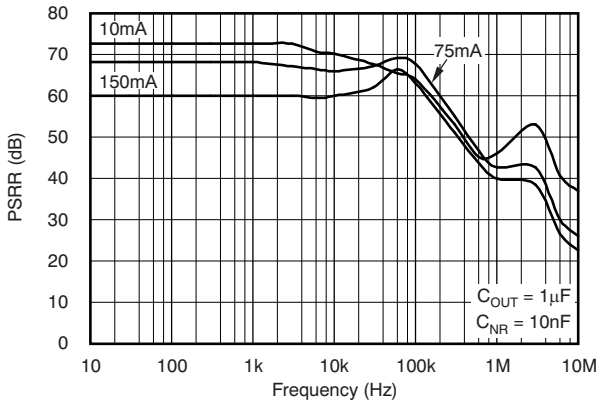



**Figure 14. Power-Supply Ripple Rejection vs Frequency ($V_{IN}$ – $V_{OUT}$ = 0.5 V)**

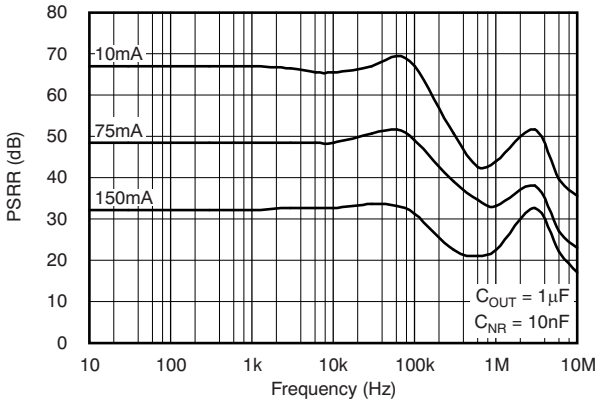



**Figure 15. Power-Supply Ripple Rejection vs Frequency in Dropout Conditions ($V_{IN}$ – $V_{OUT}$ = 0.25 V)**

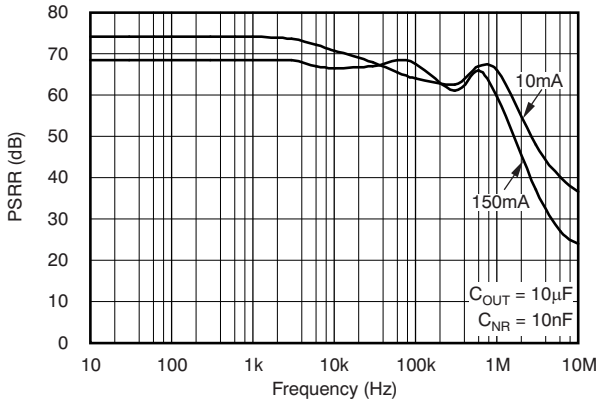



**Figure 16. Power-Supply Ripple Rejection vs Frequency ($V_{IN}$ – $V_{OUT}$ = 1 V)**

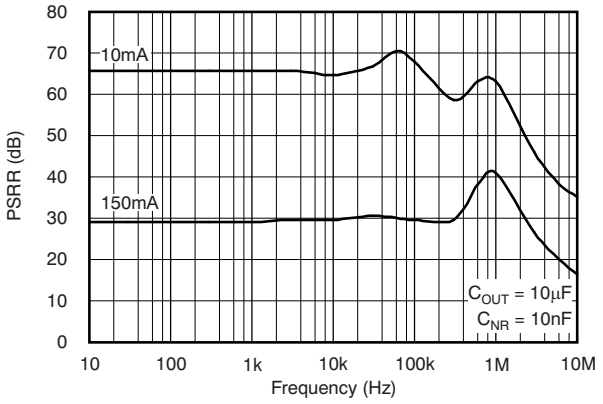



**Figure 17. Power-Supply Ripple Rejection vs Frequency in Dropout Conditions ($V_{IN}$ – $V_{OUT}$ = 0.25 V)**

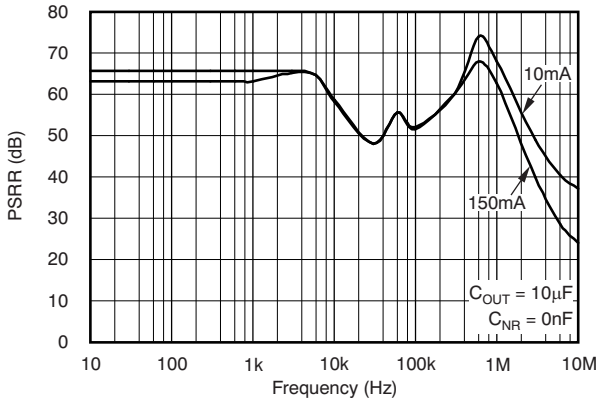



**Figure 18. Power-Supply Ripple Rejection vs Frequency ($V_{IN}$ – $V_{OUT}$ = 1 V)**


Copyright © 2006–2015, Texas Instruments Incorporated

## Typical Characteristics (continued)

Over operating temperature range ($T_J$ = –40°C to 125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; $I_{OUT}$ = 0.5 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, $C_{NR}$ = 0.01 µF, unless otherwise noted. For the adjustable version (TPS71701,) $V_{OUT}$ = 2.8 V. Typical values are at $T_A$ = 25°C.

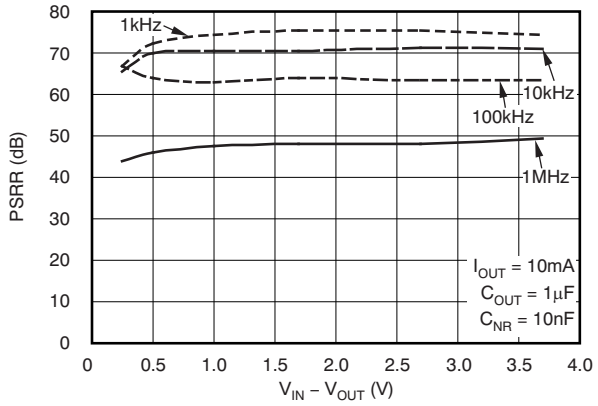



**Figure 19. Power-Supply Ripple Rejection vs ($V_{IN}$ – $V_{OUT}$)**

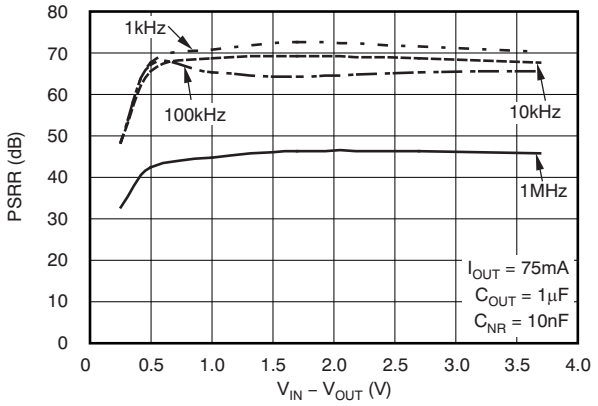



**Figure 20. Power-Supply Ripple Rejection vs ($V_{IN}$ – $V_{OUT}$)**

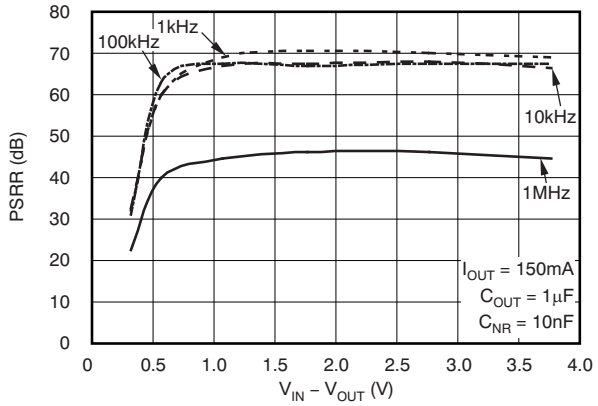



**Figure 21. Power-Supply Ripple Rejection vs ($V_{IN}$ – $V_{OUT}$)**

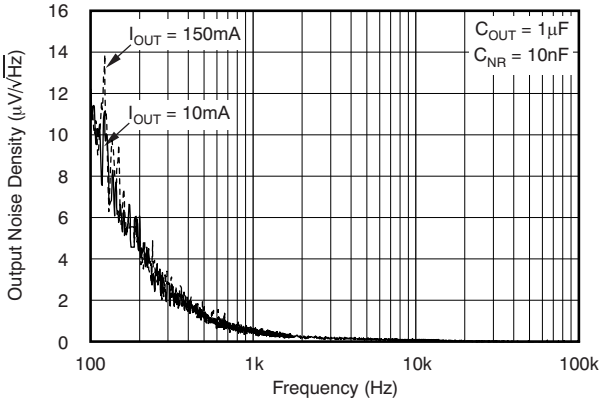



**Figure 22. Output Spectral Noise Density vs Output Current**

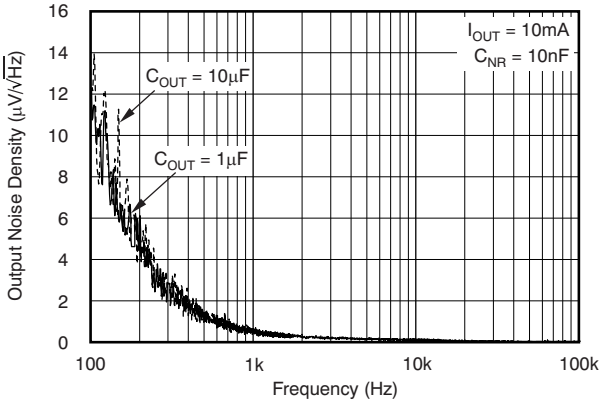



**Figure 23. Output Spectral Noise Density vs Output Capacitance**

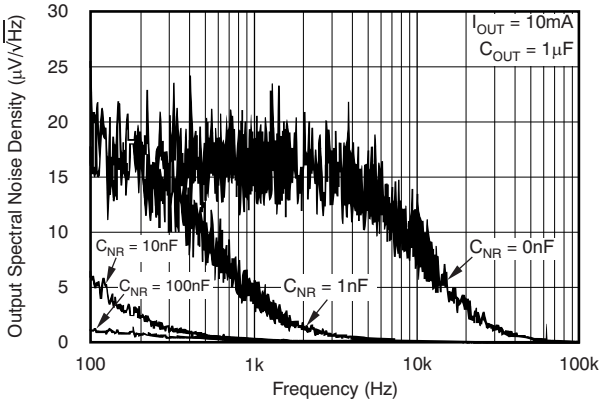



**Figure 24. Output Spectral Noise Density vs Noise Reduction**

Copyright © 2006–2015, Texas Instruments Incorporated

## Typical Characteristics (continued)

Over operating temperature range ($T_J$ = –40°C to 125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.5 V, whichever is greater; $I_{OUT}$ = 0.5 mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 1 µF, $C_{NR}$ = 0.01 µF, unless otherwise noted. For the adjustable version (TPS71701,) $V_{OUT}$ = 2.8 V. Typical values are at $T_A$ = 25°C.

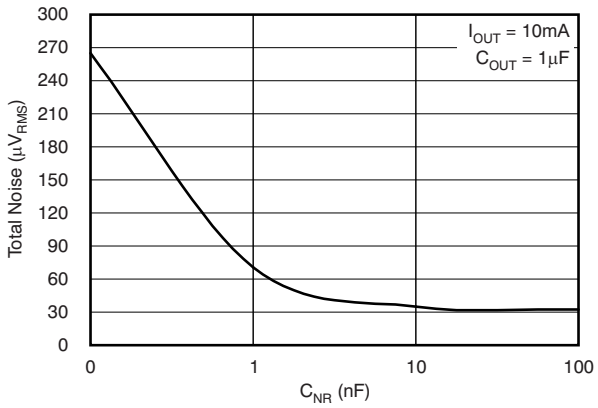



**Figure 25. Total Output Noise vs Noise Reduction Capacitor**

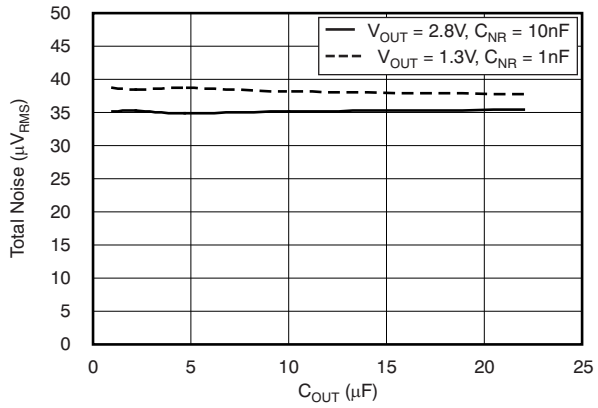



**Figure 26. Total Output Noise vs Output Capacitance**

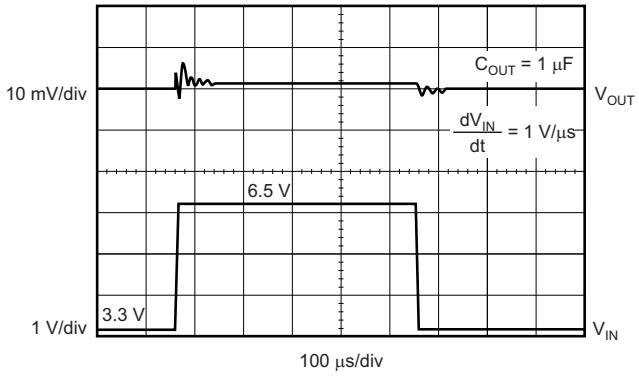



**Figure 27. Line Transient Response**

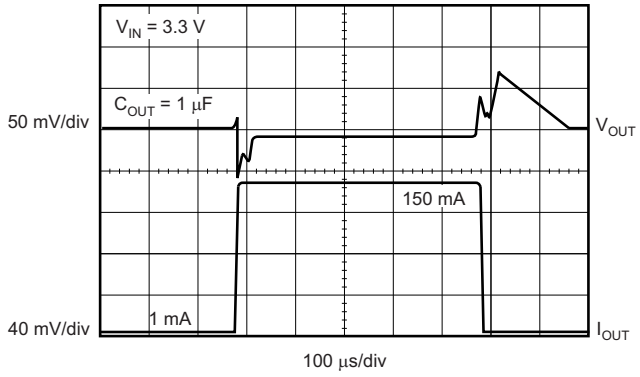



**Figure 28. Load Transient Response**

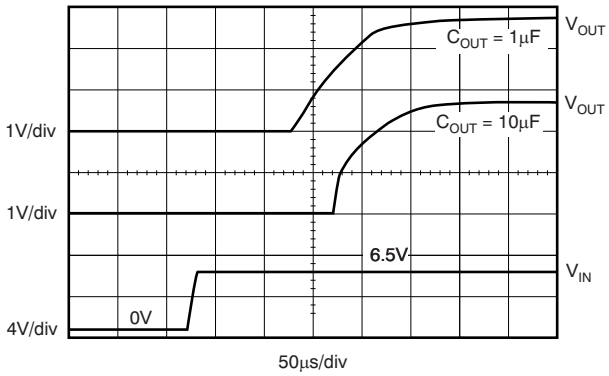



**Figure 29. Turn-On Response**

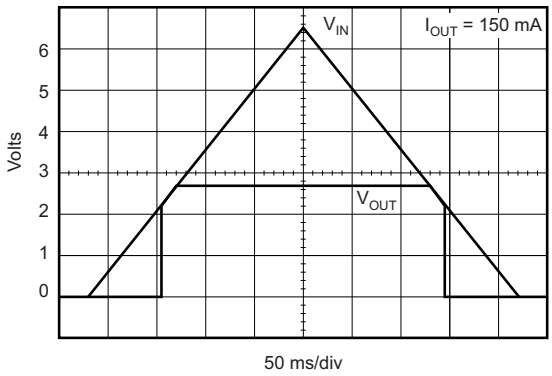



**Figure 30. Power-Up and Power-Down**


Copyright © 2006–2015, Texas Instruments Incorporated

# 7 Detailed Description

## 7.1 Overview

The TPS717xx family of low-dropout (LDO) regulators combines the high performance required by many RF and precision analog applications with ultra-low current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection with very low headroom ($V_{IN}$ – $V_{OUT}$). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the band-gap reference and to improve PSRR. A quick-start circuit fast-charges this capacitor at startup. The combination of high performance and low ground current also make the TPS717xx family of devices an excellent choice for battery-powered applications. All versions have thermal and overcurrent protection.

## 7.2 Functional Block Diagrams

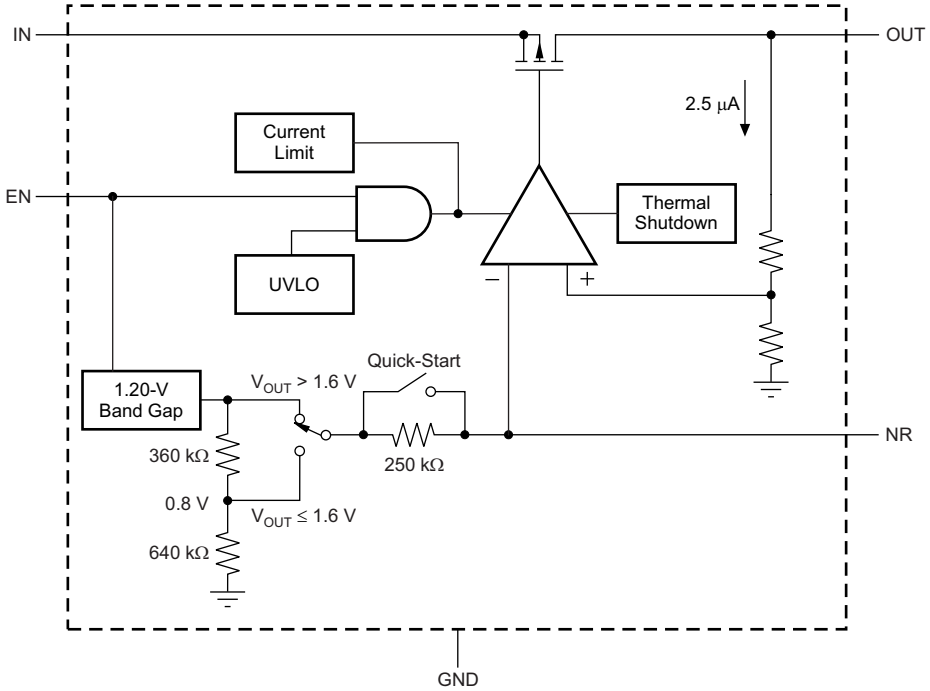



**Figure 31. Fixed Voltage Versions**

## Functional Block Diagrams (continued)

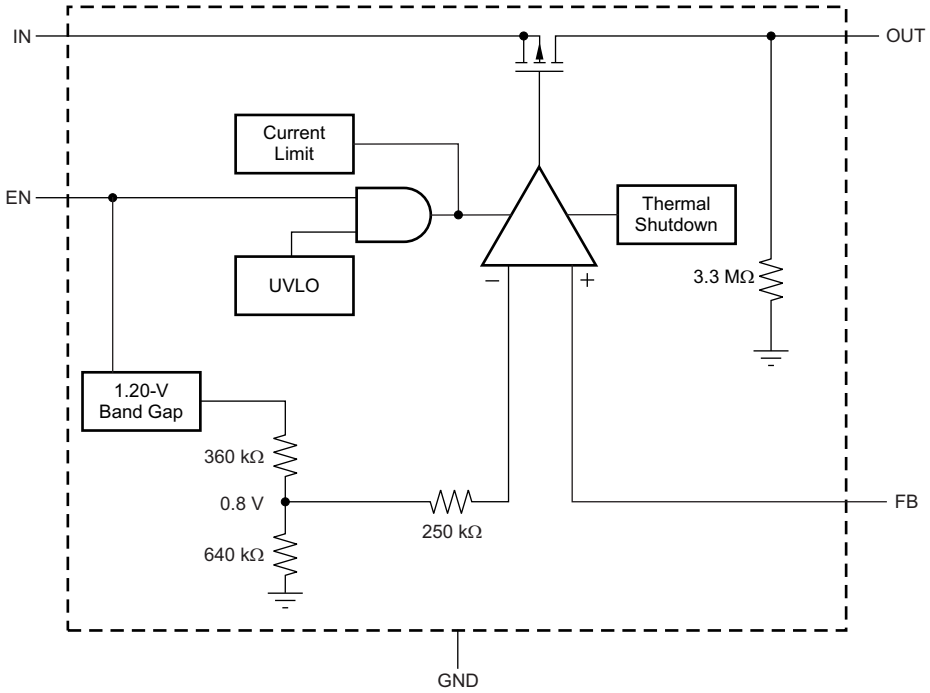



**Figure 32. Adjustable Voltage Version**

## 7.3 Feature Description

### 7.3.1 Internal Current Limit

The TPS717xx internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, do not operate the device in a current-limit state for extended periods of time.

The PMOS pass element in the TPS717xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

### 7.3.2 Shutdown

The enable pin (EN) is active high and compatible with standard and low voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

### 7.3.3 Startup and Noise Reduction Capacitor

Fixed voltage versions of the TPS717xx use a quick-start circuit to fast-charge the noise reduction capacitor, $C_{NR}$, if present (see Figure 31). This circuit allows the combination of very low output noise and fast start-up times. The NR pin is high impedance, so a low-leakage $C_{NR}$ capacitor must be used; most ceramic capacitors are appropriate in this configuration.

Note that for fastest startup, apply $V_{IN}$ first, then the enable pin (EN) driven high. If EN is tied to IN, startup is somewhat slower. Refer to Figure 29 in *Typical Characteristics*. The quick-start switch is closed for approximately 135 µs. To ensure that $C_{NR}$ is fully charged during the quick-start time, use a 0.01-µF or smaller capacitor.


Copyright © 2006–2015, Texas Instruments Incorporated

## Feature Description (continued)

For output voltages below 1.6 V, a voltage divider on the band-gap reference voltage is employed to optimize output regulation performance for lower output voltages. This configuration results in an additional resistor in the quick-start path and combined with the noise reduction capacitor ($C_{NR}$) results in slower start-up times for output voltages below 1.6 V.

Equation 1 approximates the start-up time as a function of $C_{NR}$ for output voltages below 1.6 V:

$$t_{START} = 160\mu s + (540 \frac{\mu s}{nF} \times C_{NR} nF)\mu s \quad (1)$$

### 7.3.4 Undervoltage Lockout (UVLO)

The TPS717xx uses an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a limited glitch immunity so undershoot transients are typically ignored on the input if these transients are less than 5 µs in duration.

### 7.3.5 Minimum Load

The TPS717xx is stable with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS717xx employs an innovative low-current mode circuit to increase loop gain under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

### 7.3.6 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 35°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS717xx is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS717xx into thermal shutdown degrades device reliability.

## 7.4 Device Functional Modes

### 7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage has previously exceeded the UVLO rising voltage and has not decreased below the UVLO falling threshold.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

Copyright © 2006–2015, Texas Instruments Incorporated

## Device Functional Modes (continued)

### 7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

### 7.4.3 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO falling voltage, or has not yet exceeded the UVLO rising threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 shows the conditions that lead to the different modes of operation.

**Table 1. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | | | |
|---|---|---|---|---|
| | $V_{IN}$ | $V_{EN}$ | $I_{OUT}$ | $T_J$ |
| Normal mode | $V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > UVLO$ | $V_{EN} > V_{EN(high)}$ | $I_{OUT} < I_{LIM}$ | $T_J < 125°C$ |
| Dropout mode | $UVLO < V_{IN} < V_{OUT(nom)} + V_{DO}$ | $V_{EN} > V_{EN(high)}$ | — | $T_J < 125°C$ |
| Disabled mode (any true condition disables the device) | $V_{IN} < UVLO – V_{hys}$ | $V_{EN} < V_{EN(low)}$ | — | $T_J > 165°C$ |


Copyright © 2006–2015, Texas Instruments Incorporated

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TPS717xx belongs to a family of new generation LDO regulators that use innovative circuitry to achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR at very low headroom ($V_{IN}$ – $V_{OUT}$). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the band-gap reference and to improve PSRR while a quick-start circuit fast-charges this capacitor. These features, combined with low noise, enable, low ground pin current, and ultra-small packaging, make this part ideal for automotive applications. This family of regulators offers sub-band-gap output voltages, current limit, and thermal protection, and is fully specified from –40°C to 125°C.

### 8.1.1 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot or undershoot magnitude but increases duration of the transient. The TPS717xx has an ultra-wide loop bandwidth that allows it to respond quickly to load transient events. As with any regulator, the loop bandwidth is finite and the initial transient voltage peak is controlled by the sizing of the output capacitor. Typically, larger output capacitors reduce the peak while also reducing the bandwidth of the LDO, slowing the response time.

### 8.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-μF or larger low equivalent series resistance (ESR) capacitor from IN to GND near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-μF input capacitor may be necessary to ensure stability.

The TPS717xx is designed to be stable with ceramic output capacitors of values 1 μF or larger. The X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. The maximum ESR of the output capacitor must be less than 1 Ω.

### 8.1.3 Dropout Voltage

The TPS717xx uses a PMOS pass transistor to achieve low dropout. When ($V_{IN}$ – $V_{OUT}$) is less than the dropout voltage ($V_{DO}$), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DSon}$ of the PMOS pass element. $V_{DO}$ scales approximately with output current because the PMOS device functions as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded when ($V_{IN}$ – $V_{OUT}$) approaches dropout. This effect is illustrated in Figure 15 through Figure 17 in *Typical Characteristics*.

Copyright © 2006–2015, Texas Instruments Incorporated

## Application Information (continued)

### 8.1.4 Output Noise

In most LDOs, the band gap is the dominant noise source. If a noise reduction capacitor ($C_{NR}$) is used with the TPS717xx, the band gap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01-µF (minimum) noise reduction capacitor; for the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that gives 2.5 µA of divider current has the same noise performance as a fixed voltage version.

Equation 2 approximates the total noise referred to the feedback point (FB pin) when $C_{NR}$ = 0.01 µF:

$$V_N = 11.5 \frac{\mu V_{RMS}}{V} \times V_{OUT} \tag{2}$$

## 8.2 Typical Applications

### 8.2.1 Application for Fixed Voltage Versions and Adjustable Voltage Version

Figure 33 shows the basic circuit connections for the fixed voltage options. Figure 34 gives the connections for the adjustable output version (TPS71701). **Note that the NR pin is not available on the adjustable version**.

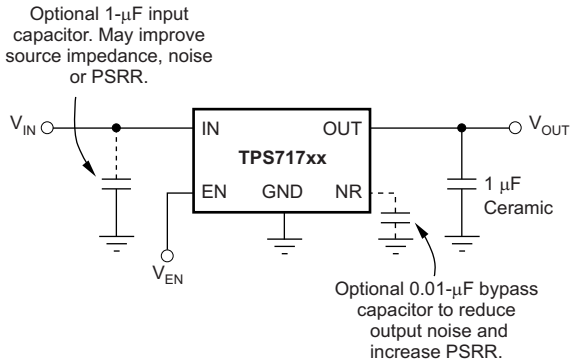



**Figure 33. Typical Application Circuit (Fixed Voltage Versions)**

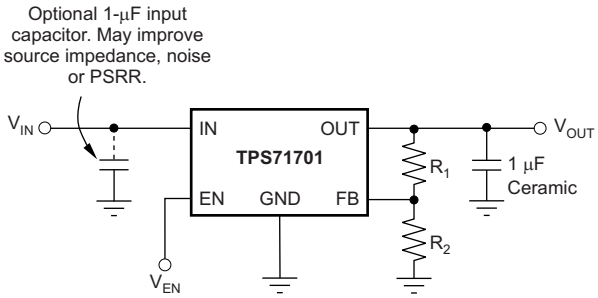



**Figure 34. Typical Application Circuit (Adjustable Voltage Version)**

#### *8.2.1.1 Design Requirements*

Table 2 summarizes the design requirements for Figure 36.

**Table 2. Design Parameters**

| PARAMETER | DESIGN REQUIREMENT |
|---|---|
| Input voltage | 3.3 V, ±10% |
| Output voltage | 2.8 V, ±5% |
| Output current | 100 mA typical, 150 mA peak |
| Output voltage transient deviation | 5% |
| Maximum ambient temperature | 85°C |

#### *8.2.1.2 Detailed Design Procedure*

For the adjustable version (TPS71701), the NR pin is replaced with a feedback (FB) pin. The voltage on this pin sets the output voltage and is determined by the values of $R_1$ and $R_2$. The values of $R_1$ and $R_2$ can be calculated for any voltage using the formula given in Equation 3:

$$R_1 = R_2 * (V_{OUT} / V_{REF} - 1) \tag{3}$$

The value of $R_2$ directly impacts the operation of the device and must be chosen in the range of approximately 160 kΩ to 320 kΩ. Sample resistor values for common output voltages are shown in Table 3.


Copyright © 2006–2015, Texas Instruments Incorporated

**Table 3. Sample 1% Resistor Values for Common Output Voltages**

| $V_{OUT}$ | $R_1$ | $R_2$ |
|---|---|---|
| 1 | 80.6 kΩ | 324 kΩ |
| 1.2 | 162 kΩ | 324 kΩ |
| 1.5 | 294 kΩ | 332 kΩ |
| 1.8 | 402 kΩ | 324 kΩ |
| 2.5 | 665 kΩ | 316 kΩ |
| 3.3 | 1.02 MΩ | 324 kΩ |
| 5 | 1.74 MΩ | 332 kΩ |

#### *8.2.1.3 Application Curve*

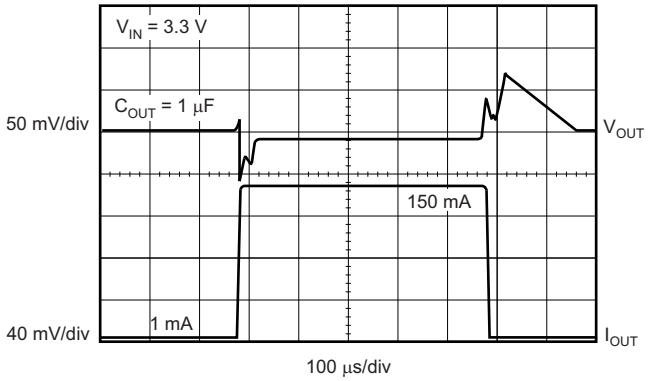



**Figure 35. Load Transient Response**

### 8.2.2 Powering a PLL Integrated on an SOC

Figure 36 shows the TPS71701 powering a phase-locked loop (PLL) that is integrated into a system-on-a-chip (SOC).

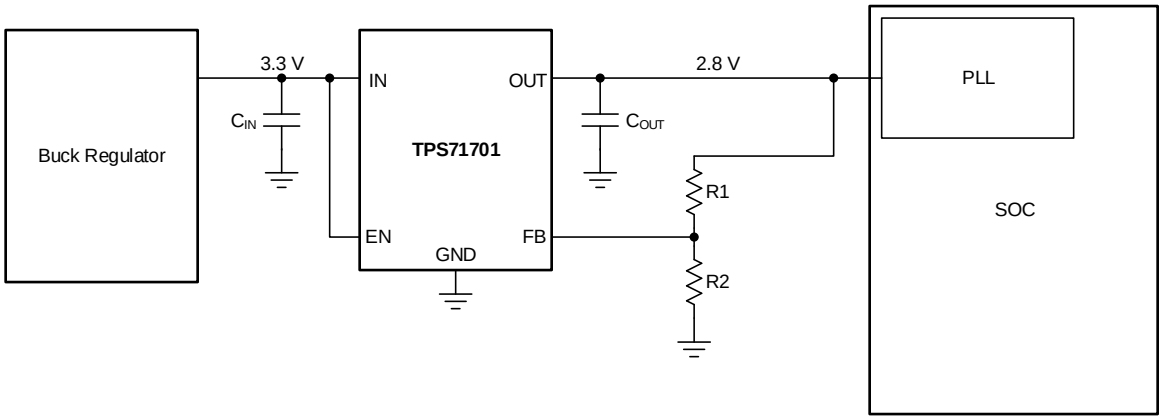



**Figure 36. Typical Application Circuit: PLL on an SOC**

Use the input and output capacitors to ensure the voltage transient requirements. A 1-µF input and 1-µF output capacitor are selected to maximize the capacitance and minimize capacitor size.

$R_2$ is chosen to be 158 kΩ for optimal noise and PSRR, and by Equation 4, $R_1$ is selected to be 402 kΩ. Both $R_1$ and $R_2$ must be 1% tolerance resistors to meet the dc accuracy specification over line, load, and temperature.

### 8.3 Do's and Don'ts

Do place at least one 1-µF ceramic capacitor as close as possible in the range of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Do not place any components in the feedback loop except for the output capacitor and feedback resistors.

Do not exceed the device absolute maximum ratings.

Do not float the enable (EN) pin.

## 9 Power Supply Recommendations

The TPS717xx is designed to operate from an input voltage between 2.5 V and 6.5 V. The input supply must provide adequate headroom for the device to operate in a normal mode of operation.

Connect a low output impedance power supply directly to the IN pin of the TPS717xx. Inductive impedances between the input supply and the IN pin can create significant voltage excursions at the IN pin during startup or load transient events. If inductive impedances are unavoidable, use an input capacitor. To increase the overall PSRR of the power solution, use a pi-filter before the input of the LDO or after the FB network of the LDO.


Copyright © 2006–2015, Texas Instruments Incorporated

# 10 Layout

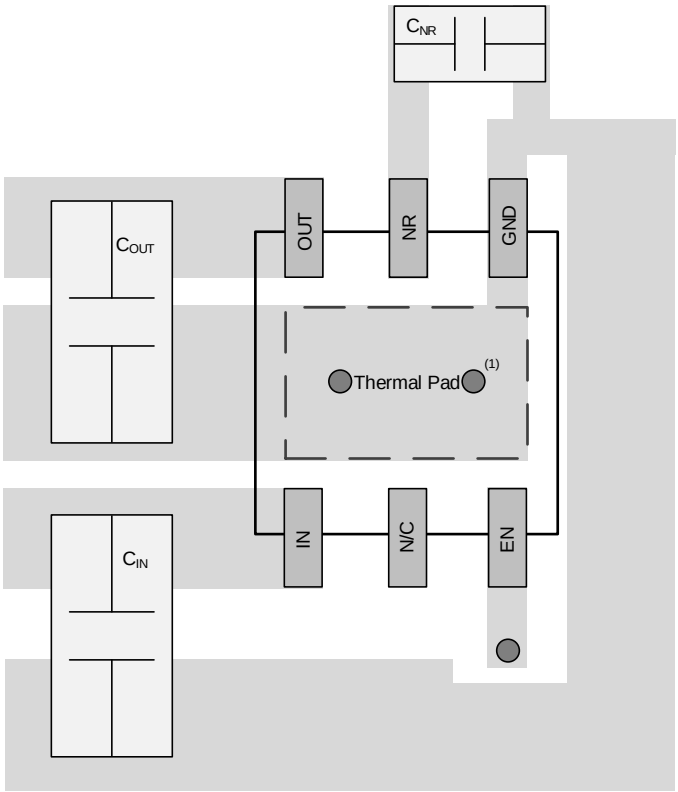
## 10.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to the GND pin as possible, connected by wide, component-side, copper surface area. The use of vias and long traces to create LDO component connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the printed circuit board (PCB) itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shields the LDO from noise, and functions similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

### 10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for $V_{IN}$ and $V_{OUT}$, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

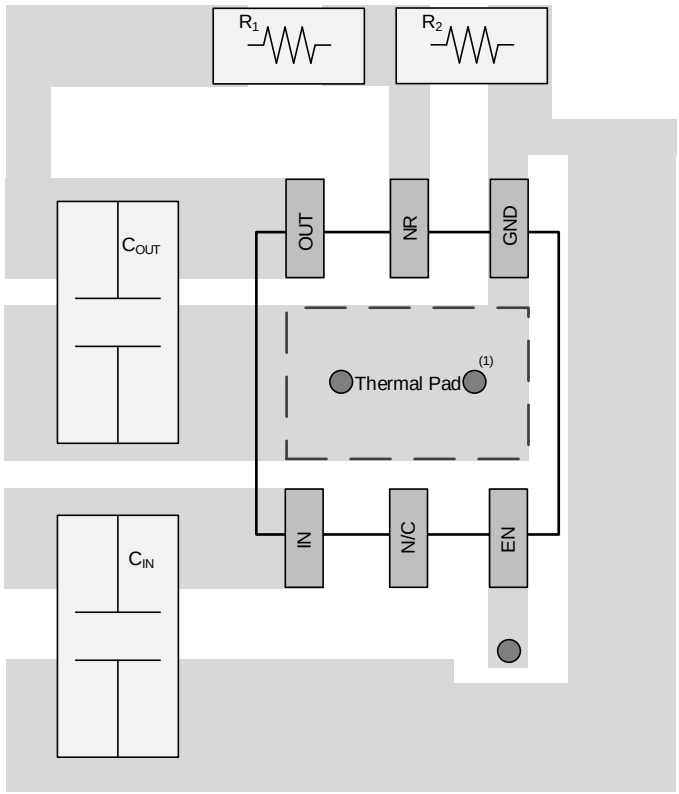
## 10.2 Layout Example




(1) Circles within thermal pad area indicate vias to other layers on the board, for electrical connections or thermal conduction.

**Figure 37. Fixed Voltage Layout**

## Layout Example (continued)




(1) Circles within thermal pad area indicate vias to other layers on the board, for electrical connections or thermal conduction.

**Figure 38. Adjustable Voltage Layout**

## 10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation ($P_D$) is equal to the product of the output current times the voltage drop across the output pass element ($V_{IN}$ to $V_{OUT}$), as shown in Equation 4:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{4}$$

A better method of estimating the thermal measure comes from using the thermal metrics $\Psi_{JT}$ and $\Psi_{JB}$, shown in *Thermal Information*. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with Equation 5.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D$$

where

- $P_D$ is the power dissipation shown by Equation 4,
- $T_T$ is the temperature at the center-top of the IC package,
- $T_B$ is the PCB temperature measured 1 mm away from the IC package *on the PCB surface*. (5)


版权 © 2006–2015, Texas Instruments Incorporated

## Power Dissipation (接下页)

**NOTE**

Both $T_T$ and $T_B$ can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring $T_T$ and $T_B$, see the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

# 11 器件和文档支持

## 11.1 器件支持

### 11.1.1 开发支持

#### *11.1.1.1 评估模块*

评估模块 (EVM) 可与 TPS717 配套使用，帮助评估初始电路性能。 TPS717xxEVM-134 评估模块（和相关的用户指南）可在德州仪器 (TI) 网站上的产品文件夹中获取，也可直接从 TI 网上商店购买。

### 11.1.2 器件命名规则

表 **4.** 器件命名规则(1)

| 产品 | $V_{OUT}$ |
|---|---|
| TPS717**xx(x)yyyz** | **xx(x)** 为标称输出电压。 对于分辨率为 100mV 的输出电压，订货编号中使用两位数字；否则，使用三位数字（例如，28 = 2.8V；125 = 1.25V）。 **01** 表示可调电压版本。<br>**yyy** 为封装标识符。<br>**z** 为封装数量。 R 表示卷（3000 片），T 表示带（250 片）。 |

(1) 要获得最新的封装和订货信息，请参见本文档末尾的封装选项附录，或者访问器件产品文件夹（www.ti.com）。

## 11.2 文档支持

### 11.2.1 相关文档

*《TPS717xxEVM-134 评估模块用户指南》*，SLVU148

## 11.3 商标

Bluetooth is a registered trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

## 11.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 11.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

# 12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。


版权 © 2006–2015, Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS71701DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BMT | Samples |
| TPS71701DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BMT | Samples |
| TPS71701DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BMT | Samples |
| TPS71701DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BMT | Samples |
| TPS71709DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | FY | Samples |
| TPS71709DSERG4 | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | FY | Samples |
| TPS71709DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | FY | Samples |
| TPS71709DSETG4 | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | FY | Samples |
| TPS71710DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BMU | Samples |
| TPS71710DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BMU | Samples |
| TPS71710DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BMU | Samples |
| TPS71710DRVR | ACTIVE | WSON | DRV | 6 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | BMU | Samples |
| TPS71710DRVT | ACTIVE | WSON | DRV | 6 | 250 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | BMU | Samples |
| TPS71711DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BRL | Samples |
| TPS71711DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BRL | Samples |
| TPS71711DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BRL | Samples |
| TPS71711DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BRL | Samples |
| TPS71712DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CKE | Samples |
| TPS71712DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CKE | Samples |
| TPS71712DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CKE | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS71712DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CKE | Samples |
| TPS71713DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BMW | Samples |
| TPS71713DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BMW | Samples |
| TPS71715DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CAA | Samples |
| TPS71715DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CAA | Samples |
| TPS71715DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CAA | Samples |
| TPS717185DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | KB | Samples |
| TPS717185DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | KB | Samples |
| TPS71718DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BMX | Samples |
| TPS71718DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BMX | Samples |
| TPS71718DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BMX | Samples |
| TPS71718DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BMX | Samples |
| TPS71718DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | G6 | Samples |
| TPS71718DSERG4 | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | G6 | Samples |
| TPS71718DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | G6 | Samples |
| TPS71719DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CCZ | Samples |
| TPS71719DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CCZ | Samples |
| TPS71719DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CCZ | Samples |
| TPS71719DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CCZ | Samples |
| TPS71721DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NXL | Samples |
| TPS71721DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NXL | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS71725DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CAF | Samples |
| TPS71725DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CAF | Samples |
| TPS71725DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CAF | Samples |
| TPS71726DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BRK | Samples |
| TPS71726DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BRK | Samples |
| TPS71727DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BSC | Samples |
| TPS71727DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BSC | Samples |
| TPS71727DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BSC | Samples |
| TPS71727DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | KU | Samples |
| TPS71727DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | KU | Samples |
| TPS717285DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BRJ | Samples |
| TPS717285DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BRJ | Samples |
| TPS71728DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BMZ | Samples |
| TPS71728DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BMZ | Samples |
| TPS71728DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BMZ | Samples |
| TPS71728DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | FU | Samples |
| TPS71728DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | FU | Samples |
| TPS71728DSETG4 | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | FU | Samples |
| TPS71729DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CJR | Samples |
| TPS71729DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CJR | Samples |
| TPS71730DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BNA | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS71730DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BNA | Samples |
| TPS71730DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BNA | Samples |
| TPS71730DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BNA | Samples |
| TPS71733DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BNB | Samples |
| TPS71733DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BNB | Samples |
| TPS71733DCKT | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BNB | Samples |
| TPS71733DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BNB | Samples |
| TPS71733DRVR | ACTIVE | WSON | DRV | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BNB | Samples |
| TPS71733DRVRG4 | ACTIVE | WSON | DRV | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BNB | Samples |
| TPS71733DRVT | ACTIVE | WSON | DRV | 6 | 250 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | BNB | Samples |
| TPS71733DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | FV | Samples |
| TPS71733DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | FV | Samples |
| TPS71745DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GL | Samples |
| TPS71745DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GL | Samples |
| TPS71750DSER | ACTIVE | WSON | DSE | 6 | 3000 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | PD | Samples |
| TPS71750DSET | ACTIVE | WSON | DSE | 6 | 250 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | PD | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

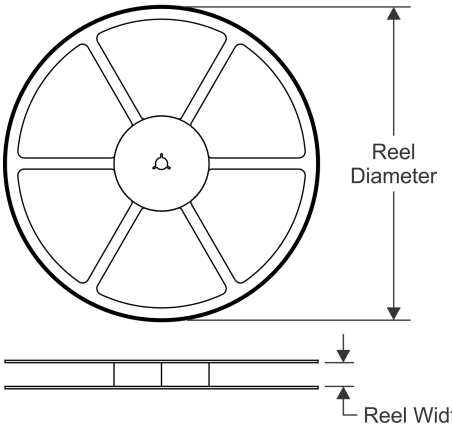
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

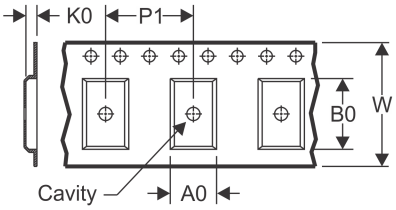
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

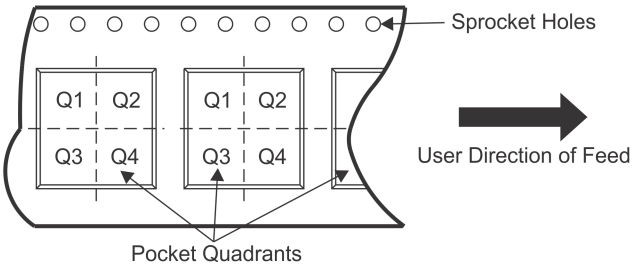



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



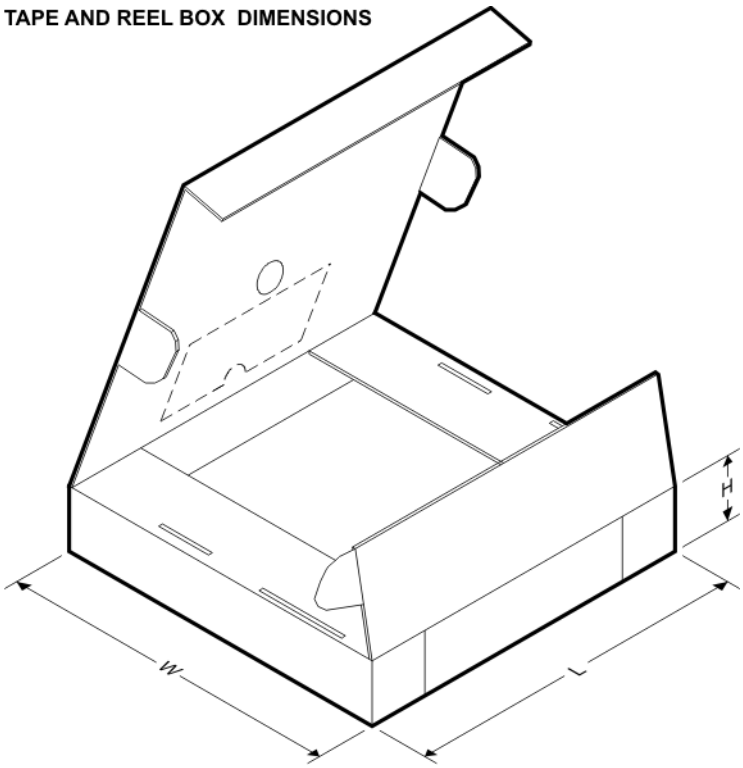

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS71701DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71701DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71701DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71709DSER | WSON | DSE | 6 | 3000 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS71709DSET | WSON | DSE | 6 | 250 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS71710DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71710DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71710DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71710DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71710DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71710DRVT | WSON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71711DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71711DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71711DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71711DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71712DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71712DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71712DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS71712DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71713DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71713DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71713DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71713DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71715DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71715DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71715DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71715DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS717185DSER | WSON | DSE | 6 | 3000 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS717185DSET | WSON | DSE | 6 | 250 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS71718DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71718DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71718DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71718DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71718DSER | WSON | DSE | 6 | 3000 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS71718DSET | WSON | DSE | 6 | 250 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS71719DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71719DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71719DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71719DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71721DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71721DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71721DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71721DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71725DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71725DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71725DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71725DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71726DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71726DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71726DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71726DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71727DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71727DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71727DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71727DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71727DSER | WSON | DSE | 6 | 3000 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS71727DSET | WSON | DSE | 6 | 250 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS717285DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS717285DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS717285DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS717285DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS71728DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71728DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71728DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71728DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71728DSER | WSON | DSE | 6 | 3000 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS71728DSET | WSON | DSE | 6 | 250 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS71729DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71729DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71729DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71729DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71730DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71730DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71730DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71730DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71733DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71733DCKR | SC70 | DCK | 5 | 3000 | 179.0 | 8.4 | 2.2 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71733DCKT | SC70 | DCK | 5 | 250 | 179.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| TPS71733DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPS71733DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71733DRVT | WSON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS71733DSER | WSON | DSE | 6 | 3000 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS71733DSET | WSON | DSE | 6 | 250 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS71745DSER | WSON | DSE | 6 | 3000 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS71745DSET | WSON | DSE | 6 | 250 | 180.0 | 8.4 | 1.75 | 1.75 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS71750DSER | WSON | DSE | 6 | 3000 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS71750DSET | WSON | DSE | 6 | 250 | 179.0 | 8.4 | 1.8 | 1.8 | 1.0 | 4.0 | 8.0 | Q2 |

**TAPE AND REEL BOX DIMENSIONS**



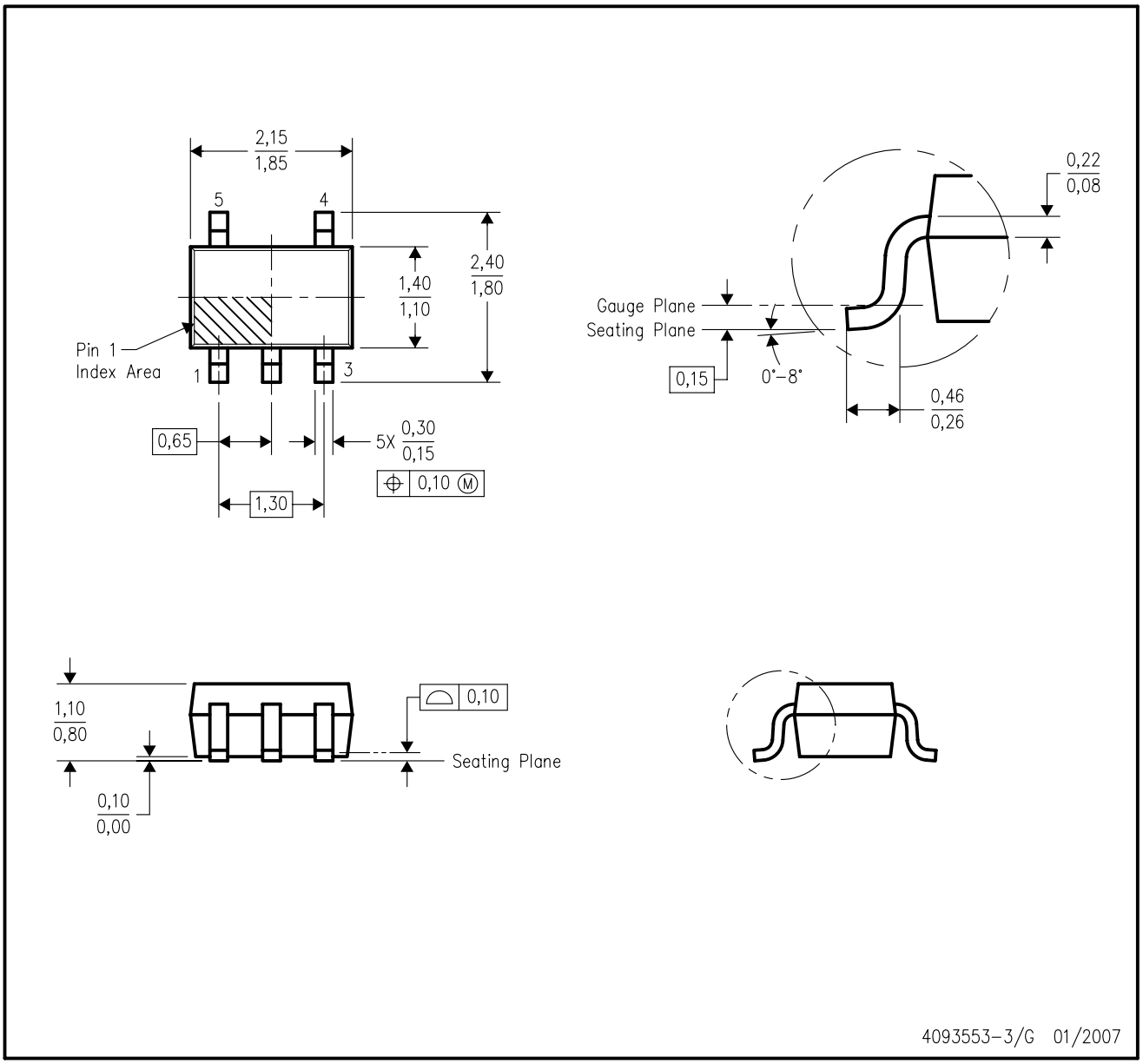

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS71701DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71701DCKR | SC70 | DCK | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71701DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS71709DSER | WSON | DSE | 6 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71709DSET | WSON | DSE | 6 | 250 | 200.0 | 183.0 | 25.0 |
| TPS71710DCKR | SC70 | DCK | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71710DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71710DCKT | SC70 | DCK | 5 | 250 | 340.0 | 340.0 | 38.0 |
| TPS71710DCKT | SC70 | DCK | 5 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71710DRVR | WSON | DRV | 6 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71710DRVT | WSON | DRV | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71711DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71711DCKR | SC70 | DCK | 5 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71711DCKT | SC70 | DCK | 5 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71711DCKT | SC70 | DCK | 5 | 250 | 340.0 | 340.0 | 38.0 |
| TPS71712DCKR | SC70 | DCK | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71712DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71712DCKT | SC70 | DCK | 5 | 250 | 200.0 | 183.0 | 25.0 |
| TPS71712DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS71713DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS71713DCKR | SC70 | DCK | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71713DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS71713DCKT | SC70 | DCK | 5 | 250 | 200.0 | 183.0 | 25.0 |
| TPS71715DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71715DCKR | SC70 | DCK | 5 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71715DCKT | SC70 | DCK | 5 | 250 | 200.0 | 183.0 | 25.0 |
| TPS71715DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS717185DSER | WSON | DSE | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS717185DSET | WSON | DSE | 6 | 250 | 200.0 | 183.0 | 25.0 |
| TPS71718DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71718DCKR | SC70 | DCK | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71718DCKT | SC70 | DCK | 5 | 250 | 200.0 | 183.0 | 25.0 |
| TPS71718DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS71718DSER | WSON | DSE | 6 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71718DSET | WSON | DSE | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71719DCKR | SC70 | DCK | 5 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71719DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71719DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS71719DCKT | SC70 | DCK | 5 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71721DCKR | SC70 | DCK | 5 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71721DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71721DCKT | SC70 | DCK | 5 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71721DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS71725DCKR | SC70 | DCK | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71725DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71725DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS71725DCKT | SC70 | DCK | 5 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71726DCKR | SC70 | DCK | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71726DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71726DCKT | SC70 | DCK | 5 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71726DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS71727DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71727DCKR | SC70 | DCK | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71727DCKT | SC70 | DCK | 5 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71727DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS71727DSER | WSON | DSE | 6 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71727DSET | WSON | DSE | 6 | 250 | 200.0 | 183.0 | 25.0 |
| TPS717285DCKR | SC70 | DCK | 5 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS717285DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS717285DCKT | SC70 | DCK | 5 | 250 | 203.0 | 203.0 | 35.0 |
| TPS717285DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS71728DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71728DCKR | SC70 | DCK | 5 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS71728DCKT | SC70 | DCK | 5 | 250 | 203.0 | 203.0 | 35.0 |

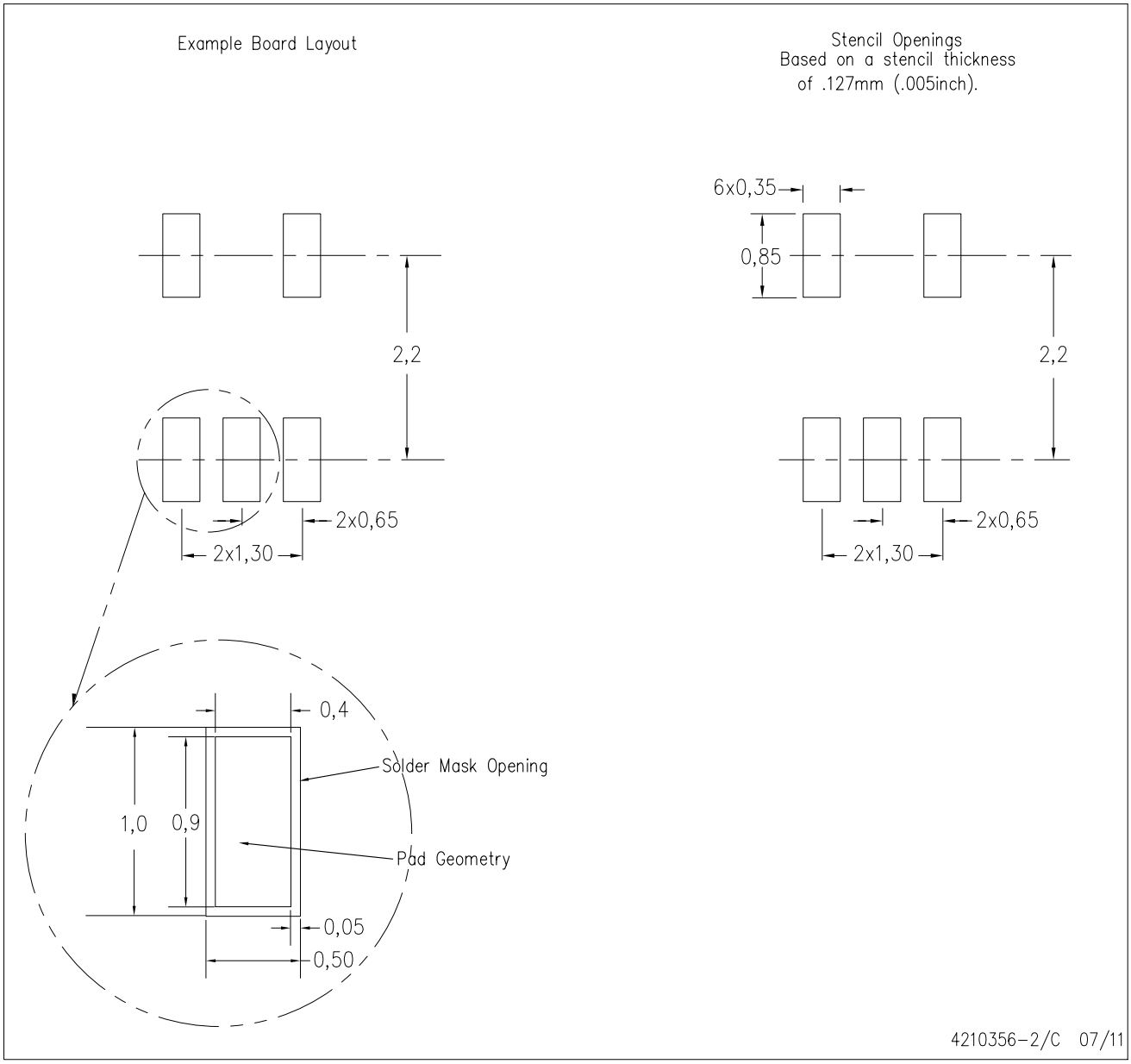
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS71728DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS71728DSER | WSON | DSE | 6 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71728DSET | WSON | DSE | 6 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71729DCKR | SC70 | DCK | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71729DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71729DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS71729DCKT | SC70 | DCK | 5 | 250 | 200.0 | 183.0 | 25.0 |
| TPS71730DCKR | SC70 | DCK | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71730DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71730DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS71730DCKT | SC70 | DCK | 5 | 250 | 200.0 | 183.0 | 25.0 |
| TPS71733DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS71733DCKR | SC70 | DCK | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71733DCKT | SC70 | DCK | 5 | 250 | 203.0 | 203.0 | 35.0 |
| TPS71733DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS71733DRVR | WSON | DRV | 6 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71733DRVT | WSON | DRV | 6 | 250 | 200.0 | 183.0 | 25.0 |
| TPS71733DSER | WSON | DSE | 6 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71733DSET | WSON | DSE | 6 | 250 | 200.0 | 183.0 | 25.0 |
| TPS71745DSER | WSON | DSE | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS71745DSET | WSON | DSE | 6 | 250 | 182.0 | 182.0 | 20.0 |
| TPS71750DSER | WSON | DSE | 6 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS71750DSET | WSON | DSE | 6 | 250 | 200.0 | 183.0 | 25.0 |

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

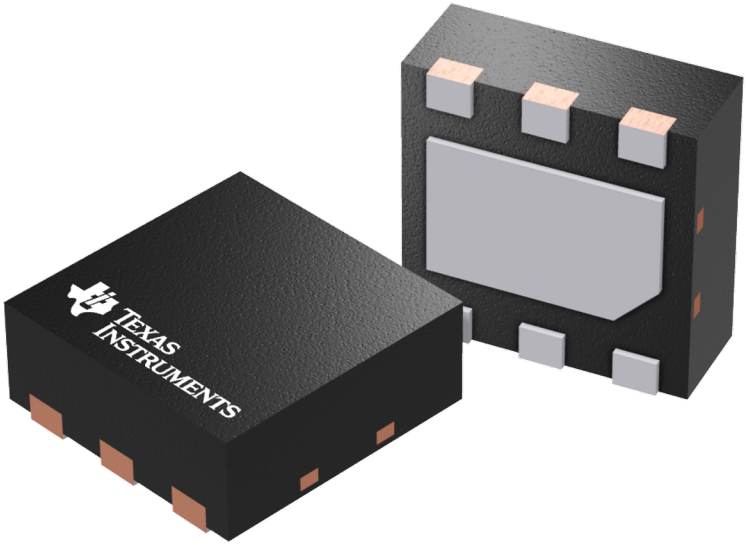
DCK (R-PDSO-G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

# DRV 6 WSON - 0.8 mm max height

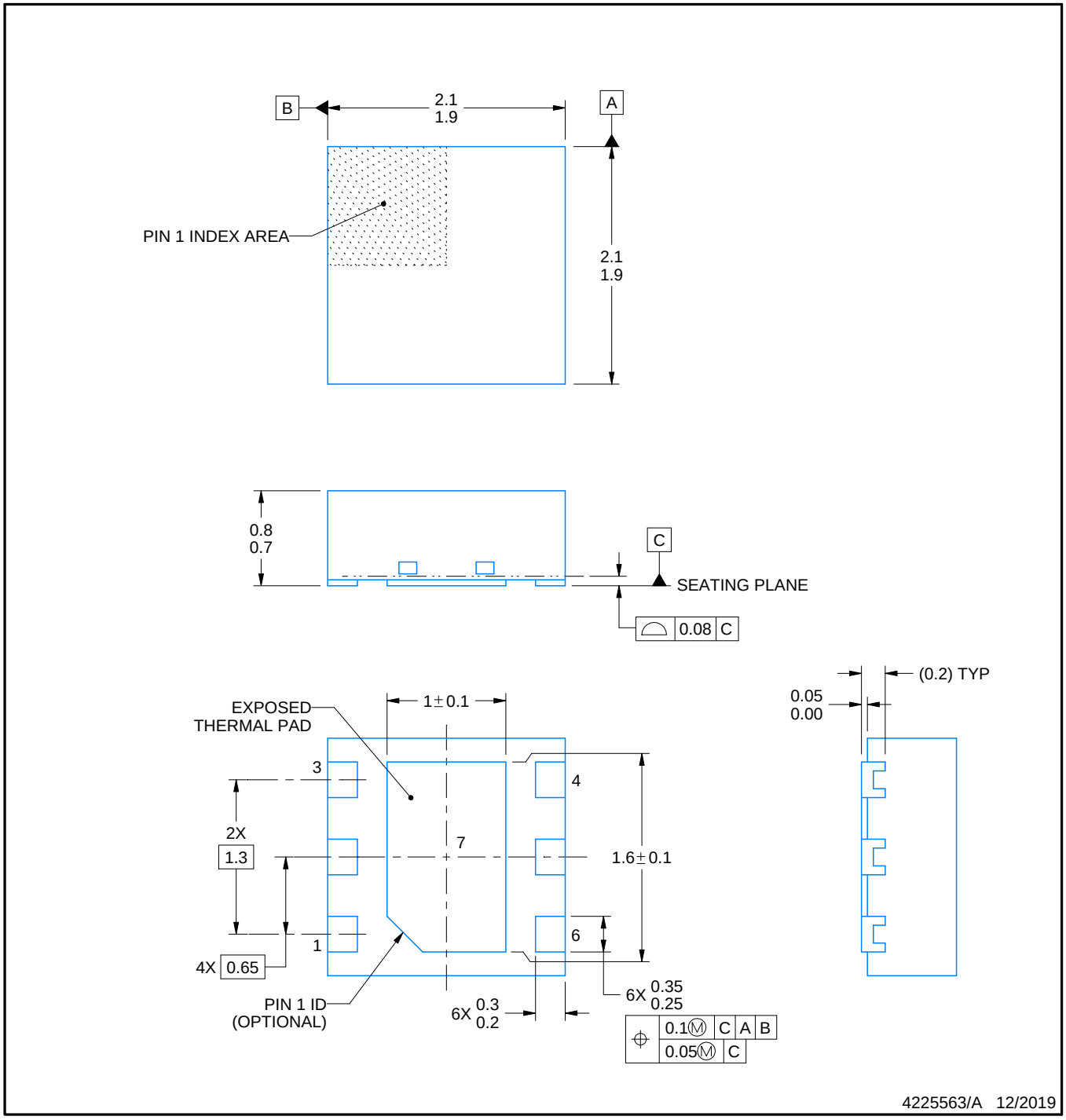
PLASTIC SMALL OUTLINE - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

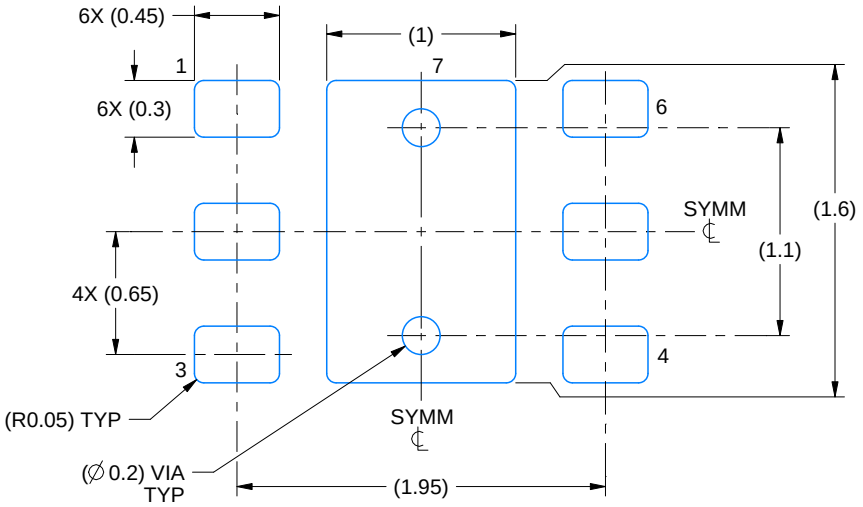


TEXAS INSTRUMENTS

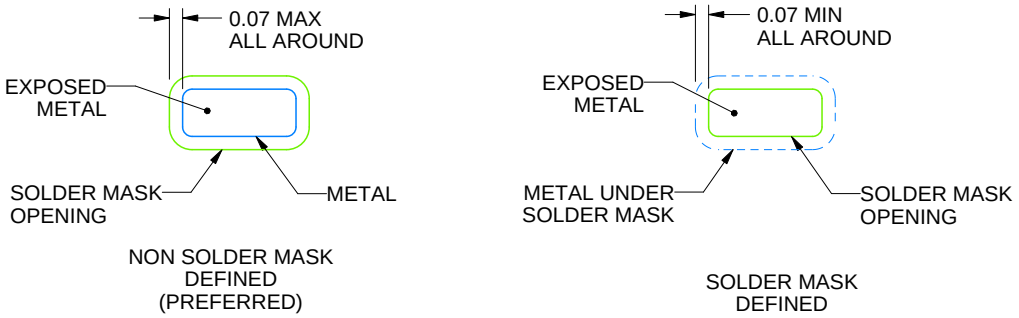



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

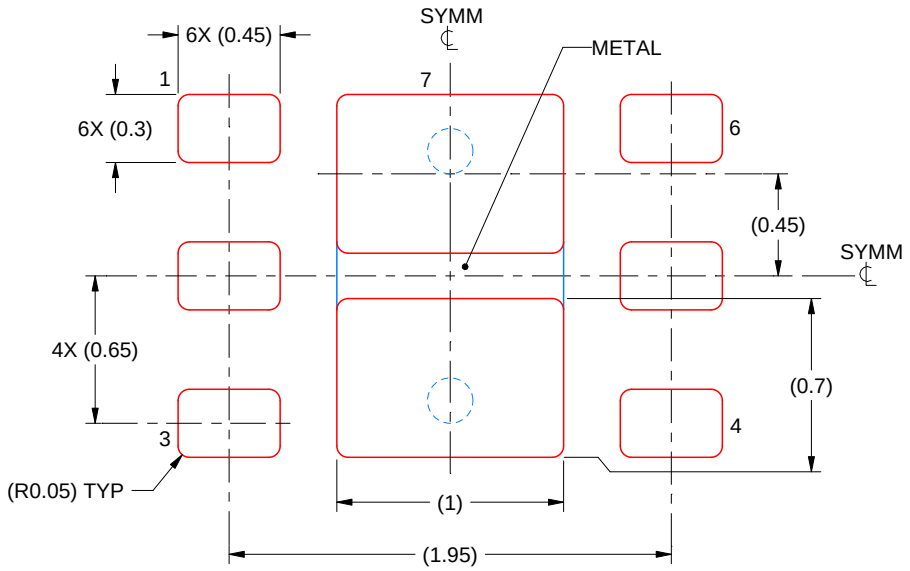



SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

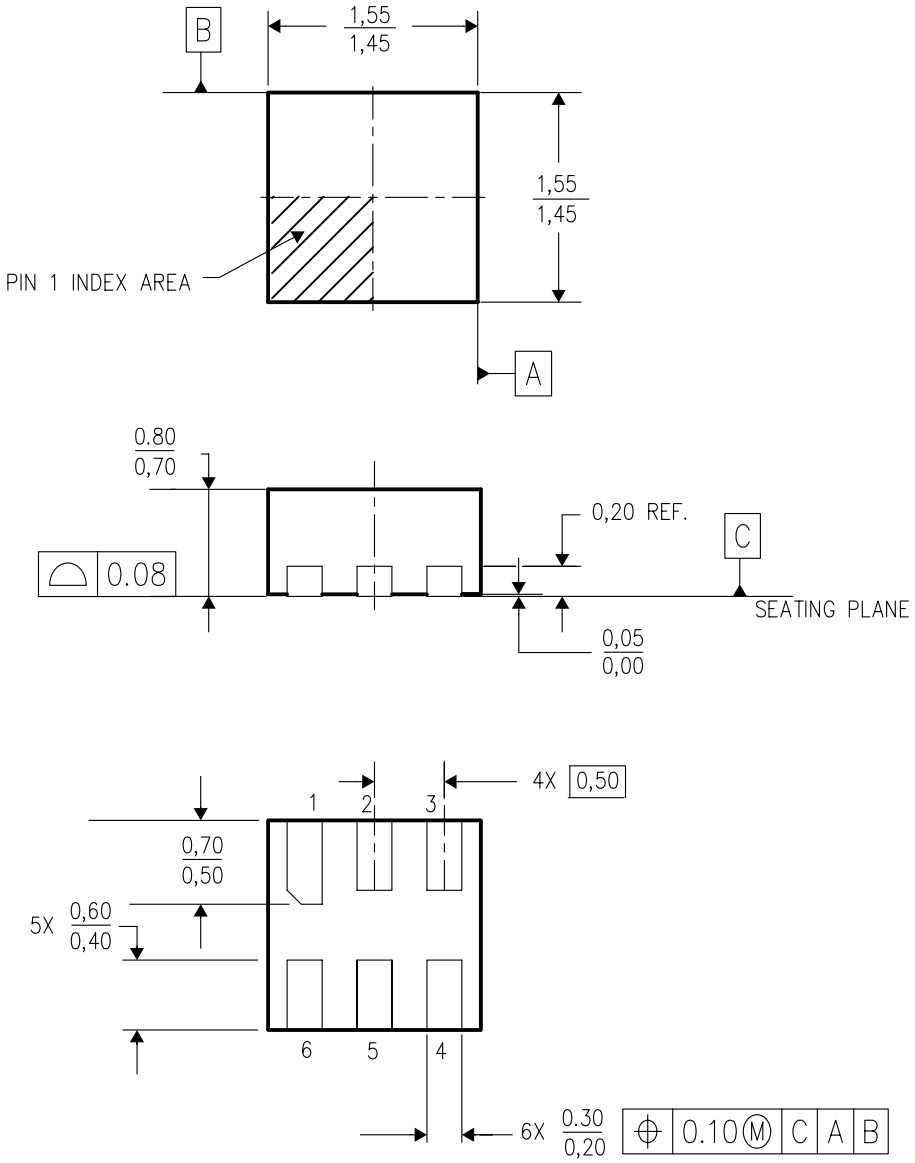
EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

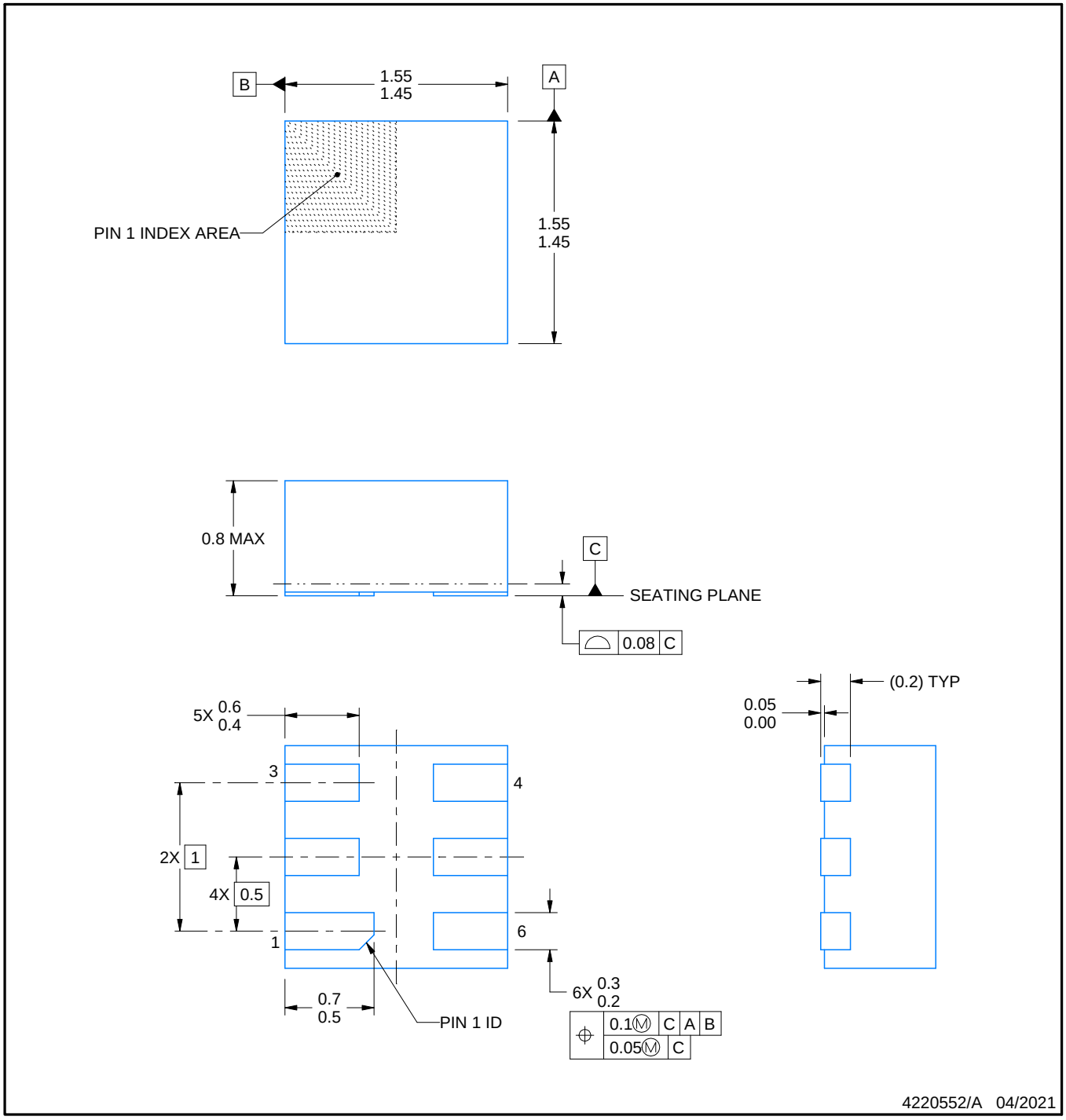
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE



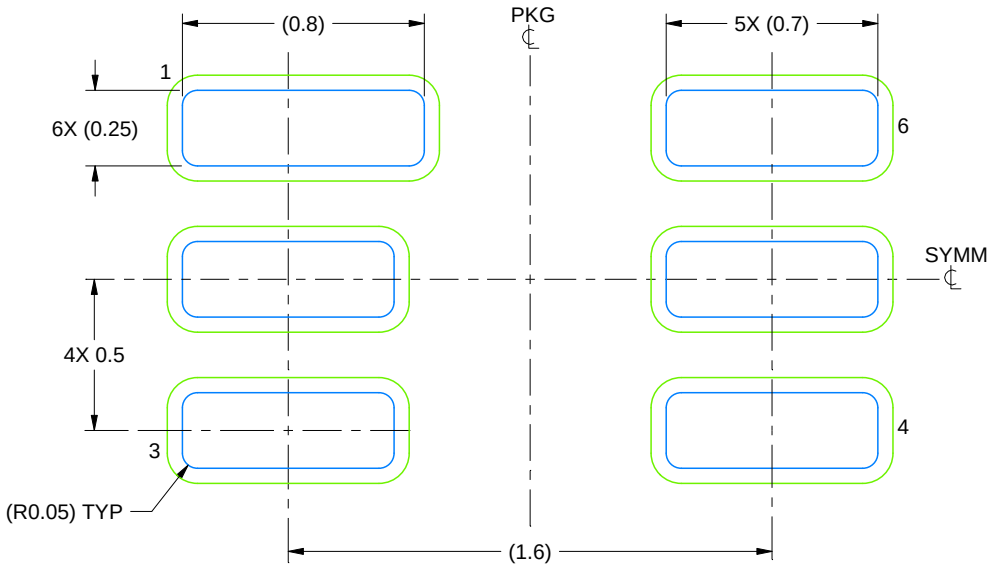

4207810/A 03/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. This package is lead–free.

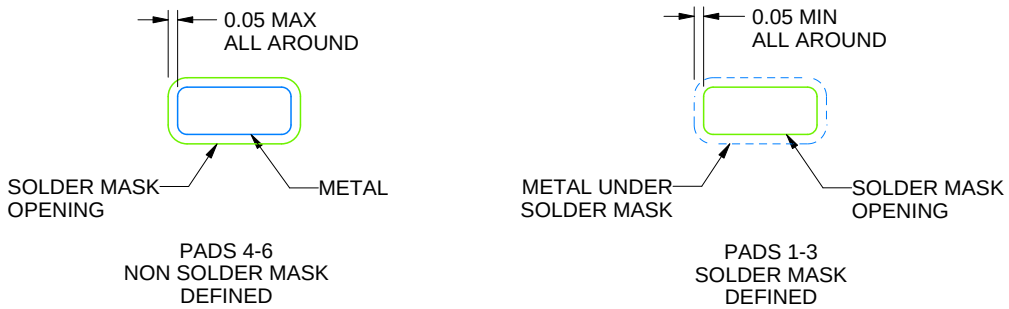



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:40X

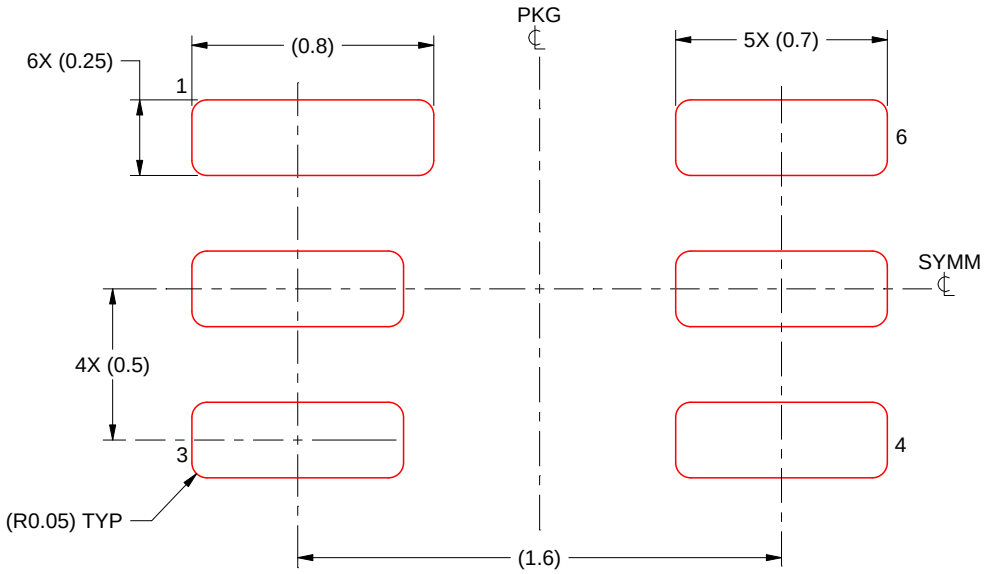



SOLDER MASK DETAILS

4220552/A 04/2021

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# 重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com.cn/zh-cn/legal/termsofsale.html) 或 ti.com.cn 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2021 德州仪器半导体技术（上海）有限公司