

TPS7201Q, TPS7225Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

SLVS102G – MARCH 1995 – REVISED JUNE 2000

- Available in 5-V, 4.85-V, 3.3-V, 3.0-V, and 2.5-V Fixed-Output and Adjustable Versions
- Dropout Voltage <85 mV Max at $I_O = 100$ mA (TPS7250)
- Low Quiescent Current, Independent of Load, 180 μ A Typ
- 8-Pin SOIC and 8-Pin TSSOP Package
- Output Regulated to $\pm 2\%$ Over Full Operating Range for Fixed-Output Versions
- Extremely Low Sleep-State Current, 0.5 μ A Max
- Power-Good (PG) Status Output

description

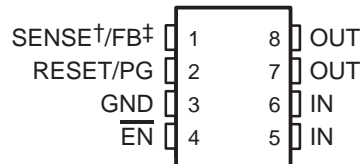
The TPS72xx family of low-dropout (LDO) voltage regulators offers the benefits of low-dropout voltage, micropower operation, and miniaturized packaging. These regulators feature extremely low dropout voltages and quiescent currents compared to conventional LDO regulators. Offered in small-outline integrated-circuit (SOIC) packages and 8-terminal thin shrink small-outline (TSSOP), the TPS72xx series devices are ideal for cost-sensitive designs and for designs where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual pnp pass transistor to be replaced by a PMOS device. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low – maximum of 85 mV at 100 mA of load current (TPS7250) – and is directly proportional to the load current (see Figure 1). Since the PMOS pass element is a voltage-driven device, the quiescent current is very low (300 μ A maximum) and is stable over the entire range of output load current (0 mA to 250 mA). Intended for use in portable systems such as laptops and cellular phones, the low-dropout voltage and micropower operation result in a significant increase in system battery operating life.

The TPS72xx also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 0.5 μ A maximum at $T_J = 25^\circ\text{C}$. Other features include a power-good function that reports low output voltage and may be used to implement a power-on reset or a low-battery indicator.

The TPS72xx is offered in 2.5-V, 3-V, 3.3-V, 4.85-V, and 5-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.2 V to 9.75 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges (3% for adjustable version).

D, P, OR PW PACKAGE
(TOP VIEW)



† SENSE – Fixed voltage options only (TPS7225, TPS7230, TPS7233, TPS7248, and TPS7250)

‡ FB – Adjustable version only (TPS7201)

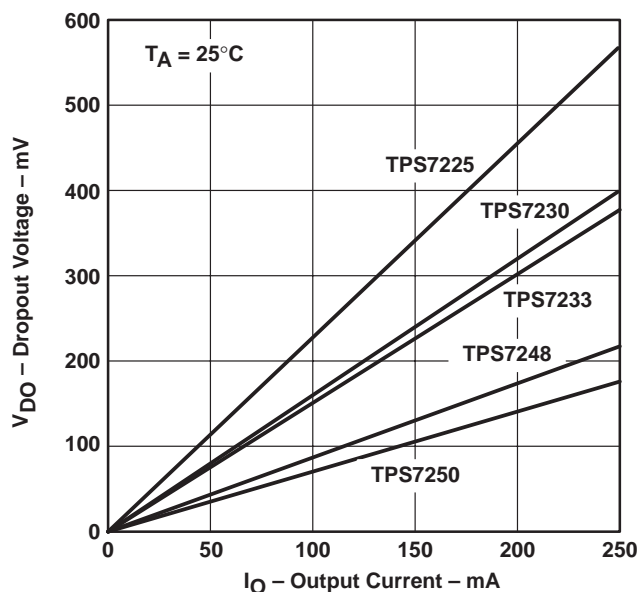


Figure 1. Typical Dropout Voltage Versus Output Current



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000, Texas Instruments Incorporated

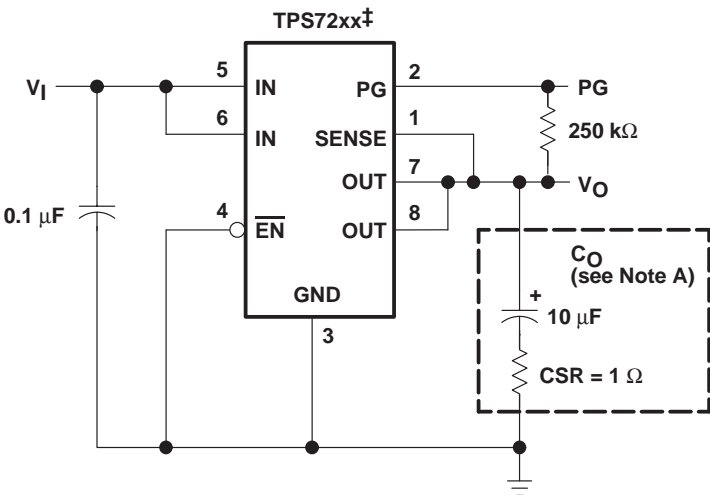
TPS7201Q, TPS7225Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

SLVS102G – MARCH 1995 – REVISED JUNE 2000

AVAILABLE OPTIONS

| T _J | OUTPUT VOLTAGE (V) | | | PACKAGED DEVICES | | | CHIP FORM (Y) |
|----------------|-------------------------------|------|------|-------------------|-----------|-------------|---------------|
| | MIN | TYP | MAX | SMALL OUTLINE (D) | PDIP (P) | TSSOP (PW) | |
| –55°C to 150°C | 4.9 | 5 | 5.1 | TPS7250QD | TPS7250QP | TPS7250QPWR | TPS7250Y |
| | 4.75 | 4.85 | 4.95 | TPS7248QD | TPS7248QP | TPS7248QPWR | TPS7248Y |
| | 3.23 | 3.3 | 3.37 | TPS7233QD | TPS7233QP | TPS7233QPWR | TPS7233Y |
| | 2.94 | 3 | 3.06 | TPS7230QD | TPS7230QP | TPS7230QPWR | TPS7230Y |
| | 2.45 | 2.5 | 2.55 | TPS7225QD | TPS7225QP | TPS7225QPWR | TPS7225Y |
| | Adjustable 1.2 V to 9.75 V | | | TPS7201QD | TPS7201QP | TPS7201QPWR | TPS7201Y |

The D package is available taped and reeled. Add R suffix to device type (e.g., TPS7250QDR). The PW package is only available left-end taped and reeled. The TPS7201Q is programmable using an external resistor divider (see application information). The chip form is tested at 25°C.



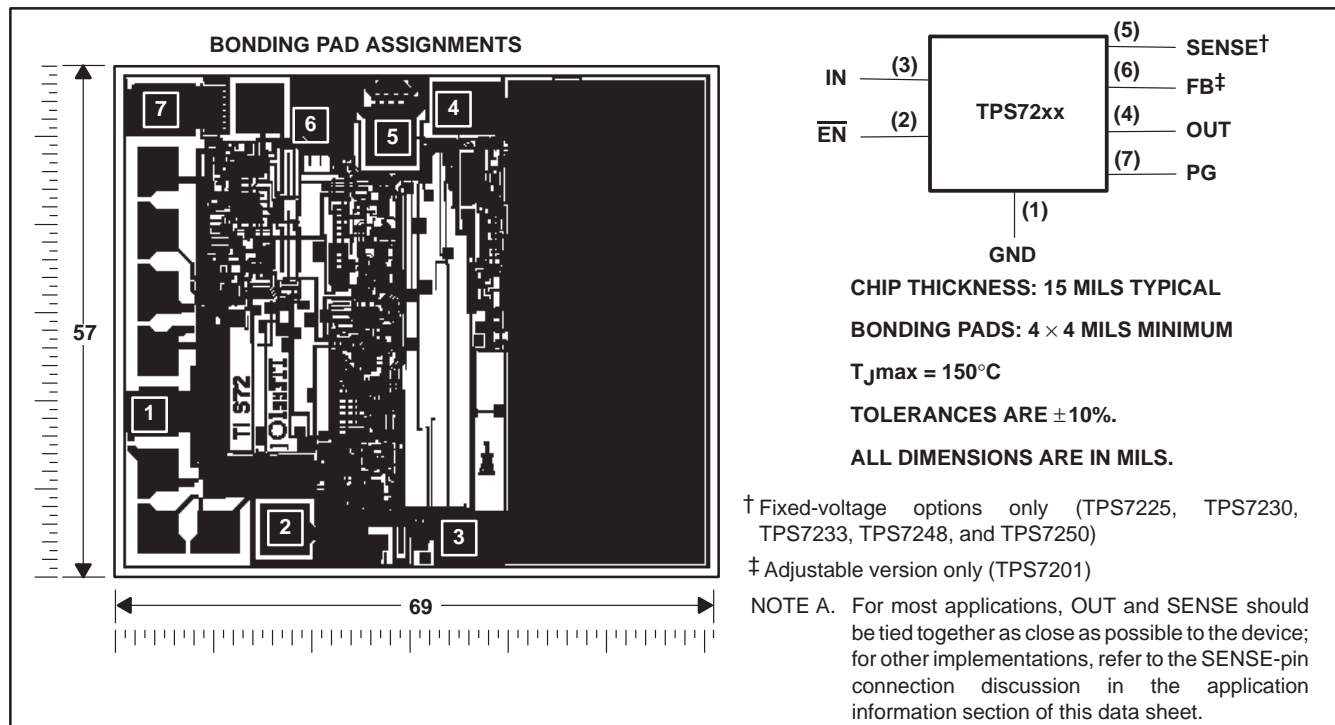
‡ TPS7225Q, TPS7230Q, TPS7233Q, TPS7248Q, TPS7250Q (fixed-voltage options)
NOTE A: Capacitor selection is nontrivial. See application information section for details.

Figure 2. Typical Application Configuration

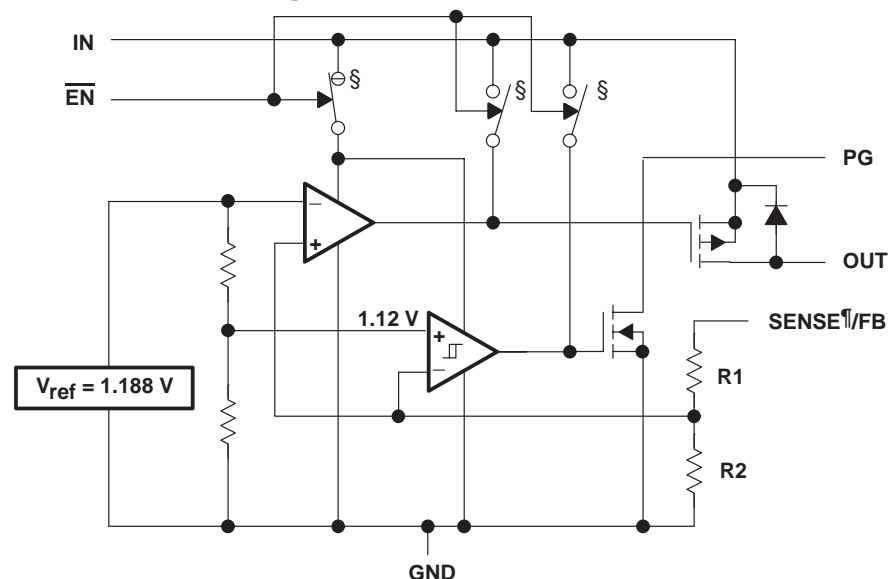
TPS7201Q, TPS7225Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS
SLVS102G – MARCH 1995 – REVISED JUNE 2000

TPS72xx chip information

These chips, when properly assembled, display characteristics similar to the TPS72xxQ. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.



functional block diagram



RESISTOR DIVIDER OPTIONS

| DEVICE | R1 | R2 | UNIT |
|---------|-----|-----|------|
| TPS7201 | 0 | ∞ | Ω |
| TPS7225 | 257 | 233 | kΩ |
| TPS7230 | 357 | 233 | kΩ |
| TPS7233 | 420 | 233 | kΩ |
| TPS7248 | 726 | 233 | kΩ |
| TPS7250 | 756 | 233 | kΩ |

NOTE A: Resistors are nominal values only.

COMPONENT COUNT

| | |
|---------------------|-----|
| MOS transistors | 108 |
| Bipolar transistors | 41 |
| Diodes | 4 |
| Capacitors | 15 |
| Resistors | 75 |

§ Switch positions are shown with EN low (active).

¶ For most applications, SENSE should be externally connected to OUT as close as possible to the device. For other implementations, refer to the SENSE-pin connection discussion in application information section.

**TPS7201Q, TPS7225Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS**

SLVS102G – MARCH 1995 – REVISED JUNE 2000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|---------------------------------------|
| Input voltage range [‡] , V_I , PG, SENSE, \overline{EN} | –0.3 V to 11 V |
| Output current, I_O | 1.5 A |
| Continuous total power dissipation | See Dissipation Rating Tables 1 and 2 |
| Operating virtual junction temperature range, T_J | –55°C to 150°C |
| Storage temperature range, T_{stg} | –65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (see Note 1 and Figure 3)

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 85^\circ\text{C}$ POWER RATING | $T_A = 125^\circ\text{C}$ POWER RATING |
|---------|---|---|--|--|---|
| D | 725 mW | 5.8 mW/°C | 464 mW | 377 mW | 145 mW |
| P | 1175 mW | 8.74 mW/°C | 782 mW | 650 mW | 301 mW |
| PW | 525 mW | 4.2 mW/°C | 336 mW | 273 mW | 105 mW |

DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (see Note 1 and Figure 4)

| PACKAGE | $T_C \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_C = 25^\circ\text{C}$ | $T_C = 70^\circ\text{C}$ POWER RATING | $T_C = 85^\circ\text{C}$ POWER RATING | $T_C = 125^\circ\text{C}$ POWER RATING |
|---------|---|---|--|--|---|
| D | 2063 mW | 16.5 mW/°C | 1320 mW | 1073 mW | 413 mW |
| P | 2738 mW | 20.49 mW/°C | 1816 mW | 1508 mW | 689 mW |
| PW | 2900 mW | 23.2 mW/°C | 1856 mW | 1508 mW | 580 mW |

NOTE 1: Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum of 150°C. For guidelines on maintaining junction temperature within the recommended operating range, see application information section.

**MAXIMUM CONTINUOUS DISSIPATION
vs
FREE-AIR TEMPERATURE**

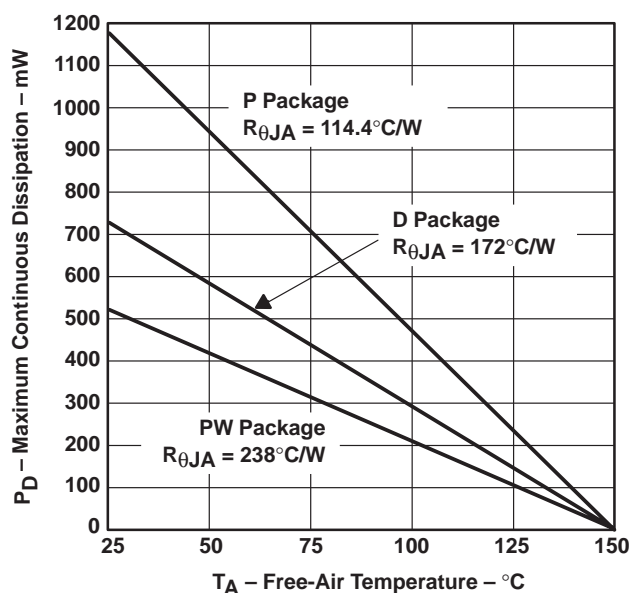


Figure 3

**MAXIMUM CONTINUOUS DISSIPATION
vs
CASE TEMPERATURE**

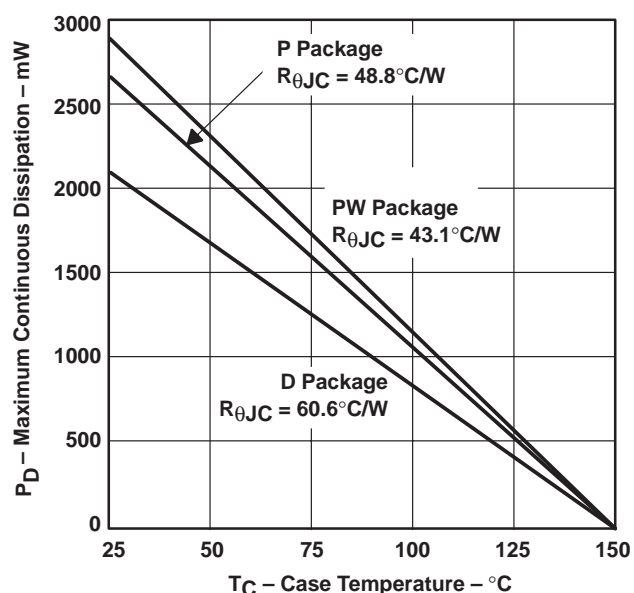


Figure 4

TPS7201Q, TPS7225Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS
SLVS102G – MARCH 1995 – REVISED JUNE 2000

recommended operating conditions

| | | MIN | MAX | UNIT |
|--|----------|------|-----|------|
| Input voltage, V_I^\dagger | TPS7201Q | 3 | 10 | V |
| | TPS7225Q | 3.65 | 10 | |
| | TPS7230Q | 3.96 | 10 | |
| | TPS7233Q | 3.98 | 10 | |
| | TPS7248Q | 5.24 | 10 | |
| | TPS7250Q | 5.41 | 10 | |
| High-level input voltage at \overline{EN} , V_{IH} | | 2 | | V |
| Low-level input voltage at \overline{EN} , V_{IL} | | | 0.5 | V |
| Output current, I_O | | 0 | 250 | mA |
| Operating virtual junction temperature, T_J | | -40 | 125 | °C |

[†] Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage at the maximum specified load range. Since dropout voltage is a function of output current, *the usable range can be extended for lighter loads*. To calculate the minimum input voltage for the maximum load current used in a given application, use the following equation:

$$V_{I(\min)} = V_{O(\max)} + V_{DO(\max \text{ load})}$$

Because the TPS7201 is programmable, $r_{DS(on)}$ should be used to calculate V_{DO} before applying the above equation. The equation for calculating V_{DO} from $r_{DS(on)}$ is given in Note 3 under the TPS7201 electrical characteristics table. The minimum value of 3 V is the absolute lower limit for the recommended input-voltage range for the TPS7201.

TPS7201Q, TPS7225Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

SLVS102G – MARCH 1995 – REVISED JUNE 2000

electrical characteristics, $I_O = 10 \text{ mA}$, $\overline{\text{EN}} = 0 \text{ V}$, $C_O = 4.7 \mu\text{F}$ ($\text{CSR}^\dagger = 1 \Omega$), SENSE/FB shorted to OUT (unless otherwise noted)

| PARAMETER | TEST CONDITIONS [‡] | T _J | TPS72xxQ | | | UNIT |
|--|---|----------------|----------|-----|-----|---------------|
| | | | MIN | TYP | MAX | |
| Ground current (active mode) | $\text{EN} \leq 0.5 \text{ V}$, $0 \text{ mA} \leq I_O \leq 250 \text{ mA}$ | 25°C | | 180 | 225 | μA |
| | | –40°C to 125°C | | | 325 | |
| Input current (standby mode) | $\overline{\text{EN}} = V_I$, $3 \text{ V} \leq V_I \leq 10 \text{ V}$ | 25°C | | | 0.5 | μA |
| | | –40°C to 125°C | | | 1 | |
| Output current limit threshold | $V_O = 0 \text{ V}$ $V_I = 10 \text{ V}$ | 25°C | | 0.6 | 1 | A |
| | | –40°C to 125°C | | | 1.5 | |
| Pass-element leakage current in standby mode | $\text{EN} = V_I$, $3 \text{ V} \leq V_I \leq 10 \text{ V}$ | 25°C | | | 0.5 | μA |
| | | –40°C to 125°C | | | 1 | |
| PG leakage current | $V_{\text{PG}} = 10 \text{ V}$, Normal operation | 25°C | | | 0.5 | μA |
| | | –40°C to 125°C | | | 0.5 | |
| Output voltage temperature coefficient | | –40°C to 125°C | | 31 | 75 | ppm/°C |
| Thermal shutdown junction temperature | | | | 165 | | °C |
| $\overline{\text{EN}}$ logic high (standby mode) | $3 \text{ V} \leq V_I \leq 6 \text{ V}$ | –40°C to 125°C | | 2 | | V |
| | $6 \text{ V} \leq V_I \leq 10 \text{ V}$ | | | 2.7 | | |
| $\overline{\text{EN}}$ logic low (active mode) | $3 \text{ V} \leq V_I \leq 10 \text{ V}$ | 25°C | | | 0.5 | V |
| | | –40°C to 125°C | | | 0.5 | |
| $\overline{\text{EN}}$ hysteresis voltage | | 25°C | | 50 | | mV |
| $\overline{\text{EN}}$ input current | $0 \text{ V} \leq V_I \leq 10 \text{ V}$ | 25°C | –0.5 | | 0.5 | μA |
| | | –40°C to 125°C | –0.5 | | 0.5 | |
| Minimum V_I for active pass element | | 25°C | | 1.9 | 2.5 | V |
| | | –40°C to 125°C | | | 2.5 | |
| Minimum V_I for valid PG | $I_{\text{PG}} = 300 \mu\text{A}$ | 25°C | | 1.1 | 1.5 | V |
| | | –40°C to 125°C | | | 1.9 | |

[†] CSR(compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

[‡] Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7201Q, TPS7225Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS
SLVS102G – MARCH 1995 – REVISED JUNE 2000

TPS7201Q electrical characteristics, $I_O = 10$ mA, $V_I = 3.5$ V, $\overline{EN} = 0$ V, $C_O = 4.7$ μ F (CSR $^\dagger = 1$ Ω), FB shorted to OUT at device leads (unless otherwise noted)

| PARAMETER | TEST CONDITIONS‡ | | T _J | TPS7201Q | | | UNIT | |
|---|---|-------------------------------------|----------------|-----------------------------|-----|-------|--------|-----|
| | | | | MIN | TYP | MAX | | |
| Reference voltage (measured at FB with OUT connected to FB) | V _I = 3.5 V, I _O = 10 mA | | 25°C | 1.188 | | | V | |
| | 3 V ≤ V _I ≤ 10 V, See Note 2 | 5 mA ≤ I _O ≤ 250 mA, | –40°C to 125°C | 1.152 | | 1.224 | V | |
| Reference voltage temperature coefficient | | | –40°C to 125°C | | 31 | 75 | ppm/°C | |
| Pass-element series resistance (see Note 3) | V _I = 2.4 V,§ | 50 μA ≤ I _O ≤ 100 mA | 25°C | 2.1 | | | Ω | |
| | V _I = 2.4 V,§ | 100 mA ≤ I _O ≤ 200 mA | 25°C | 2.9 | | | | |
| | V _I = 2.9 V, | 50 μA ≤ I _O ≤ 250 mA | 25°C | 1.6 | | | | 2.7 |
| | | | –40°C to 125°C | 4.5 | | | | |
| | V _I = 3.9 V, | 50 μA ≤ I _O ≤ 250 mA | 25°C | 1 | | | | |
| | V _I = 5.9 V, | 50 μA ≤ I _O ≤ 250 mA | 25°C | 0.8 | | | | |
| Input regulation | V _I = 3 V to 10 V, See Note 2 | 50 μA ≤ I _O ≤ 250 mA, | 25°C | | | 23 | mV | |
| | | | –40°C to 125°C | | | 36 | | |
| Output regulation | I _O = 5 mA to 250 mA, See Note 2 | 3 V ≤ V _I ≤ 10 V, | 25°C | | 15 | 25 | mV | |
| | | | –40°C to 125°C | | 36 | | | |
| | I _O = 50 μA to 250 mA, See Note 2 | 3 V ≤ V _I ≤ 10 V, | 25°C | | 17 | 27 | | |
| | | | –40°C to 125°C | | 43 | | | |
| Ripple rejection | f = 120 Hz | I _O = 50 μA | 25°C | 49 | 60 | dB | | |
| | | | –40°C to 125°C | 32 | | | | |
| | | I _O = 250 mA, See Note 2 | 25°C | 45 | 50 | | | |
| | | | –40°C to 125°C | 30 | | | | |
| Output noise spectral density | f = 120 Hz | | 25°C | 2 | | | μV/√Hz | |
| Output noise voltage | 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω | C _O = 4.7 μF | 25°C | 235 | | | μVrms | |
| | | C _O = 10 μF | 25°C | 190 | | | | |
| | | C _O = 100 μF | 25°C | 125 | | | | |
| PG trip-threshold voltage¶ | V _{FB} voltage decreasing from above V _{PG} | | –40°C to 125°C | 0.95 × V _{FB(nom)} | | | V | |
| PG hysteresis voltage¶ | Measured at V _{FB} | | 25°C | 12 | | | mV | |
| PG output low voltage¶ | I _{PG} = 400 μA, V _I = 2.13 V | | 25°C | 0.1 | 0.4 | V | | |
| | | | –40°C to 125°C | 0.4 | | | | |
| FB input current | | | 25°C | –10 | 0.1 | 10 | nA | |
| | | | –40°C to 125°C | –20 | 20 | | | |

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ This voltage is not recommended.

¶ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 2. When $V_I < 2.9$ V and $I_O > 100$ mA simultaneously, pass element $r_{DS(\text{on})}$ increases (see Figure 10) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

3. To calculate dropout voltage, use equation:

$$V_{DO} = I_O \cdot r_{DS(\text{on})}$$

$r_{DS(\text{on})}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(\text{on})}$ for $V_I = 2.4$ V, 2.9 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 2.5 V, 3 V, 4 V, and 6 V, respectively. For other programmed values, refer to Figures 10 and 11.

TPS7201Q, TPS7225Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

SLVS102G – MARCH 1995 – REVISED JUNE 2000

TPS7225Q electrical characteristics, $I_O = 10\text{ mA}$, $V_I = 3.5\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($CSR^\dagger = 1\text{ }\Omega$), SENSE shorted to OUT (unless otherwise noted)

| PARAMETER | TEST CONDITIONS‡ | | T _J | TPS7225Q | | | UNIT |
|--------------------------------|--|--------------------------------|----------------|----------|---------------------------------|------|--------------------------------|
| | | | | MIN | TYP | MAX | |
| Output voltage | $V_I = 3.5\text{ V}$, $I_O = 10\text{ mA}$ | | 25°C | | 2.5 | | V |
| | $3.5\text{ V} \leq V_I \leq 10\text{ V}$, $5\text{ mA} \leq I_O \leq 250\text{ mA}$ | | –40°C to 125°C | 2.45 | | 2.55 | |
| Dropout voltage | $I_O = 250\text{ mA}$, $V_I = 2.97\text{ V}$ | | 25°C | | 560 | 850 | mV |
| | | | –40°C to 125°C | | | 1.1 | V |
| Pass-element series resistance | $(2.97\text{ V} - V_O)/I_O$, $I_O = 250\text{ mA}$ | $V_I = 2.97\text{ V}$ | 25°C | | 2.24 | 3.4 | Ω |
| | | | –40°C to 125°C | | | 3.84 | |
| Input regulation | $V_I = 3.5\text{ V to }10\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$ | | 25°C | | 9 | 27 | mV |
| | | | –40°C to 125°C | | | 33 | |
| Output regulation | $I_O = 5\text{ mA to }250\text{ mA}$, $3.5\text{ V} \leq V_I \leq 10\text{ V}$ | | 25°C | | 28 | 36 | mV |
| | | | –40°C to 125°C | | | 60 | |
| | $I_O = 50\text{ }\mu\text{A to }250\text{ mA}$, $3.5\text{ V} \leq V_I \leq 10\text{ V}$ | | 25°C | | 24 | 41 | |
| | | | –40°C to 125°C | | | 73 | |
| Ripple rejection | $f = 120\text{ Hz}$ | $I_O = 50\text{ }\mu\text{A}$ | 25°C | 47 | 58 | | dB |
| | | | –40°C to 125°C | 45 | | | |
| | | $I_O = 250\text{ mA}$ | 25°C | 40 | 46 | | |
| | | | –40°C to 125°C | 38 | | | |
| Output noise spectral density | $f = 120\text{ Hz}$ | | 25°C | | 2 | | $\mu\text{V}/\sqrt{\text{Hz}}$ |
| Output noise voltage | $10\text{ Hz} \leq f \leq 100\text{ kHz}$, $CSR^\dagger = 1\text{ }\Omega$ | $C_O = 4.7\text{ }\mu\text{F}$ | 25°C | | 248 | | μV_{rms} |
| | | $C_O = 10\text{ }\mu\text{F}$ | 25°C | | 200 | | |
| | | $C_O = 100\text{ }\mu\text{F}$ | 25°C | | 130 | | |
| PG trip-threshold voltage | V_O voltage decreasing from above V_{PG} | | –40°C to 125°C | | $0.95 \times V_{O(\text{nom})}$ | | V |
| PG hysteresis voltage | | | 25°C | | 50 | | mV |
| PG output low voltage | $I_{\text{PG}} = 1.2\text{ mA}$, $V_I = 2.13\text{ V}$ | | 25°C | | 0.3 | 0.44 | V |
| | | | –40°C to 125°C | | | 0.5 | |

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7201Q, TPS7225Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS
SLVS102G – MARCH 1995 – REVISED JUNE 2000

TPS7230Q electrical characteristics, $I_O = 10\text{ mA}$, $V_I = 4\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($\text{CSR}^\dagger = 1\text{ }\Omega$), SENSE shorted to OUT (unless otherwise noted)

| PARAMETER | TEST CONDITIONS‡ | | T _J | TPS7230Q | | | UNIT |
|--------------------------------|---|--------------------------|----------------|----------------------------|------|------|--------|
| | | | | MIN | TYP | MAX | |
| Output voltage | V _I = 4 V, I _O = 10 mA | | 25°C | 3 | | | V |
| | 4 V ≤ V _I ≤ 10 V, 5 mA ≤ I _O ≤ 250 mA | | −40°C to 125°C | 2.94 | | 3.06 | |
| Dropout voltage | I _O = 100 mA, V _I = 2.97 V | | 25°C | 145 185 | | | mV |
| | | | −40°C to 125°C | 270 | | | |
| | I _O = 250 mA, V _I = 2.97 V | | 25°C | 390 502 | | | |
| | | | −40°C to 125°C | 900 | | | |
| Pass-element series resistance | (2.97 V − V _O)/I _O , I _O = 250 mA | V _I = 2.97 V, | 25°C | 1.56 2.01 | | | Ω |
| | | | −40°C to 125°C | 3.6 | | | |
| Input regulation | V _I = 4 V to 10 V, 50 μA ≤ I _O ≤ 250 mA | | 25°C | 9 27 | | | mV |
| | | | −40°C to 125°C | 33 | | | |
| Output regulation | I _O = 5 mA to 250 mA, 4 V ≤ V _I ≤ 10 V | | 25°C | 34 45 | | | mV |
| | | | −40°C to 125°C | 74 | | | |
| | I _O = 50 μA to 250 mA, 4 V ≤ V _I ≤ 10 V | | 25°C | 42 60 | | | |
| | | | −40°C to 125°C | 98 | | | |
| Ripple rejection | f = 120 Hz | I _O = 50 μA | 25°C | 45 | 56 | dB | |
| | | | −40°C to 125°C | 44 | | | |
| | | I _O = 250 mA | 25°C | 40 | 45 | | |
| | | | −40°C to 125°C | 38 | | | |
| Output noise spectral density | f = 120 Hz | | 25°C | 2 | | | μV/√Hz |
| Output noise voltage | 10 Hz ≤ f ≤ 100 kHz, CSRT = 1 Ω | C _O = 4.7 μF | 25°C | 256 | | | μVrms |
| | | C _O = 10 μF | 25°C | 206 | | | |
| | | C _O = 100 μF | 25°C | 132 | | | |
| PG trip-threshold voltage | V _O voltage decreasing from above V _{PG} | | −40°C to 125°C | 0.95 × V _{O(nom)} | | | V |
| PG hysteresis voltage | | | 25°C | 50 | | | mV |
| PG output low voltage | I _{PG} = 1.2 mA, V _I = 2.55 V | | 25°C | 0.25 | 0.44 | V | |
| | | | −40°C to 125°C | 0.44 | | | |

[†] CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

[‡] Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7201Q, TPS7225Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

SLVS102G – MARCH 1995 – REVISED JUNE 2000

TPS7233Q electrical characteristics, $I_O = 10\text{ mA}$, $V_I = 4.3\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($CSR^\dagger = 1\text{ }\Omega$), SENSE shorted to OUT (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | | T _J | TPS7233Q | | | UNIT |
|--------------------------------|---|--------------------------|----------------|----------------------------|------|-----|--------|
| | | | | MIN | TYP | MAX | |
| Output voltage | V _I = 4.3 V, I _O = 10 mA | | 25°C | 3.3 | | | V |
| | 4.3 V ≤ V _I ≤ 10 V, 5 mA ≤ I _O ≤ 250 mA | | –40°C to 125°C | 3.23 | 3.37 | | |
| Dropout voltage | I _O = 10 mA, V _I = 3.23 V | | 25°C | 14 | 20 | | mV |
| | | | –40°C to 125°C | 30 | | | |
| | I _O = 100 mA, V _I = 3.23 V | | 25°C | 140 | 180 | | |
| | | | –40°C to 125°C | 232 | | | |
| | I _O = 250 mA, V _I = 3.23 V | | 25°C | 360 | 460 | | |
| | | | –40°C to 125°C | 610 | | | |
| Pass-element series resistance | (3.23 V – V _O)/I _O , I _O = 250 mA | V _I = 3.23 V, | 25°C | 1.5 | 1.84 | | Ω |
| | | | –40°C to 125°C | 2.5 | | | |
| Input regulation | V _I = 4.3 V to 10 V, 50 μA ≤ I _O ≤ 250 mA | | 25°C | 8 | 25 | | mV |
| | | | –40°C to 125°C | 33 | | | |
| Output regulation | I _O = 5 mA to 250 mA, 4.3 V ≤ V _I ≤ 10 V | | 25°C | 32 | 42 | | mV |
| | | | –40°C to 125°C | 71 | | | |
| | I _O = 50 μA to 250 mA, 4.3 V ≤ V _I ≤ 10 V | | 25°C | 41 | 55 | | |
| | | | –40°C to 125°C | 98 | | | |
| Ripple rejection | f = 120 Hz | I _O = 50 μA | 25°C | 40 | 52 | | dB |
| | | | | –40°C to 125°C | 38 | | |
| | | I _O = 250 mA | 25°C | 35 | 44 | | |
| | | | | –40°C to 125°C | 33 | | |
| Output noise spectral density | f = 120 Hz | | 25°C | 2 | | | μV/√Hz |
| Output noise voltage | 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω | C _O = 4.7 μF | 25°C | 265 | | | μVrms |
| | | C _O = 10 μF | 25°C | 212 | | | |
| | | C _O = 100 μF | 25°C | 135 | | | |
| PG trip-threshold voltage | V _O voltage decreasing from above V _{PG} | | –40°C to 125°C | 0.95 × V _{O(nom)} | | | V |
| PG hysteresis voltage | | | 25°C | 32 | | | mV |
| PG output low voltage | I _{PG} = 1.2 mA, V _I = 2.8 V | | 25°C | 0.22 | 0.4 | | V |
| | | | –40°C to 125°C | 0.4 | | | |

[†] CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

[‡] Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7201Q, TPS7225Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

SLVS102G – MARCH 1995 – REVISED JUNE 2000

TPS7248Q electrical characteristics, $I_O = 10\text{ mA}$, $V_I = 5.85\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($\text{CSR}^\dagger = 1\text{ }\Omega$), SENSE shorted to OUT (unless otherwise noted)

| PARAMETER | TEST CONDITIONS‡ | | T _J | TPS7248Q | | | UNIT |
|--------------------------------|---|-------------------------|----------------|----------------------------|-----|-----|--------|
| | | | | MIN | TYP | MAX | |
| Output voltage | V _I = 5.85 V, I _O = 10 mA | | 25°C | 4.85 | | | V |
| | 5.85 V ≤ V _I ≤ 10 V, 5 mA ≤ I _O ≤ 250 mA | | −40°C to 125°C | 4.75 4.95 | | | |
| Dropout voltage | I _O = 10 mA, V _I = 4.75 V | | 25°C | 10 19 | | | mV |
| | | | −40°C to 125°C | 30 | | | |
| | I _O = 100 mA, V _I = 4.75 V | | 25°C | 90 100 | | | |
| | | | −40°C to 125°C | 150 | | | |
| | I _O = 250 mA, V _I = 4.75 V | | 25°C | 216 250 | | | |
| | | | −40°C to 125°C | 285 | | | |
| Pass-element series resistance | (4.75 V − V _O)/I _O , I _O = 250 mA | | 25°C | 0.8 1 | | | Ω |
| | | | −40°C to 125°C | 1.4 | | | |
| Input regulation | V _I = 5.85 V to 10 V, 50 μA ≤ I _O ≤ 250 mA | | 25°C | 34 | | | mV |
| | | | −40°C to 125°C | 50 | | | |
| Output regulation | I _O = 5 mA to 250 mA, 5.85 V ≤ V _I ≤ 10 V | | 25°C | 43 55 | | | mV |
| | | | −40°C to 125°C | 95 | | | |
| | I _O = 50 μA to 250 mA, 5.85 V ≤ V _I ≤ 10 V | | 25°C | 55 75 | | | |
| | | | −40°C to 125°C | 135 | | | |
| Ripple rejection | f = 120 Hz | I _O = 50 μA | 25°C | 42 53 | | | dB |
| | | | −40°C to 125°C | 36 | | | |
| | | I _O = 250 mA | 25°C | 36 46 | | | |
| | | | −40°C to 125°C | 34 | | | |
| Output noise spectral density | f = 120 Hz | | 25°C | 2 | | | μV/√Hz |
| Output noise voltage | 10 Hz ≤ f ≤ 100 kHz, CSR† = 1 Ω | C _O = 4.7 μF | 25°C | 370 | | | μVrms |
| | | C _O = 10 μF | 25°C | 290 | | | |
| | | C _O = 100 μF | 25°C | 168 | | | |
| PG trip-threshold voltage | V _O voltage decreasing from above V _{PG} | | −40°C to 125°C | 0.95 × V _{O(nom)} | | | V |
| PG hysteresis voltage | | | 25°C | 50 | | | mV |
| PG output low voltage | I _{PG} = 1.2 mA, V _I = 4.12 V | | 25°C | 0.2 0.4 | | | V |
| | | | −40°C to 125°C | 0.4 | | | |

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7201Q, TPS7225Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

SLVS102G – MARCH 1995 – REVISED JUNE 2000

TPS7250Q electrical characteristics, $I_O = 10\text{ mA}$, $V_I = 6\text{ V}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($CSR^\dagger = 1\text{ }\Omega$), SENSE shorted to OUT (unless otherwise noted)

| PARAMETER | TEST CONDITIONS‡ | | T _J | TPS7250Q | | | UNIT |
|--------------------------------|---|--------------------------|----------------|----------------------------|-----|-------|--------|
| | | | | MIN | TYP | MAX | |
| Output voltage | V _I = 6 V, I _O = 10 mA | | 25°C | 5 | | | V |
| | 6 V ≤ V _I ≤ 10 V, 5 mA ≤ I _O ≤ 250 mA | | –40°C to 125°C | 4.9 | 5.1 | | |
| Dropout voltage | I _O = 10 mA, V _I = 4.88 V | | 25°C | 8 12 | | | mV |
| | | | –40°C to 125°C | 30 | | | |
| | I _O = 100 mA, V _I = 4.88 V | | 25°C | 76 85 | | | |
| | | | –40°C to 125°C | 136 | | | |
| | I _O = 250 mA, V _I = 4.88 V | | 25°C | 190 206 | | | |
| | | | –40°C to 125°C | 312 | | | |
| Pass-element series resistance | (4.88 V – V _O)/I _O , I _O = 250 mA | V _I = 4.88 V, | 25°C | 0.76 | | 0.825 | Ω |
| | | | –40°C to 125°C | 1.25 | | | |
| Input regulation | V _I = 6 V to 10 V, 50 μA ≤ I _O ≤ 250 mA | | 25°C | 28 | | | mV |
| | | | –40°C to 125°C | 35 | | | |
| Output regulation | I _O = 5 mA to 250 mA, 6 V ≤ V _I ≤ 10 V | | 25°C | 46 | | 61 | mV |
| | | | –40°C to 125°C | 100 | | | |
| | I _O = 50 μA to 250 mA, 6 V ≤ V _I ≤ 10 V | | 25°C | 59 | | 79 | |
| | | | –40°C to 125°C | 150 | | | |
| Ripple rejection | f = 120 Hz | I _O = 50 μA | 25°C | 41 | 52 | | dB |
| | | | –40°C to 125°C | 37 | | | |
| | | I _O = 250 mA | 25°C | 36 | 46 | | |
| | | | –40°C to 125°C | 32 | | | |
| Output noise spectral density | f = 120 Hz | | 25°C | 2 | | | μV/√Hz |
| Output noise voltage | 10 Hz ≤ f ≤ 100 kHz, CSRT = 1 Ω | C _O = 4.7 μF | 25°C | 390 | | | μVrms |
| | | C _O = 10 μF | 25°C | 300 | | | |
| | | C _O = 100 μF | 25°C | 175 | | | |
| PG trip-threshold voltage | V _O voltage decreasing from above V _{PG} | | –40°C to 125°C | 0.95 × V _{O(nom)} | | | V |
| PG hysteresis voltage | | | 25°C | 50 | | | mV |
| PG output low voltage | I _{PG} = 1.2 mA, V _I = 4.25 V | | 25°C | 0.19 | | 0.4 | V |
| | | | –40°C to 125°C | 0.4 | | | |

[†] CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

[‡] Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7201Q, TPS7225Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

SLVS102G – MARCH 1995 – REVISED JUNE 2000

electrical characteristics, $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($CSR^\dagger = 1\text{ }\Omega$), $T_J = 25^\circ\text{C}$, SENSE/FB shorted to OUT (unless otherwise noted)

| PARAMETER | TEST CONDITIONS‡ | TPS72xxY | | | UNIT |
|---------------------------------------|---|----------|-----|-----|------------------|
| | | MIN | TYP | MAX | |
| Ground current (active mode) | $\overline{EN} \leq 0.5\text{ V}$, $V_I = V_O + 1\text{ V}$, $0\text{ mA} \leq I_O \leq 250\text{ mA}$ | | 180 | | μA |
| Output current limit threshold | $V_O = 0\text{ V}$, $V_I = 10\text{ V}$ | | 0.6 | | A |
| Thermal shutdown junction temperature | | | 165 | | $^\circ\text{C}$ |
| \overline{EN} hysteresis voltage | | | 50 | | mV |
| Minimum V_I for active pass element | | | 1.9 | | V |
| Minimum V_I for valid PG | $I_{PG} = 300\text{ }\mu\text{A}$ | | 1.1 | | V |

electrical characteristics, $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($CSR^\dagger = 1\text{ }\Omega$), $T_J = 25^\circ\text{C}$, FB shorted to OUT at device leads (unless otherwise noted)

| PARAMETER | TEST CONDITIONS‡ | TPS7201Y | | | UNIT |
|---|---|---------------------------------------|-------|-----|--------------------------------|
| | | MIN | TYP | MAX | |
| Reference voltage (measured at FB with OUT connected to FB) | $V_I = 3.5\text{ V}$, $I_O = 10\text{ mA}$ | | 1.188 | | V |
| Pass-element series resistance (see Note 3) | $V_I = 2.4\text{ V}$, § $50\text{ }\mu\text{A} \leq I_O \leq 100\text{ mA}$ | | 2.1 | | Ω |
| | $V_I = 2.4\text{ V}$, § $100\text{ mA} \leq I_O \leq 200\text{ mA}$ | | 2.9 | | |
| | $V_I = 2.9\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$ | | 1.6 | | |
| | $V_I = 3.9\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$ | | 1 | | |
| | $V_I = 5.9\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$ | | 0.8 | | |
| Output regulation | $3\text{ V} \leq V_I \leq 10\text{ V}$, See Note 2 $I_O = 5\text{ mA}$ to 250 mA , | | 15 | | mV |
| | $3\text{ V} \leq V_I \leq 10\text{ V}$, See Note 2 $I_O = 50\text{ }\mu\text{A}$ to 250 mA , | | 17 | | |
| Ripple rejection | $V_I = 3.5\text{ V}$, $f = 120\text{ Hz}$ | $I_O = 50\text{ }\mu\text{A}$ | 60 | | dB |
| | | $I_O = 250\text{ mA}$, See Note 2 | 50 | | |
| Output noise spectral density | $V_I = 3.5\text{ V}$, $f = 120\text{ Hz}$ | | 2 | | $\mu\text{V}/\sqrt{\text{Hz}}$ |
| Output noise voltage | $V_I = 3.5\text{ V}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$, $CSR^\dagger = 1\text{ }\Omega$ | $C_O = 4.7\text{ }\mu\text{F}$ | 235 | | μV_{rms} |
| | | $C_O = 10\text{ }\mu\text{F}$ | 190 | | |
| | | $C_O = 100\text{ }\mu\text{F}$ | 125 | | |
| PG hysteresis voltage¶ | $V_I = 3.5\text{ V}$, Measured at V_{FB} | | 12 | | mV |
| PG output low voltage¶ | $V_I = 2.13\text{ V}$, $I_{PG} = 400\text{ }\mu\text{A}$ | | 0.1 | | V |
| FB input current | $V_I = 3.5\text{ V}$ | | 0.1 | | nA |

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

§ This voltage is not recommended.

¶ Output voltage programmed to 2.5 V with closed-loop configuration (see application information).

NOTES: 2 When $V_I < 2.9\text{ V}$ and $I_O > 100\text{ mA}$ simultaneously, pass element $r_{DS(on)}$ increases (see Figure 10) to a point such that the resulting dropout voltage prevents the regulator from maintaining the specified tolerance range.

3 To calculate dropout voltage, use equation:

$$V_{DO} = I_O \cdot r_{DS(on)}$$

$r_{DS(on)}$ is a function of both output current and input voltage. The parametric table lists $r_{DS(on)}$ for $V_I = 2.4\text{ V}$, 2.9 V , 3.9 V , and 5.9 V , which corresponds to dropout conditions for programmed output voltages of 2.5 V , 3 V , 4 V , and 6 V , respectively. For other programmed values, refer to Figures 10 and 11.



TPS7201Q, TPS7225Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

SLVS102G – MARCH 1995 – REVISED JUNE 2000

electrical characteristics, $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($CSR^\dagger = 1\text{ }\Omega$), $T_J = 25^\circ\text{C}$, FB shorted to OUT at device leads (unless otherwise noted)

| PARAMETER | TEST CONDITIONS‡ | TPS7225Y | | | UNIT |
|--------------------------------|--|--------------------------------|------|-----|--------------------------------|
| | | MIN | TYP | MAX | |
| Output voltage | $V_I = 3.5\text{ V}$, $I_O = 10\text{ mA}$ | | 2.5 | | V |
| Dropout voltage | $V_I = 2.97\text{ V}$, $I_O = 250\text{ mA}$ | | 560 | | mV |
| Pass-element series resistance | $(2.97\text{ V} - V_O)/I_O$, $V_I = 2.97\text{ V}$, $I_O = 250\text{ mA}$ | | 2.24 | | Ω |
| Input regulation | $V_I = 3.5\text{ V to }10\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$ | | 9 | | mV |
| Output regulation | $3.5\text{ V} \leq V_I \leq 10\text{ V}$, $I_O = 5\text{ mA to }250\text{ mA}$ | | 28 | | mV |
| | $3.5\text{ V} \leq V_I \leq 10\text{ V}$, $I_O = 50\text{ }\mu\text{A to }250\text{ mA}$ | | 24 | | |
| Ripple rejection | $V_I = 3.5\text{ V}$, $f = 120\text{ Hz}$ | $I_O = 50\text{ }\mu\text{A}$ | | 58 | dB |
| | | $I_O = 250\text{ mA}$ | | 46 | |
| Output noise spectral density | $V_I = 3.5\text{ V}$, $f = 120\text{ Hz}$ | | 2 | | $\mu\text{V}/\sqrt{\text{Hz}}$ |
| Output noise voltage | $V_I = 3.5\text{ V}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$, $CSR^\dagger = 1\text{ }\Omega$ | $C_O = 4.7\text{ }\mu\text{F}$ | | 248 | μV_{rms} |
| | | $C_O = 10\text{ }\mu\text{F}$ | | 200 | |
| | | $C_O = 100\text{ }\mu\text{F}$ | | 130 | |
| PG hysteresis voltage | $V_I = 3.5\text{ V}$ | | 50 | | mV |
| PG output low voltage | $V_I = 2.13\text{ V}$, $I_{PG} = 1.2\text{ mA}$ | | 0.3 | | V |

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

TPS7201Q, TPS7225Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS
SLVS102G – MARCH 1995 – REVISED JUNE 2000

electrical characteristics, $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($\text{CSR}^\dagger = 1\text{ }\Omega$), $T_J = 25^\circ\text{C}$, SENSE shorted to OUT (unless otherwise noted)

| PARAMETER | TEST CONDITIONS‡ | TPS7230Y | | | UNIT |
|--------------------------------|---|--------------------------------|------|-----|--------------------------------|
| | | MIN | TYP | MAX | |
| Output voltage | $V_I = 4\text{ V}$, $I_O = 10\text{ mA}$ | | 3 | | V |
| Dropout voltage | $V_I = 2.97\text{ V}$, $I_O = 100\text{ mA}$ | | 145 | | mV |
| | $V_I = 2.97\text{ V}$, $I_O = 250\text{ mA}$ | | 390 | | |
| Pass-element series resistance | $(2.97\text{ V} - V_O)/I_O$, $V_I = 2.97\text{ V}$, $I_O = 250\text{ mA}$ | | 1.56 | | Ω |
| Input regulation | $V_I = 4\text{ V to } 10\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$ | | 9 | | mV |
| Output regulation | $4\text{ V} \leq V_I \leq 10\text{ V}$, $I_O = 5\text{ mA to } 250\text{ mA}$ | | 34 | | mV |
| | $4\text{ V} \leq V_I \leq 10\text{ V}$, $I_O = 50\text{ }\mu\text{A to } 250\text{ mA}$ | | 41 | | |
| Ripple rejection | $V_I = 4\text{ V}$, $f = 120\text{ Hz}$ | $I_O = 50\text{ }\mu\text{A}$ | 56 | | dB |
| | | $I_O = 250\text{ mA}$ | 45 | | |
| Output noise spectral density | $V_I = 4\text{ V}$, $f = 120\text{ Hz}$ | | 2 | | $\mu\text{V}/\sqrt{\text{Hz}}$ |
| Output noise voltage | $V_I = 4\text{ V}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSR}^\dagger = 1\text{ }\Omega$ | $C_O = 4.7\text{ }\mu\text{F}$ | 256 | | μV_{rms} |
| | | $C_O = 10\text{ }\mu\text{F}$ | 206 | | |
| | | $C_O = 100\text{ }\mu\text{F}$ | 132 | | |
| PG hysteresis voltage | $V_I = 4\text{ V}$ | | 50 | | mV |
| PG output low voltage | $V_I = 2.55\text{ V}$, $I_{\text{PG}} = 1.2\text{ mA}$ | | 0.25 | | V |

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

| PARAMETER | TEST CONDITIONS‡ | TPS7233Y | | | UNIT |
|--------------------------------|---|--------------------------------|------|-----|--------------------------------|
| | | MIN | TYP | MAX | |
| Output voltage | $V_I = 4.3\text{ V}$, $I_O = 10\text{ mA}$ | | 3.3 | | V |
| Dropout voltage | $V_I = 3.23\text{ V}$, $I_O = 10\text{ mA}$ | | 14 | | mV |
| | $V_I = 3.23\text{ V}$, $I_O = 100\text{ mA}$ | | 140 | | |
| | $V_I = 3.23\text{ V}$, $I_O = 250\text{ mA}$ | | 360 | | |
| Pass-element series resistance | $(3.23\text{ V} - V_O)/I_O$, $V_I = 3.23\text{ V}$, $I_O = 250\text{ mA}$ | | 1.5 | | Ω |
| Input regulation | $V_I = 4.3\text{ V to } 10\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$ | | 8 | | mV |
| Output regulation | $4.3\text{ V} \leq V_I \leq 10\text{ V}$, $I_O = 5\text{ mA to } 250\text{ mA}$ | | 32 | | mV |
| | $4.3\text{ V} \leq V_I \leq 10\text{ V}$, $I_O = 50\text{ }\mu\text{A to } 250\text{ mA}$ | | 41 | | |
| Ripple rejection | $V_I = 4.3\text{ V}$, $f = 120\text{ Hz}$ | $I_O = 50\text{ }\mu\text{A}$ | 52 | | dB |
| | | $I_O = 250\text{ mA}$ | 44 | | |
| Output noise spectral density | $V_I = 4.3\text{ V}$, $f = 120\text{ Hz}$ | | 2 | | $\mu\text{V}/\sqrt{\text{Hz}}$ |
| Output noise voltage | $V_I = 4.3\text{ V}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSR}^\dagger = 1\text{ }\Omega$ | $C_O = 4.7\text{ }\mu\text{F}$ | 265 | | μV_{rms} |
| | | $C_O = 10\text{ }\mu\text{F}$ | 212 | | |
| | | $C_O = 100\text{ }\mu\text{F}$ | 135 | | |
| PG hysteresis voltage | $V_I = 4.3\text{ V}$ | | 32 | | mV |
| PG output low voltage | $V_I = 2.8\text{ V}$, $I_{\text{PG}} = 1.2\text{ mA}$ | | 0.22 | | V |

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



TPS7201Q, TPS7225Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

SLVS102G – MARCH 1995 – REVISED JUNE 2000

electrical characteristics, $I_O = 10\text{ mA}$, $\overline{EN} = 0\text{ V}$, $C_O = 4.7\text{ }\mu\text{F}$ ($\text{CSR}^\dagger = 1\text{ }\Omega$), $T_J = 25^\circ\text{C}$, SENSE shorted to OUT (unless otherwise noted) (continued)

| PARAMETER | TEST CONDITIONS‡ | TPS7248Y | | | UNIT |
|--------------------------------|--|--------------------------------|------|-----|--------------------------------|
| | | MIN | TYP | MAX | |
| Output voltage | $V_I = 5.85\text{ V}$, $I_O = 10\text{ mA}$ | | 4.85 | | V |
| Dropout voltage | $V_I = 4.75\text{ V}$, $I_O = 10\text{ mA}$ | | 10 | | mV |
| | $V_I = 4.75\text{ V}$, $I_O = 100\text{ mA}$ | | 90 | | |
| | $V_I = 4.75\text{ V}$, $I_O = 250\text{ mA}$ | | 216 | | |
| Pass-element series resistance | $(4.75\text{ V} - V_O)/I_O$, $V_I = 4.75\text{ V}$, $I_O = 250\text{ mA}$ | | 0.8 | | Ω |
| Output regulation | $5.85\text{ V} \leq V_I \leq 10\text{ V}$, $I_O = 5\text{ mA to } 250\text{ mA}$ | | 43 | | mV |
| | $5.85\text{ V} \leq V_I \leq 10\text{ V}$, $I_O = 50\text{ }\mu\text{A to } 250\text{ mA}$ | | 55 | | |
| Ripple rejection | $V_I = 5.85\text{ V}$, $f = 120\text{ Hz}$ | $I_O = 50\text{ }\mu\text{A}$ | | 53 | dB |
| | | $I_O = 250\text{ mA}$ | | 46 | |
| Output noise spectral density | $V_I = 5.85\text{ V}$, $f = 120\text{ Hz}$ | | 2 | | $\mu\text{V}/\sqrt{\text{Hz}}$ |
| Output noise voltage | $V_I = 5.85\text{ V}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSR}^\dagger = 1\text{ }\Omega$ | $C_O = 4.7\text{ }\mu\text{F}$ | | 370 | μV_{rms} |
| | | $C_O = 10\text{ }\mu\text{F}$ | | 290 | |
| | | $C_O = 100\text{ }\mu\text{F}$ | | 168 | |
| PG hysteresis voltage | $V_I = 5.85\text{ V}$ | | 50 | | mV |
| PG output low voltage | $V_I = 4.12\text{ V}$, $I_{\text{PG}} = 1.2\text{ mA}$ | | 0.2 | | V |

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

| PARAMETER | TEST CONDITIONS‡ | TPS7250Y | | | UNIT |
|--------------------------------|---|--------------------------------|------|-----|--------------------------------|
| | | MIN | TYP | MAX | |
| Output voltage | $V_I = 6\text{ V}$, $I_O = 10\text{ mA}$ | | 5 | | V |
| Dropout voltage | $V_I = 4.88\text{ V}$, $I_O = 10\text{ mA}$ | | 8 | | mV |
| | $V_I = 4.88\text{ V}$, $I_O = 100\text{ mA}$ | | 76 | | |
| | $V_I = 4.88\text{ V}$, $I_O = 250\text{ mA}$ | | 190 | | |
| Pass-element series resistance | $(4.88\text{ V} - V_O)/I_O$, $V_I = 4.88\text{ V}$, $I_O = 250\text{ mA}$ | | 0.76 | | Ω |
| Input regulation | $V_I = 6\text{ V to } 10\text{ V}$, $50\text{ }\mu\text{A} \leq I_O \leq 250\text{ mA}$ | | | | mV |
| Output regulation | $6\text{ V} \leq V_I \leq 10\text{ V}$, $I_O = 5\text{ mA to } 250\text{ mA}$ | | 46 | | mV |
| | $6\text{ V} \leq V_I \leq 10\text{ V}$, $I_O = 50\text{ }\mu\text{A to } 250\text{ mA}$ | | 59 | | |
| Ripple rejection | $V_I = 6\text{ V}$, $f = 120\text{ Hz}$ | $I_O = 50\text{ }\mu\text{A}$ | | 52 | dB |
| | | $I_O = 250\text{ mA}$ | | 46 | |
| Output noise spectral density | $V_I = 6\text{ V}$, $f = 120\text{ Hz}$ | | 2 | | $\mu\text{V}/\sqrt{\text{Hz}}$ |
| Output noise voltage | $V_I = 6\text{ V}$, $10\text{ Hz} \leq f \leq 100\text{ kHz}$, $\text{CSR}^\dagger = 1\text{ }\Omega$ | $C_O = 4.7\text{ }\mu\text{F}$ | | 390 | μV_{rms} |
| | | $C_O = 10\text{ }\mu\text{F}$ | | 300 | |
| | | $C_O = 100\text{ }\mu\text{F}$ | | 175 | |
| PG hysteresis voltage | $V_I = 6\text{ V}$ | | 50 | | mV |
| PG output low voltage | $V_I = 4.25\text{ V}$, $I_{\text{PG}} = 1.2\text{ mA}$ | | 0.19 | | V |

† CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

‡ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.



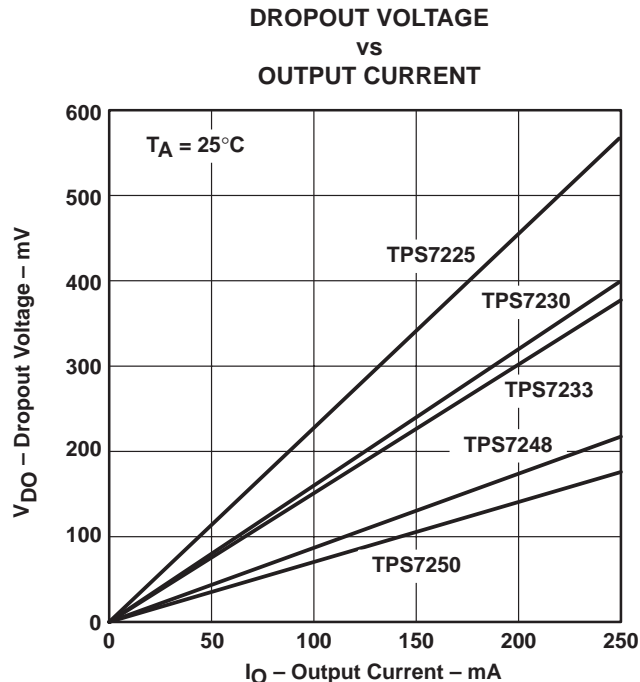
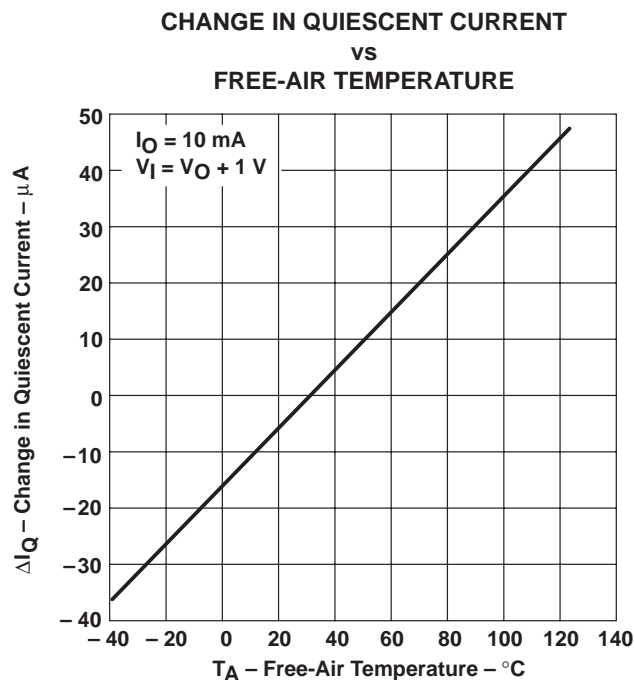
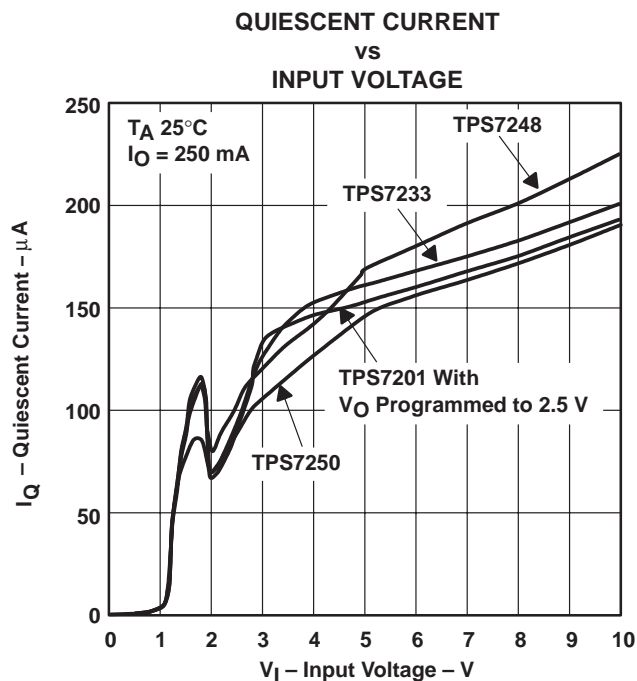
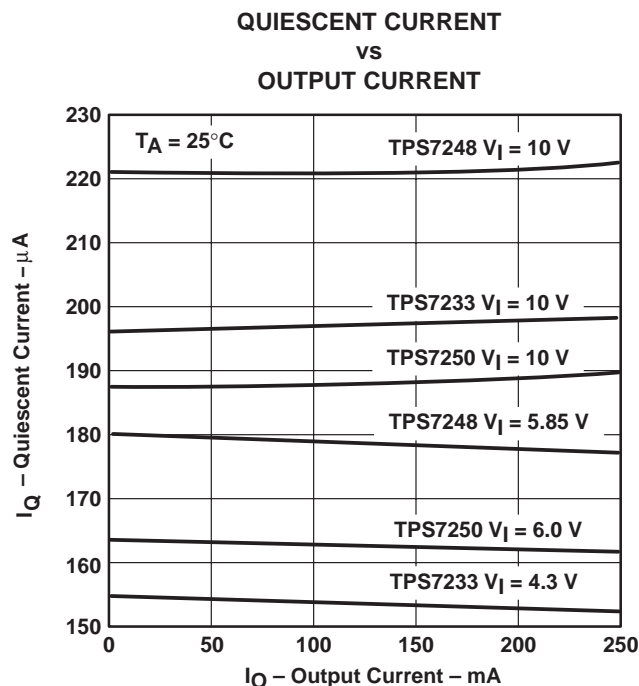
TYPICAL CHARACTERISTICS

Table of Graphs

| | | | FIGURE |
|----------------------|---|--|--------|
| I_Q | Quiescent current | vs Output current | 5 |
| | | vs Input voltage | 6 |
| ΔI_Q^\dagger | Change in quiescent current | vs Free-air temperature | 7 |
| V_{DO} | Dropout voltage | vs Output current | 8 |
| ΔV_{DO} | Change in dropout voltage | vs Free-air temperature | 9 |
| V_{DO} | Dropout voltage (TPS7201 only) | vs Output current | 10 |
| $r_{DS(on)}$ | Pass-element series resistance | vs Input voltage | 11 |
| ΔV_O | Change in output voltage | vs Free-air temperature | 12 |
| V_O | Output voltage | vs Input voltage | 13 |
| | Line regulation (TPS7201, TPS7233, TPS7248, TPS7250) | | 14 |
| | Load regulation (TPS7225, TPS7233, TPS7248, TPS7250) | | 15 |
| $V_{O(PG)}$ | Power-good (PG) voltage | vs Output voltage | 16 |
| $r_{DS(on)PG}$ | Power-good (PG) on-resistance | vs Input voltage | 17 |
| V_I | Minimum input voltage for valid PG | vs Free-air temperature | 18 |
| | Output voltage response from enable (\overline{EN}) | | 19 |
| | Load transient response (TPS7201/TPS7233) | | 20 |
| | Load transient response (TPS7248/TPS7250) | | 21 |
| | Line transient response (TPS7201) | | 22 |
| | Line transient response (TPS7233) | | 23 |
| | Line transient response (TPS7248/TPS7250) | | 24 |
| | Ripple rejection | vs Frequency | 25 |
| | Output Spectral Noise Density | vs Frequency | 26 |
| | Compensation series resistance (CSR) | vs Output current ($C_O = 4.7 \mu F$) | 27 |
| | | vs Added ceramic capacitance ($C_O = 4.7 \mu F$) | 28 |
| | | vs Output current ($C_O = 10 \mu F$) | 29 |
| | | vs Added ceramic capacitance ($C_O = 10 \mu F$) | 30 |

[†] This symbol is not currently listed within EIA or JEDEC standards for semiconductor symbology.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

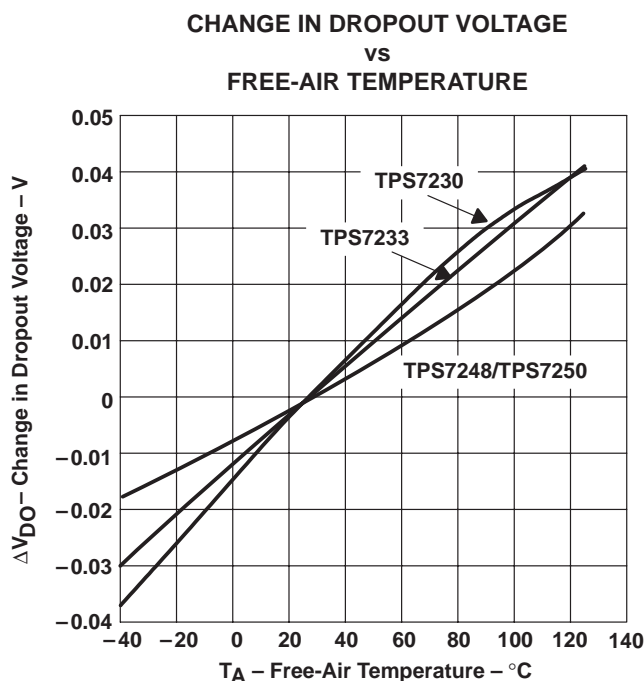
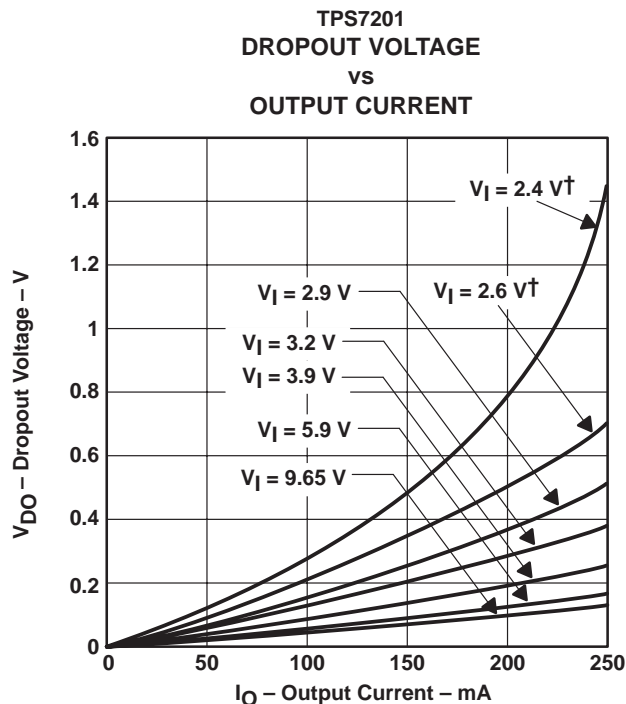


Figure 9



† This voltage is not recommended.

Figure 10

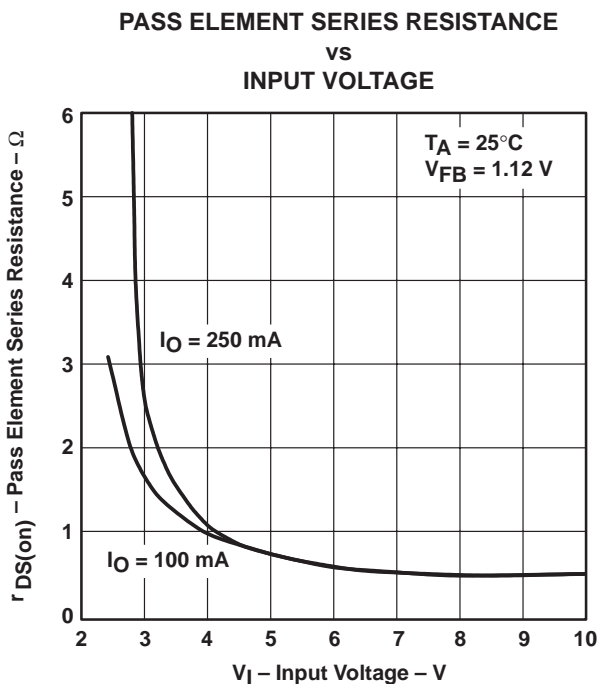


Figure 11

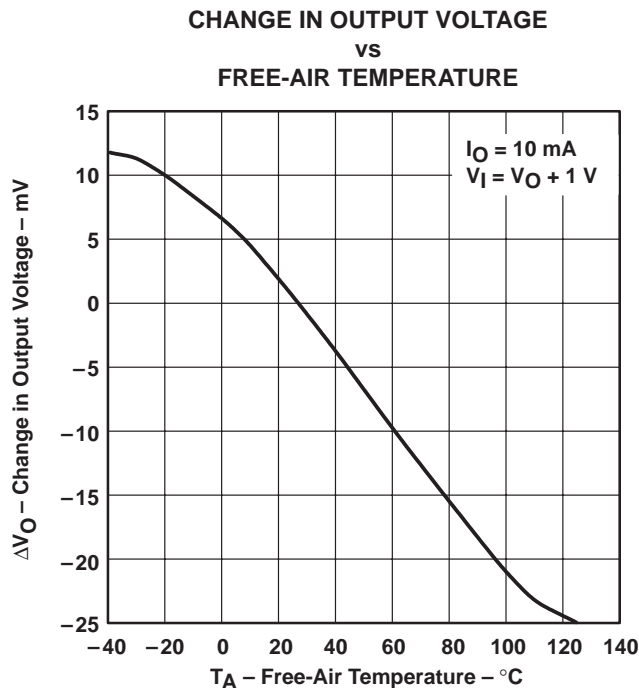
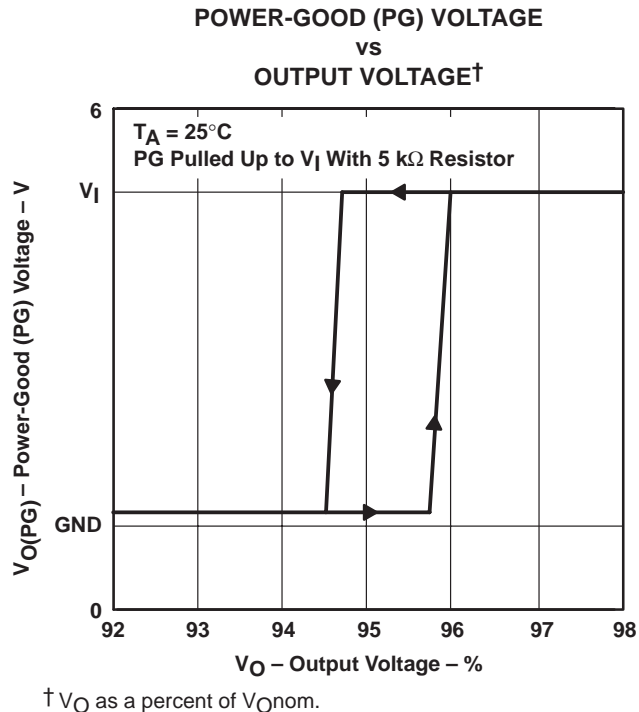
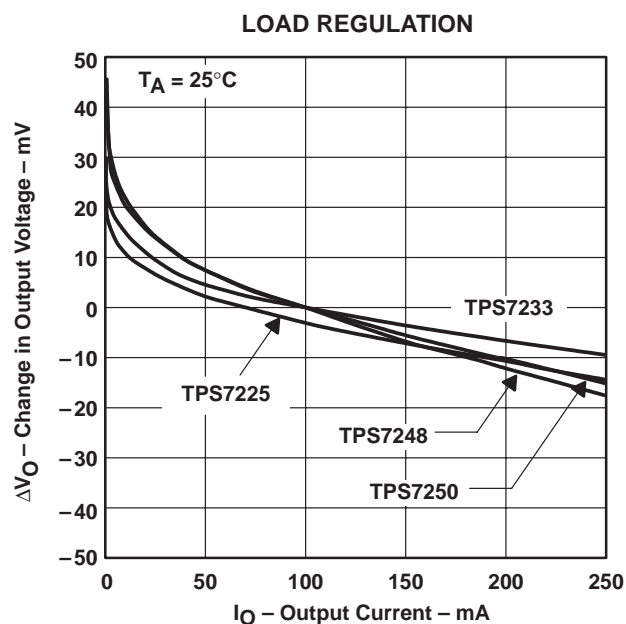
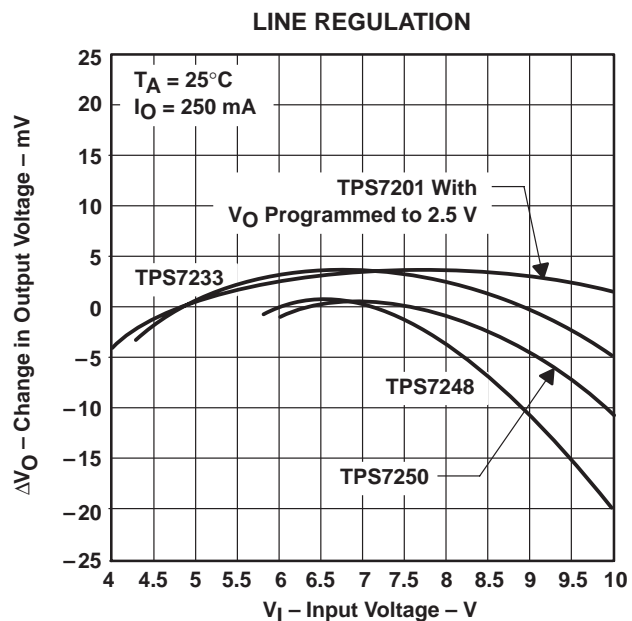
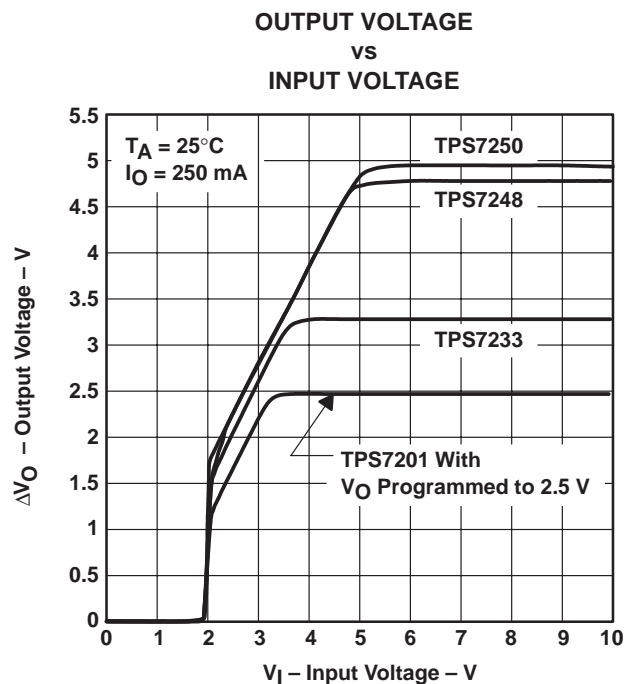


Figure 12

TPS7201Q, TPS7225Q, TPS7230Q
 TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
 MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

SLVS102G – MARCH 1995 – REVISED JUNE 2000

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

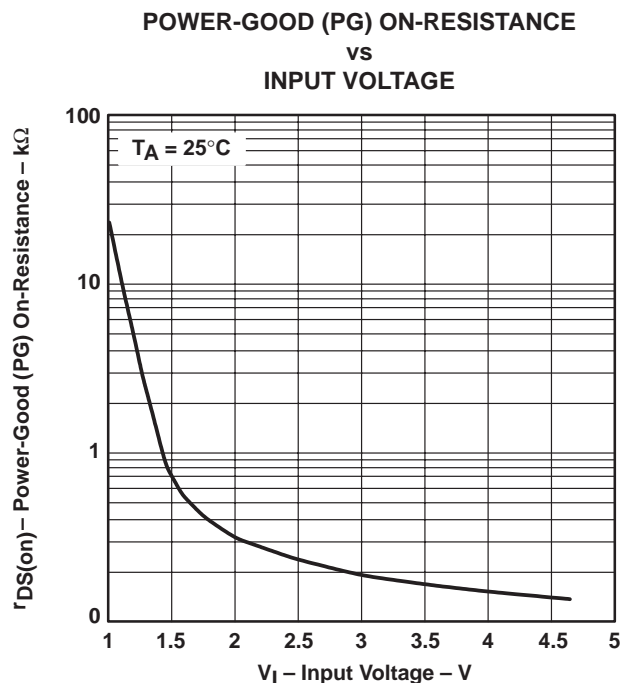


Figure 17

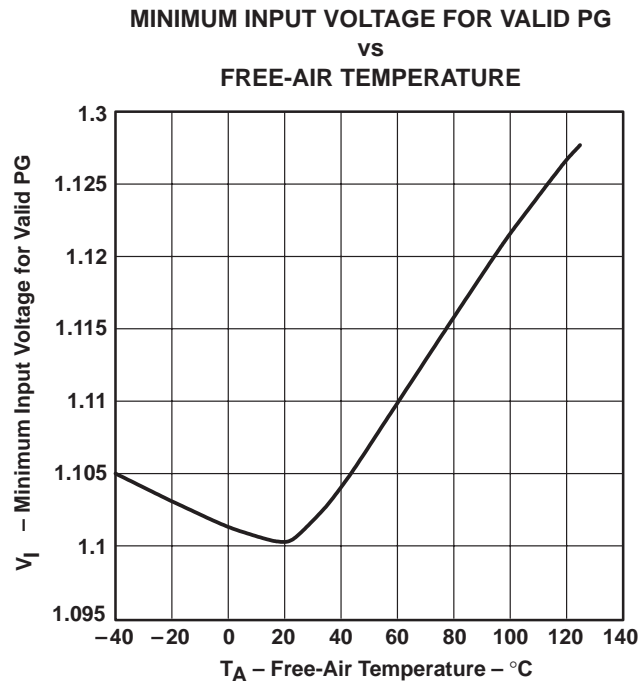


Figure 18

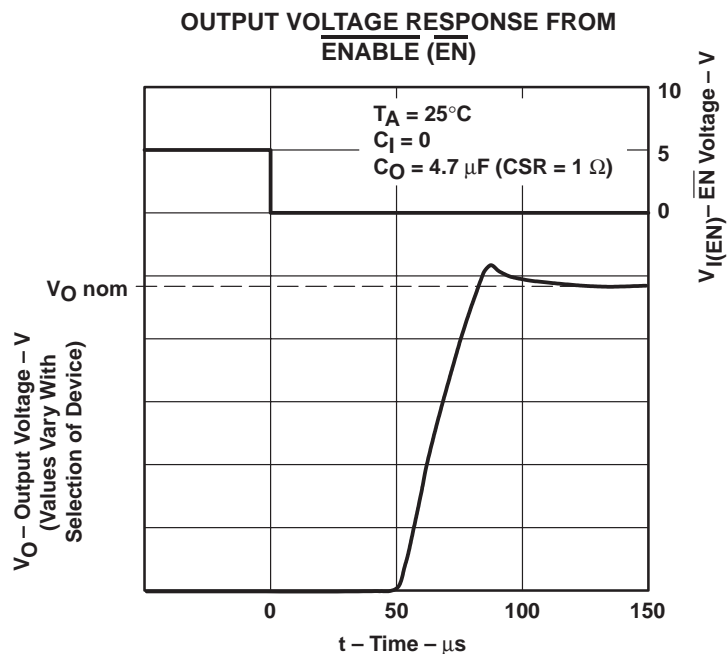


Figure 19

TYPICAL CHARACTERISTICS

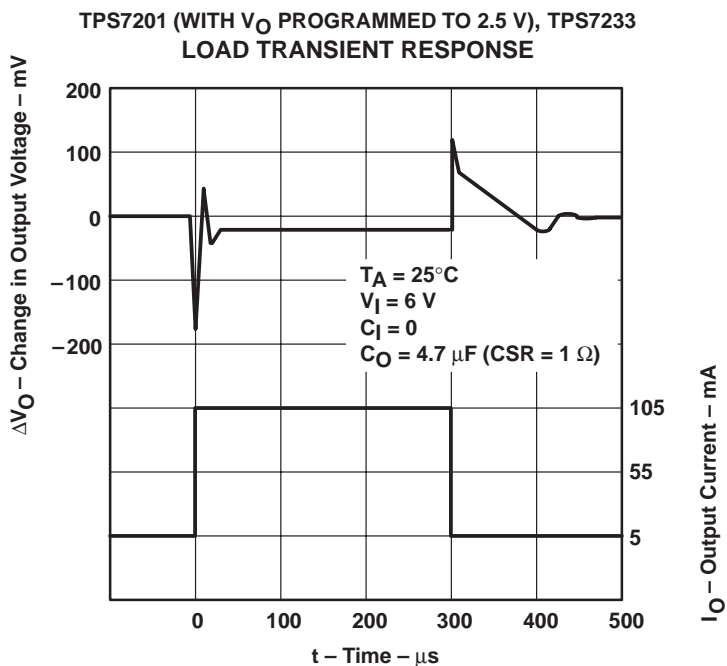


Figure 20

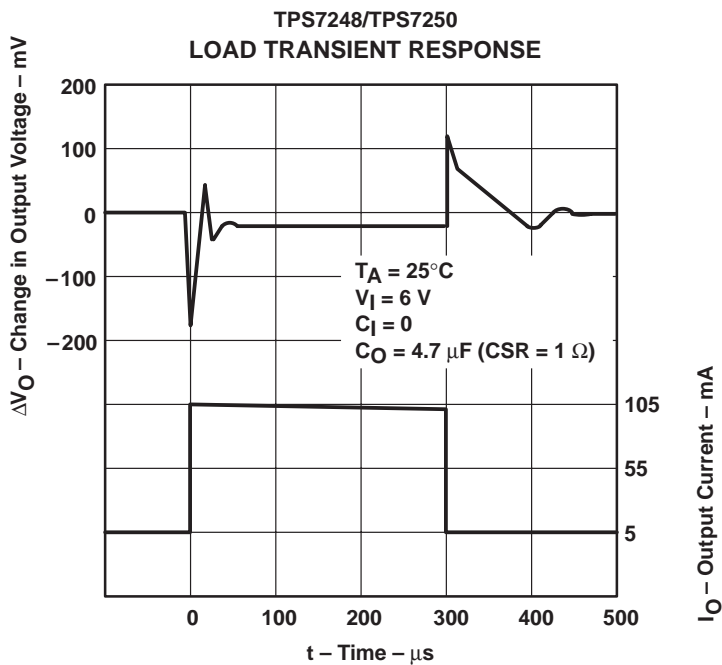


Figure 21

TYPICAL CHARACTERISTICS

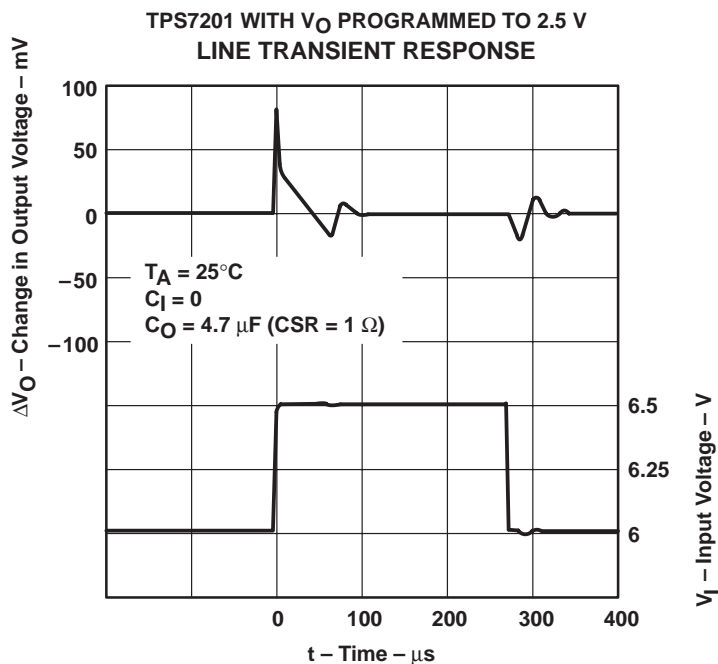


Figure 22

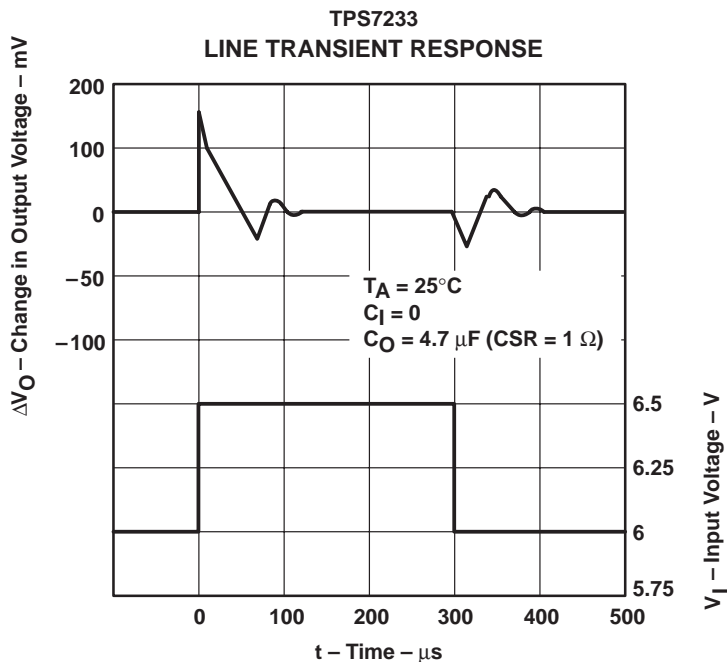


Figure 23

TPS7201Q, TPS7225Q, TPS7230Q
 TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
 MICROWPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

SLVS102G – MARCH 1995 – REVISED JUNE 2000

TYPICAL CHARACTERISTICS

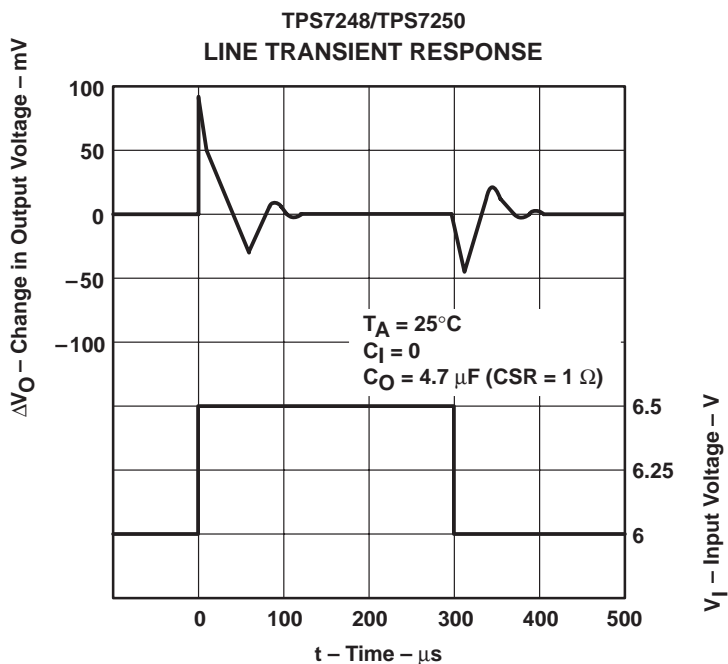


Figure 24

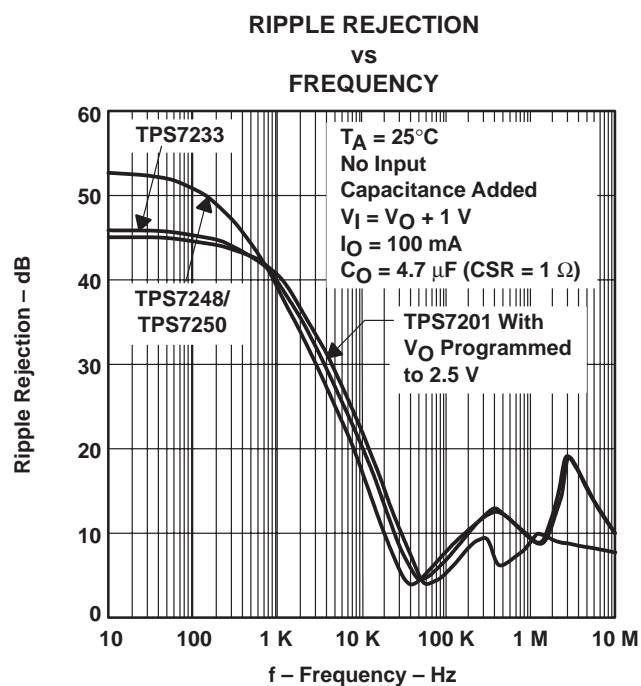


Figure 25

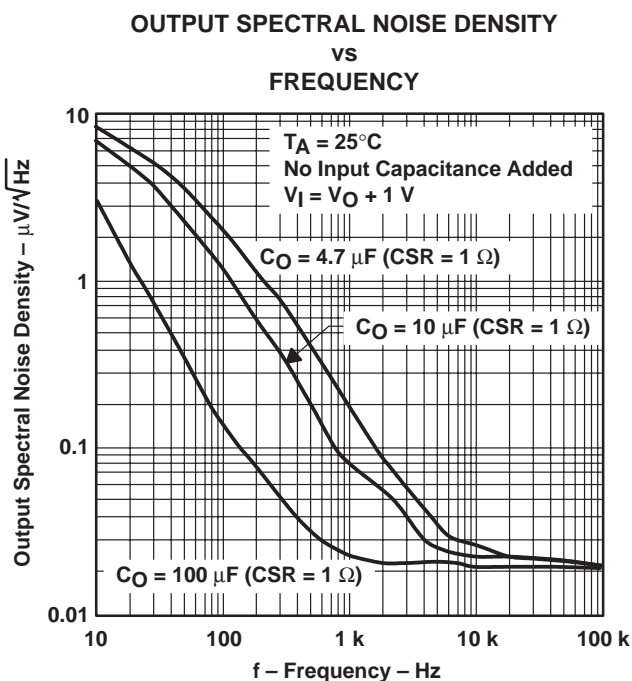


Figure 26

TYPICAL CHARACTERISTICS

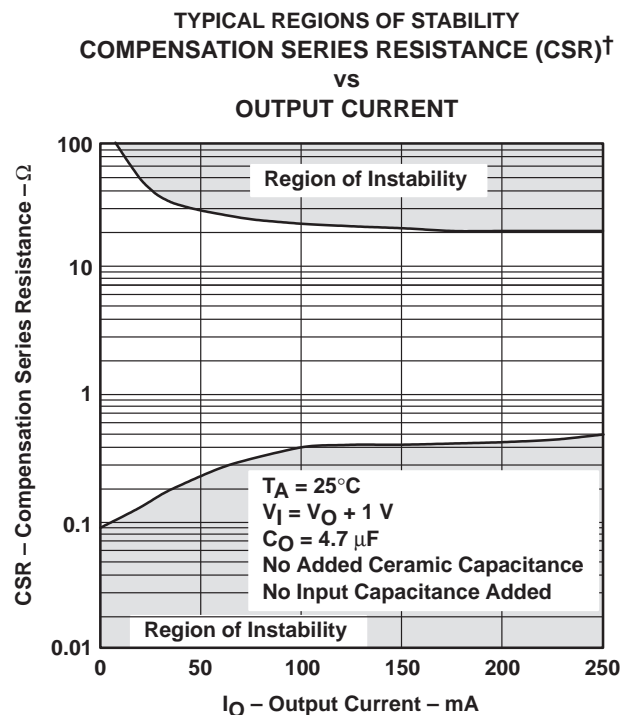


Figure 27

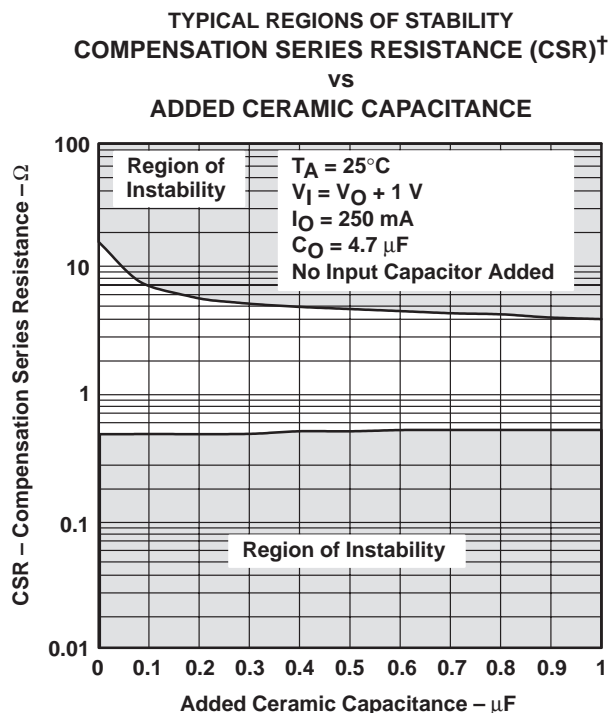


Figure 28

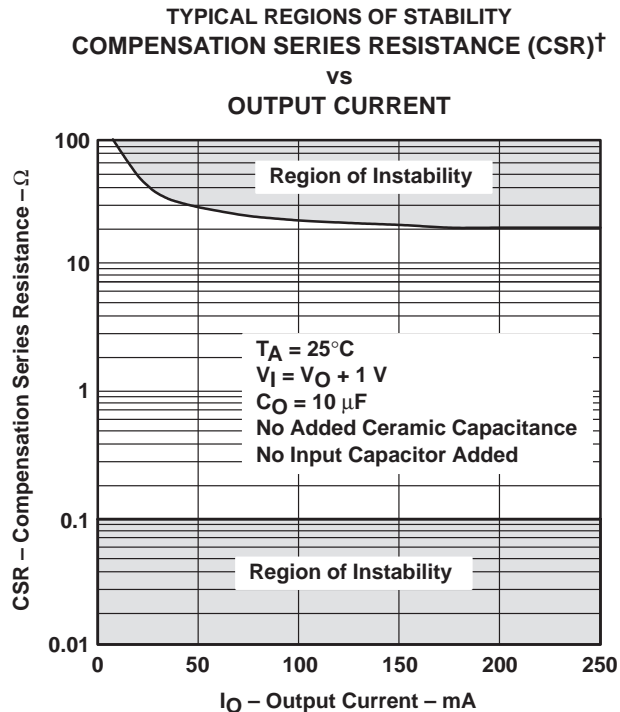


Figure 29

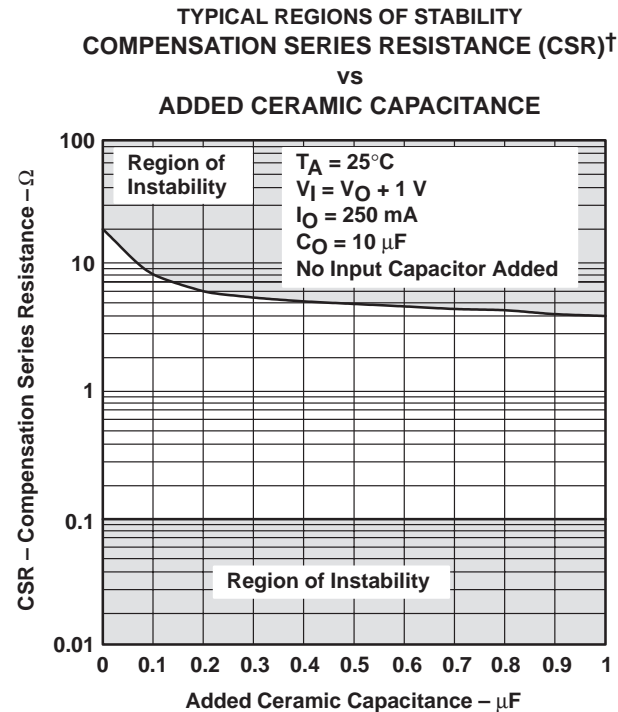


Figure 30

[†] CSR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

TPS7201Q, TPS7225Q, TPS7230Q
TPS7233Q, TPS7248Q, TPS7250Q, TPS72xxY
MICROPOWER LOW-DROPOUT (LDO) VOLTAGE REGULATORS

SLVS102G – MARCH 1995 – REVISED JUNE 2000

APPLICATION INFORMATION

The design of the TPS72xx family of low-dropout (LDO) regulators is based on the higher-current TPS71xx family. These new families of regulators have been optimized for use in battery-operated equipment and feature extremely low dropout voltages, low supply currents that remain constant over the full-output-current range of the device, and an enable input to reduce supply currents to less than 0.5 μ A when the regulator is turned off.

device operation

The TPS72xx uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP-pass-element LDO designs. The PMOS transistor is a voltage-controlled device that, unlike a PNP transistor, does not require increased drive current as output current increases. Supply current in the TPS72xx is essentially constant from no-load to maximum.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 1 A; further load increases reduce the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above 165°C. Recovery is automatic when the junction temperature drops approximately 5°C below the high temperature trip point. The PMOS pass element includes a back diode that safely conducts reverse current when the input voltage level drops below the output voltage level.

A logic high on the enable input, $\overline{\text{EN}}$, shuts off the output and reduces the supply current to less than 0.5 μ A. $\overline{\text{EN}}$ should be grounded in applications where the shutdown feature is not used.

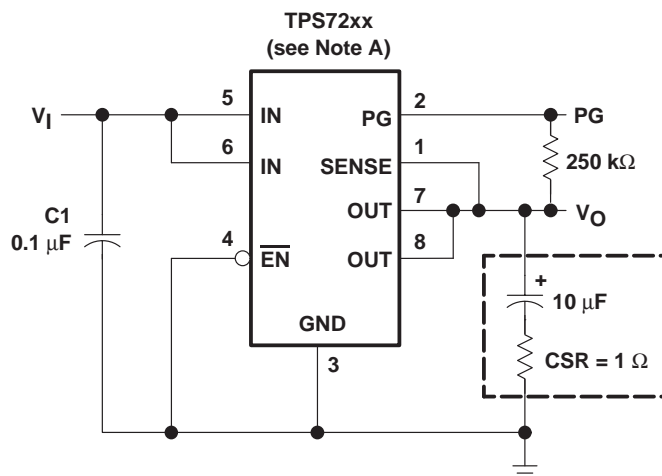
Power good (PG) is an open-drain output signal used to indicate output-voltage status. A comparator circuit continuously monitors the output voltage. When the output drops to approximately 95% of its nominal regulated value, the comparator turns on and pulls PG low.

Transient loads or line pulses can also cause activation of PG if proper care is not taken in selecting the input and output capacitors. Load transients that are faster than 5 μ s can cause a signal on PG if high-ESR output capacitors (greater than approximately 7 Ω) are used. A 1- μ s transient causes a PG signal when using an output capacitor with greater than 3.5 Ω of ESR. It is interesting to note that the output-voltage spike during the transient can drop well below the reset threshold and still not trip if the transient duration is short. A 1- μ s transient must drop at least 500 mV below the threshold before tripping the PG circuit. A 2- μ s transient trips PG at just 400 mV below the threshold. Lower-ESR output capacitors help by reducing the drop in output voltage during a transient and should be used when fast transients are expected.

A typical application circuit is shown in Figure 31.



APPLICATION INFORMATION



NOTE A: TPS7225, TPS7230, TPS7233, TPS7248, TPS7250
 (fixed-voltage options).

Figure 31. Typical Application Circuit

external capacitor requirements

Although not required, a 0.047- μ F to 0.1- μ F ceramic bypass input capacitor, connected between IN and GND and located close to the TPS72xx, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

An output capacitor is required to stabilize the internal feedback loop. For most applications, a 10- μ F to 15- μ F solid-tantalum capacitor with a 0.5- Ω resistor (see capacitor selection table) in series is sufficient. The maximum capacitor ESR should be limited to 1.3 Ω to allow for ESR doubling at cold temperatures. Figure 32 shows the transient response of a 5-mA to 85-mA load using a 10- μ F output capacitor with a total ESR of 1.7 Ω .

A 4.7- μ F solid-tantalum capacitor in series with a 1- Ω resistor may also be used (see Figures 27 and 28) provided the ESR of the capacitor does not exceed 1 Ω at room temperature and 2 Ω over the full operating temperature range.

APPLICATION INFORMATION

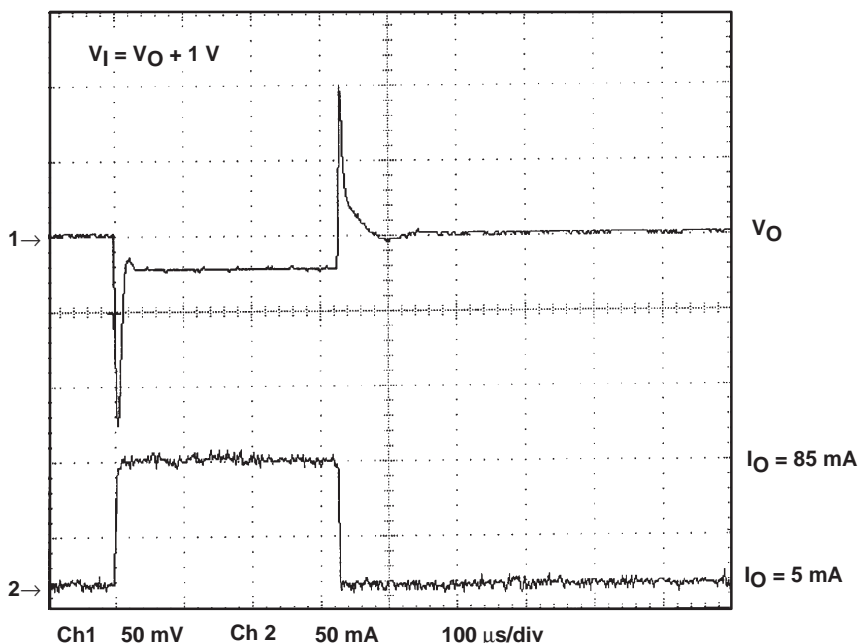


Figure 32. Load Transient Response (CSR total = 1.7 Ω), TPS7248Q

A partial listing of surface-mount capacitors usable with the TPS72xx family is provided below. This information (along with the stability graphs, Figures 27 through 30) is included to assist the designer in selecting suitable capacitors.

CAPACITOR SELECTION

| PART NO. | MFR. | VALUE | MAX ESR [†] | SIZE (H × L × W) [†] |
|-----------------|---------|-------------|----------------------|-------------------------------|
| 592D156X0020R2T | Sprague | 15 μF, 20 V | 1.1 | 1.2 × 7.2 × 6 |
| 595D156X0025C2T | Sprague | 15 μF, 25 V | 1 | 2.5 × 7.1 × 3.2 |
| 595D106X0025C2T | Sprague | 10 μF, 25 V | 1.2 | 2.5 × 7.1 × 3.2 |
| 695D106X0035G2T | Sprague | 10 μF, 35 V | 1.3 | 2.5 × 7.6 × 2.5 |

[†] Size is in mm. ESR is maximum resistance in ohms at 100 kHz and T_A = 25°C. Listings are sorted by height.

sense-pin connection

SENSE must be connected to OUT for proper operation of the regulator. Normally this connection should be as short as possible; however, remote sense may be implemented in critical applications when proper care of the circuit path is exercised. SENSE internally connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network, and any noise pickup on the PCB trace will feed through to the regulator output. SENSE must be routed to minimize noise pickup. Filtering SENSE using an RC network is not recommended because of the possibility of inducing regulator instability.

APPLICATION INFORMATION

output voltage programming

The output voltage of the TPS7201 adjustable regulator is programmed using an external resistor divider as shown in Figure 33. The output voltage is calculated using:

$$V_O = V_{\text{ref}} \cdot \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Where:

$$V_{\text{ref}} = 1.188 \text{ V typ (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 7-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 kΩ to set the divider current at 7 μA and then calculate R1 using:

$$R_1 = \left(\frac{V_O}{V_{\text{ref}}} - 1\right) \cdot R_2 \quad (2)$$

OUTPUT VOLTAGE
PROGRAMMING GUIDE

| OUTPUT VOLTAGE (V) | DIVIDER RESISTANCE (kΩ)† | |
|--------------------------|-----------------------------|-----|
| | R1 | R2 |
| 2.5 | 191 | 169 |
| 3.3 | 309 | 169 |
| 3.6 | 348 | 169 |
| 4 | 402 | 169 |
| 5 | 549 | 169 |
| 6.4 | 750 | 169 |

† 1% values shown.

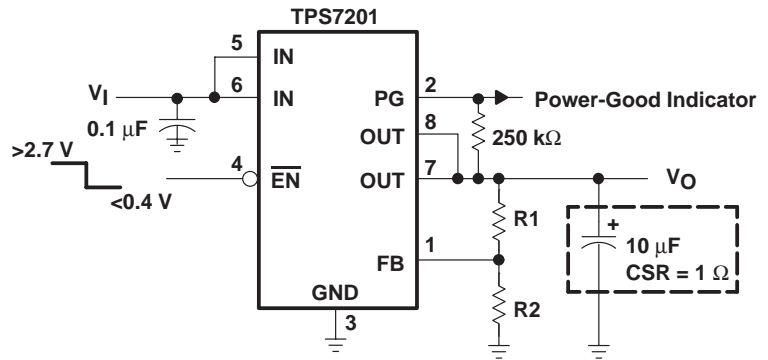


Figure 33. TPS7201 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature allowable to avoid damaging the device is 150°C. These restrictions limit the power dissipation that the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where:

T_{Jmax} is the maximum allowable junction temperature, i.e., 150°C absolute maximum and 125°C recommended operating temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 172°C/W for the 8-terminal SOIC and 238°C/W for the 8-terminal TSSOP.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \cdot I_O$$

Power dissipation resulting from quiescent current is negligible.

regulator protection

The TPS72xx PMOS-pass transistor has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

The TPS72xx also features internal current limiting and thermal protection. During normal operation, the TPS72xx limits output current to approximately 1 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled, regulator operation resumes.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS7201QD | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 7201Q | Samples |
| TPS7201QDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 7201Q | Samples |
| TPS7201QDRG4 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 7201Q | Samples |
| TPS7201QP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 125 | TPS7201QP | Samples |
| TPS7201QPW | ACTIVE | TSSOP | PW | 8 | 150 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PT7201 | Samples |
| TPS7201QPWG4 | ACTIVE | TSSOP | PW | 8 | 150 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PT7201 | Samples |
| TPS7201QPWR | ACTIVE | TSSOP | PW | 8 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PT7201 | Samples |
| TPS7225QD | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 150 | 7225Q | Samples |
| TPS7225QDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 150 | 7225Q | Samples |
| TPS7225QP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 150 | TPS7225QP | Samples |
| TPS7225QPWR | ACTIVE | TSSOP | PW | 8 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 150 | PT7225 | Samples |
| TPS7230QD | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 150 | 7230Q | Samples |
| TPS7230QP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 125 | TPS7230QP | Samples |
| TPS7230QPWR | ACTIVE | TSSOP | PW | 8 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PT7230 | Samples |
| TPS7233QD | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 7233Q | Samples |
| TPS7233QDG4 | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 7233Q | Samples |
| TPS7233QDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 7233Q | Samples |
| TPS7233QP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 125 | TPS7233QP | Samples |
| TPS7233QPE4 | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 125 | TPS7233QP | Samples |
| TPS7233QPWR | ACTIVE | TSSOP | PW | 8 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PT7233 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS7248QD | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 7248Q | Samples |
| TPS7250QD | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 7250Q | Samples |
| TPS7250QDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 7250Q | Samples |
| TPS7250QP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 125 | TPS7250QP | Samples |
| TPS7250QPWR | ACTIVE | TSSOP | PW | 8 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PT7250 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS7201QDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS7201QPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TPS7225QDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS7225QPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TPS7230QPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TPS7233QDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS7233QPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TPS7250QDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS7250QPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |

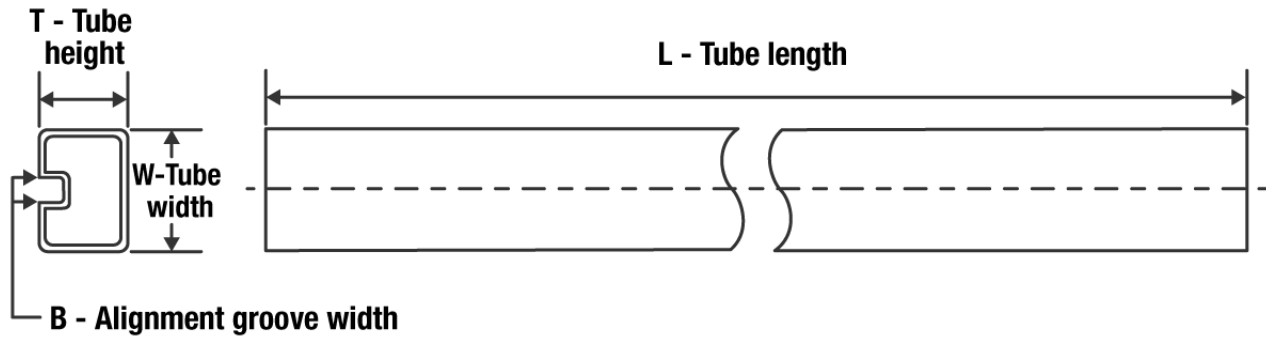
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS7201QDR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TPS7201QPWR | TSSOP | PW | 8 | 2000 | 853.0 | 449.0 | 35.0 |
| TPS7225QDR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TPS7225QPWR | TSSOP | PW | 8 | 2000 | 853.0 | 449.0 | 35.0 |
| TPS7230QPWR | TSSOP | PW | 8 | 2000 | 853.0 | 449.0 | 35.0 |
| TPS7233QDR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TPS7233QPWR | TSSOP | PW | 8 | 2000 | 853.0 | 449.0 | 35.0 |
| TPS7250QDR | SOIC | D | 8 | 2500 | 350.0 | 350.0 | 43.0 |
| TPS7250QPWR | TSSOP | PW | 8 | 2000 | 853.0 | 449.0 | 35.0 |

TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TPS7201QD | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TPS7201QP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TPS7201QPW | PW | TSSOP | 8 | 150 | 530 | 10.2 | 3600 | 3.5 |
| TPS7201QPWG4 | PW | TSSOP | 8 | 150 | 530 | 10.2 | 3600 | 3.5 |
| TPS7225QD | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TPS7225QP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TPS7230QD | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TPS7230QP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TPS7233QD | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TPS7233QDG4 | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TPS7233QP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TPS7233QPE4 | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TPS7248QD | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TPS7250QD | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| TPS7250QP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

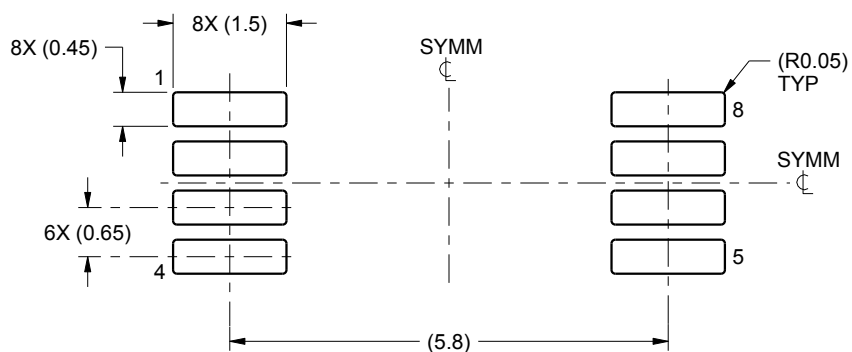
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

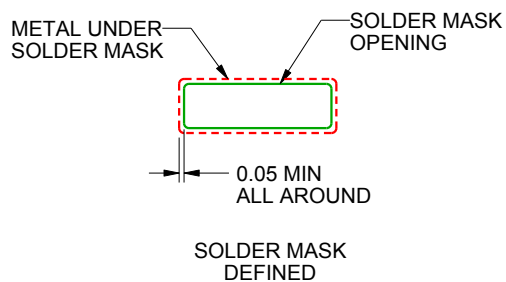
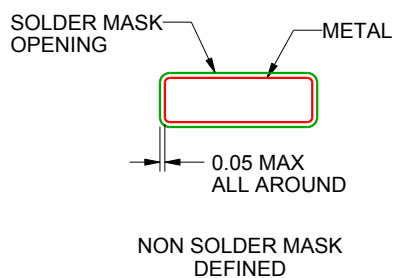
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D0008A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated