TPS74701 500-mA Low-Dropout Linear Regulator With Programmable Soft-Start

1 Features

- V_{OUT} Range: 0.8 V to 3.6 V
- Ultralow V_{IN} Range: 0.8 V to 5.5 V
- V_{BIAS} Range 2.7 V to 5.5 V
- Low Dropout: 50 mV Typically at 500 mA, V_{BIAS} = 5 V
- Power Good (PG) Output Allows Supply Monitoring or Provides a Sequencing Signal for Other Supplies
- 2% Accuracy Over Line, Load, and Temperature
- Programmable Soft-Start Provides Linear Voltage Start-Up
- V_{BIAS} Permits Low V_{IN} Operation With Good Transient Response
- Stable With Any Output Capacitor ≥ 2.2 µF
- Available in a Small 3-mm × 3-mm × 1-mm 10-Pin Package

2 Applications

- FPGA Applications
- DSP Core and I/O Voltages
- Post-Regulation Applications
- Applications With Special Start-Up Time or Sequencing Requirements
- Hot-Swap and Inrush Controls

3 Description

The TPS74701 low-dropout (LDO) linear regulator provides an easy-to-use, robust power management solution for a wide variety of applications. User-programmable soft-start minimizes stress on the input power source by reducing capacitive inrush current on start-up. The soft-start is monotonic and well-suited for powering many different types of processors and ASICs. The enable input and power good output allow easy sequencing with external regulators. This complete flexibility permits the user to configure a solution that meets the sequencing requirements of FPGAs, DSPs, and other applications with special start-up requirements.

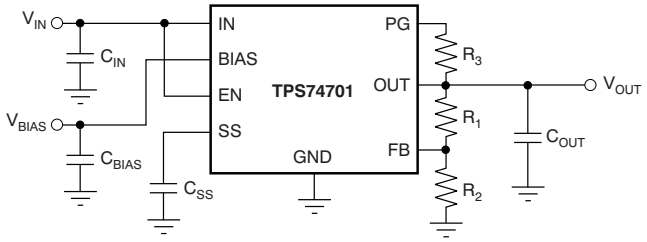
A precision reference and error amplifier deliver 2% accuracy over load, line, temperature, and process. The device is stable with any type of capacitor greater than or equal to 2.2 µF, and is fully specified from –40°C to 125°C. The TPS74701 is offered in a small 3-mm × 3-mm SON-10 package for compatibility with the TPS74801.

Device Information(1)

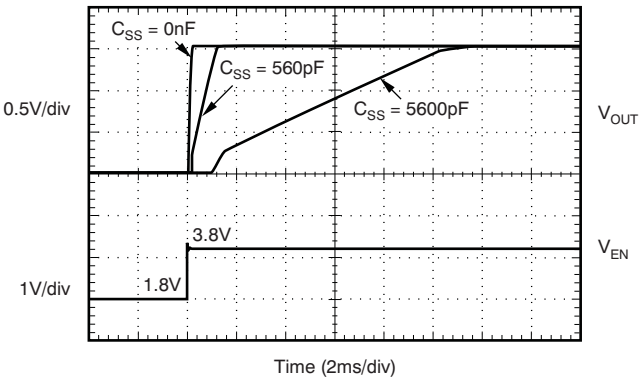
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS74701	VSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit (Adjustable)



Turnon Response



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (November 2010) to Revision G	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision E (August, 2010) to Revision F	Page
• Corrected equation for Table 3	14

Changes from Revision D (April, 2009) to Revision E	Page
• Revised *Power Dissipation* section	18
• Deleted (previously numbers) Figure 28 through Figure 30	18
• Added section	19

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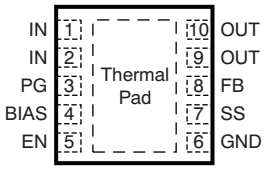
5 Pin Configuration and Functions

DRC Package
10-Pin SON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN	1, 2	I	Input to the device.
EN	5	I	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left unconnected.
SS	7	—	Soft-Start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left unconnected, the regulator output soft-start ramp time is typically 200 µs.
BIAS	4	I	Bias input voltage for error amplifier, reference, and internal control circuits.
PG	3	O	Power Good pin. An open-drain, active-high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V_{OUT} is below this threshold the pin is driven to a low-impedance state. A pullup resistor from 10 kΩ to 1 MΩ should be connected from this pin to a supply of up to 5.5 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left unconnected if output monitoring is not necessary.
FB	8	I	Feedback pin. The feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
OUT	9, 10	O	Regulated output voltage. A small capacitor (total typical capacitance ≥ 2.2 µF, ceramic) is needed from this pin to ground to assure stability.
NC	N/A	I	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
GND	6	I	Ground
Thermal Pad	—	I	Should be soldered to the ground plane for increased thermal performance.

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6 Specifications

6.1 Absolute Maximum Ratings

At T_J = –40°C to 125°C, unless otherwise noted. All voltages are with respect to GND.[1]

		MIN	MAX	UNIT
V_{IN}, V_{BIAS}	Input voltage	–0.3	6	V
V_{EN}	Enable voltage	–0.3	6	V
V_{PG}	Power good voltage	–0.3	6	V
I_{PG}	PG sink current	0	1.5	mA
V_{SS}	Soft-start voltage	–0.3	6	V
V_{FB}	Feedback voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	V_{IN} + 0.3	V
I_{OUT}	Maximum output current	Internally limited		
	Output short-circuit duration	Indefinite		
P_{DISS}	Continuous total power dissipation	See *Thermal Information*		
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	V_{OUT} + V_{DO} (V_{IN})	V_{OUT} + 0.3	5.5	V
V_{EN}	Enable supply voltage	0	V_{IN}	5.5	V
V_{BIAS}[1]	BIAS supply voltage	V_{OUT} + V_{DO} (V_{BIAS})[2]	V_{OUT} + 1.4[2]	5.5	V
V_{OUT}	Output voltage	0.8		3.3	V
I_{OUT}	Output current	0		500	mA
C_{OUT}	Output capacitor	2.2			µF
C_{IN}	Input capacitor[3]	1			µF
C_{BIAS}	Bias capacitor	0.1	1		µF
T_J	Operating junction temperature	–40		125	°C

(1) BIAS supply is required when V_{IN} is below V_{OUT} + 1.62 V.
(2) V_{BIAS} has a minimum voltage of 2.7 V or V_{OUT} + V_{DO} (V_{BIAS}), whichever is higher.
(3) If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 µF.

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6.4 Thermal Information

THERMAL METRIC[1][2]		TPS74701 DRC (VSON)[3] 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the DRC package are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
(a) The exposed pad is connected to the PCB ground layer through a 3×2 thermal via array.
(b) The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
(c) This data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3-inches × 3-inches copper area. To understand the effects of the copper area on thermal performance, see the *Power Dissipation* and *Estimating Junction Temperature* sections.

6.5 Electrical Characteristics

At V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3V, C_{BIAS} = 0.1 µF, C_{IN} = C_{OUT} = 10 µF, C_{NR} = 1 nF, I_{OUT} = 50 mA, V_{BIAS} = 5 V, and T_J = –40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		V_{OUT} + V_{DO}		5.5	V
V_{BIAS}	Bias pin voltage range		2.7		5.5	V
V_{REF}	Internal reference (Adjustable)	T_J = 25°C	0.796	0.8	0.804	V
V_{OUT}	Output voltage range	V_{IN} = 5 V, I_{OUT} = 500 mA	V_{REF}		3.6	V
	Accuracy(1)	2.97 V ≤ V_{BIAS} ≤ 5.5 V, 50 mA ≤ I_{OUT} ≤ 500 mA	–2%	±0.5%	2%	
V_{OUT}/V_{IN}	Line regulation	$V_{OUT\ (NOM)}$ + 0.3 ≤ V_{IN} ≤ 5.5 V		0.03		%/V
V_{OUT}/I_{OUT}	Load regulation	50 mA ≤ I_{OUT} ≤ 500 mA		0.09		%/A
V_{DO}	V_{IN} dropout voltage(2)	I_{OUT} = 500 mA, V_{BIAS} – $V_{OUT\ (NOM)}$ ≥ 1.62 V(3)		50	120	mV
	V_{BIAS} dropout voltage(2)	I_{OUT} = 500 mA, V_{IN} = V_{BIAS}		1.31	1.39	V
I_{CL}	Current limit	V_{OUT} = 80% × $V_{OUT\ (NOM)}$	800		1350	mA
I_{BIAS}	Bias pin current			1	2	mA
I_{SHDN}	Shutdown supply current (I_{GND})	V_{EN} ≤ 0.4 V		1	50	µA
I_{FB}	Feedback pin current		–1	0.150	1	µA
PSRR	Power-supply rejection (V_{IN} to V_{OUT})	1 kHz, I_{OUT} = 500 mA, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		60		dB
		300 kHz, I_{OUT} = 500 mA, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		30		
	Power-supply rejection (V_{BIAS} to V_{OUT})	1 kHz, I_{OUT} = 500 mA, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		50		dB
		300 kHz, I_{OUT} = 500 mA, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		30		
Noise	Output noise voltage	100 Hz to 100 kHz, I_{OUT} = 500 mA, C_{SS} = 0.001 µF		25 × V_{OUT}		$µV_{RMS}$
t_{STR}	Minimum start-up time	R_{LOAD} for I_{OUT} = 1 A, C_{SS} = open		200		µs
I_{SS}	Soft-start charging current	V_{SS} = 0.4 V		440		nA
$V_{EN,\ HI}$	Enable input high level		1.1		5.5	V
$V_{EN,\ LO}$	Enable input low level		0		0.4	V
$V_{EN,\ HYS}$	Enable pin hysteresis			50		mV
$V_{EN,\ DG}$	Enable pin deglitch time			20		µs
I_{EN}	Enable pin current	V_{EN} = 5 V		0.1	1	µA
V_{IT}	PG trip threshold	V_{OUT} decreasing	85	90	94	$\%V_{OUT}$
V_{HYS}	PG trip hysteresis			3		$\%V_{OUT}$
$V_{PG,\ LO}$	PG output low voltage	I_{PG} = 1 mA (sinking), V_{OUT} < V_{IT}			0.3	V
$I_{PG,\ LKG}$	PG leakage current	V_{PG} = 5.25 V, V_{OUT} > V_{IT}		0.1	1	µA
T_J	Operating junction temperature		–40		125	°C
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
		Reset, temperature decreasing		140		

(1) Adjustable devices tested at 0.8 V; resistor tolerance is not taken into account.
(2) Dropout is defined as the voltage from V_{IN} to V_{OUT} when V_{OUT} is 3% less than nominal.
(3) 1.62 V is a test condition of this device and can be adjusted by referring to Figure 6.

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6.6 Typical Characteristics: $V_{EN} = V_{IN}$

At T_J = 25°C, $V_{IN} = V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, $V_{EN} = V_{IN}$, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF, unless otherwise noted.

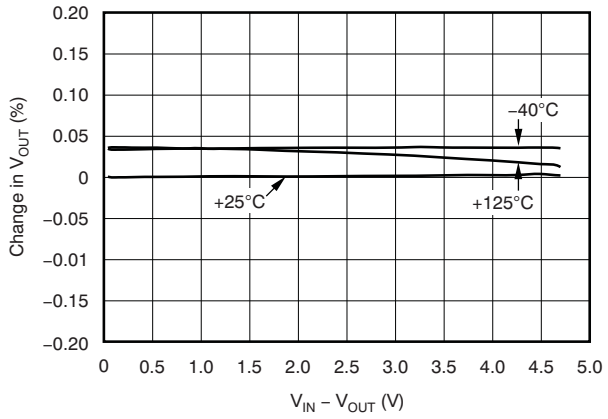

Figure 1. V_{IN} Line Regulation

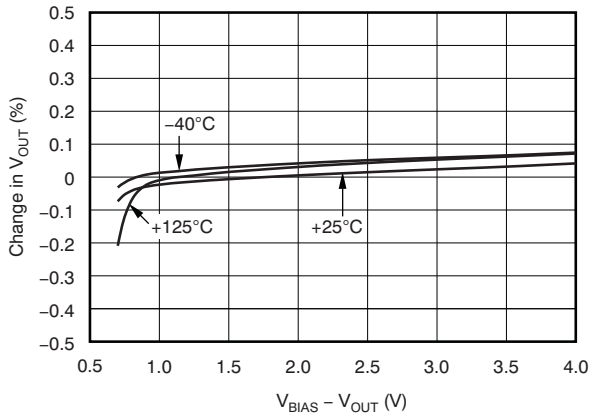

Figure 2. V_{BIAS} Line Regulation

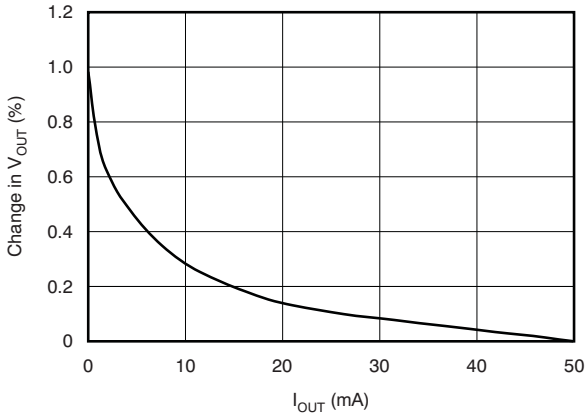

Figure 3. Load Regulation

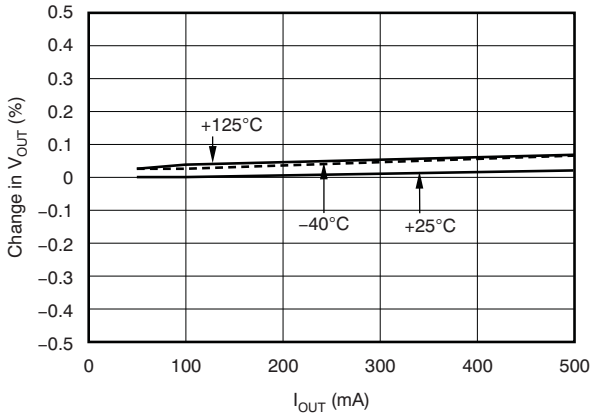

Figure 4. Load Regulation

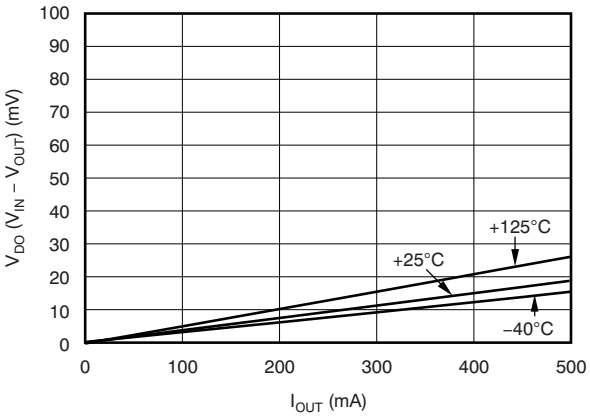

Figure 5. Dropout Voltage vs I_{OUT} and Temperature (T_J)

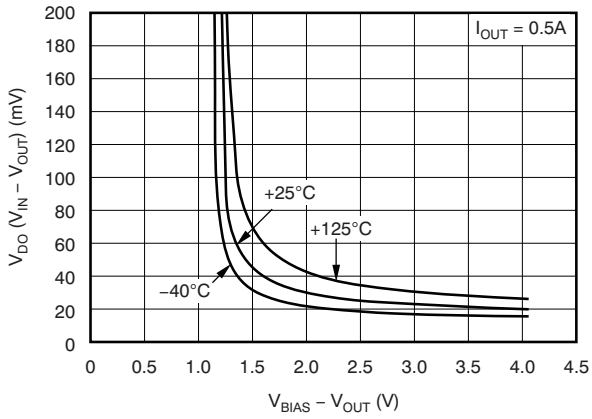

Figure 6. Dropout Voltage vs ($V_{BIAS} - V_{OUT}$) and Temperature (T_J)

Typical Characteristics: $V_{EN} = V_{IN}$ (continued)

At T_J = 25°C, $V_{IN} = V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, $V_{EN} = V_{IN}$, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF, unless otherwise noted.

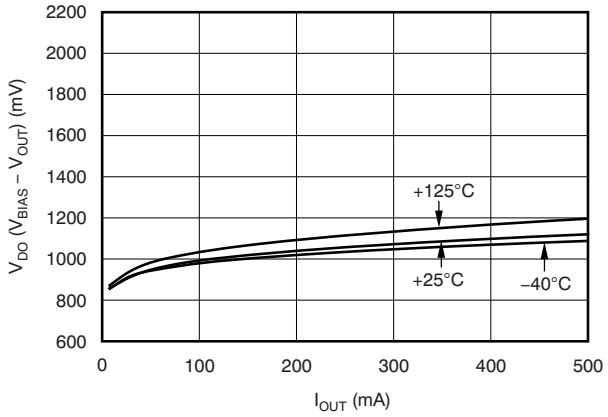

Figure 7. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (T_J)

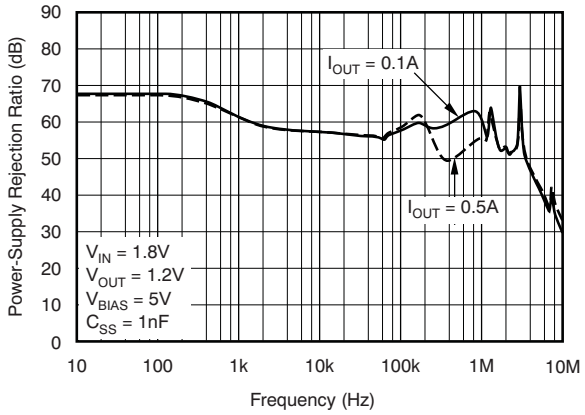

Figure 8. V_{BIAS} PSRR vs Frequency

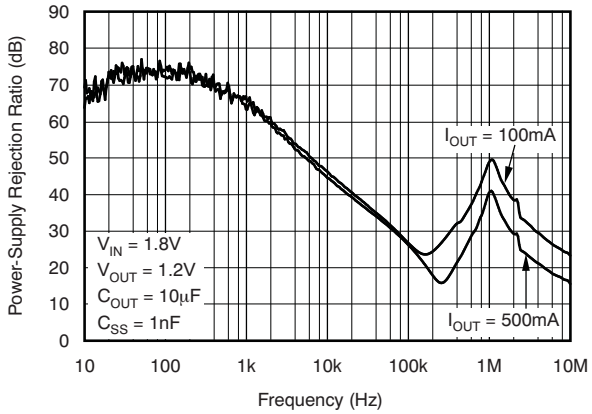

Figure 9. V_{IN} PSRR vs Frequency

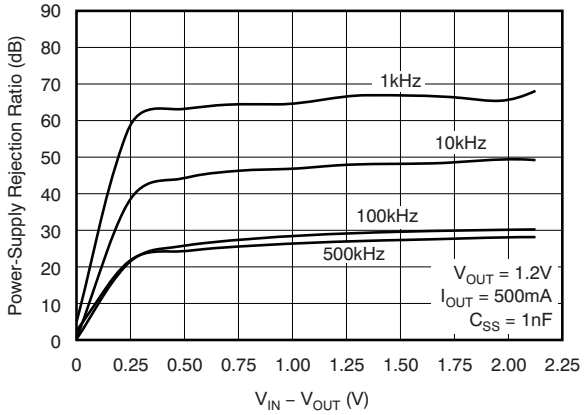

Figure 10. V_{IN} PSRR vs ($V_{IN} - V_{OUT}$)

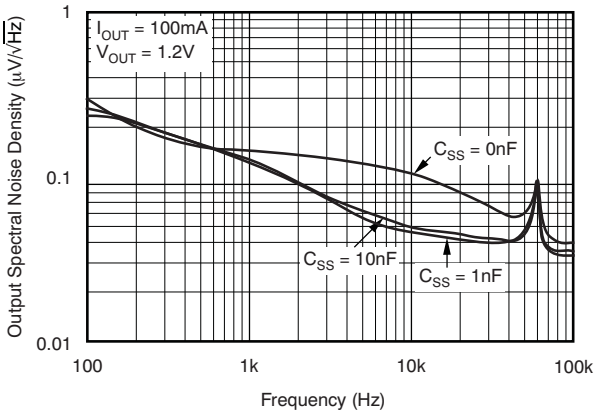

Figure 11. Noise Spectral Density

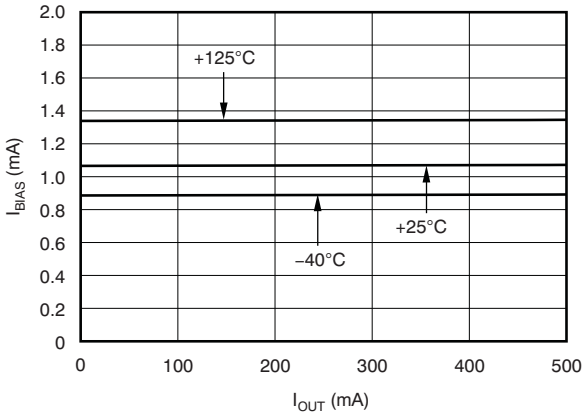

Figure 12. BIAS Pin Current vs I_{OUT} and Temperature (T_J)

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Typical Characteristics: $V_{EN} = V_{IN}$ (continued)

At T_J = 25°C, $V_{IN} = V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, $V_{EN} = V_{IN}$, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF, unless otherwise noted.

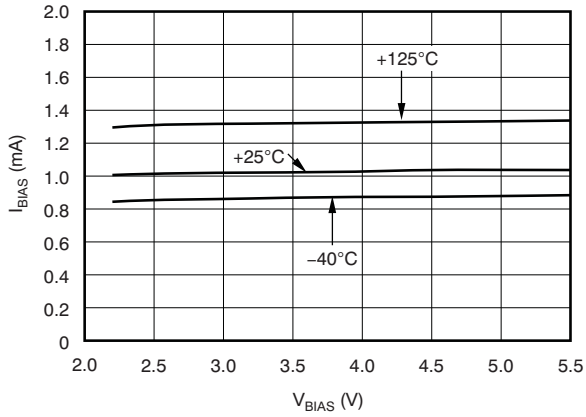

Figure 13. BIAS Pin Current vs V_{BIAS} and Temperature (T_J)

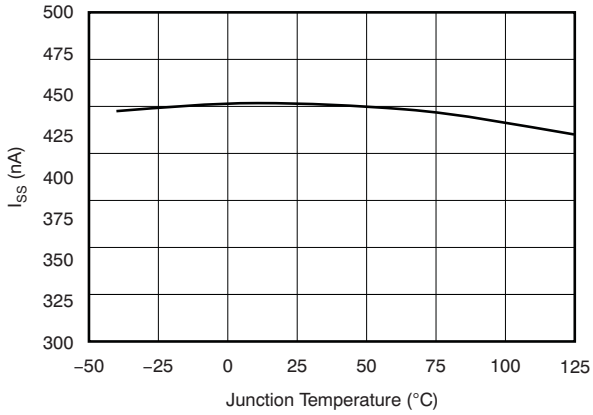

Figure 14. Soft-Start Charging Current (I_{SS}) vs Temperature (T_J)

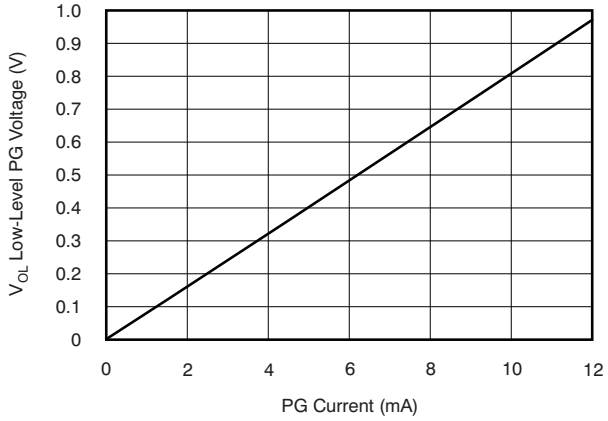

Figure 15. Low-Level PG Voltage vs Current

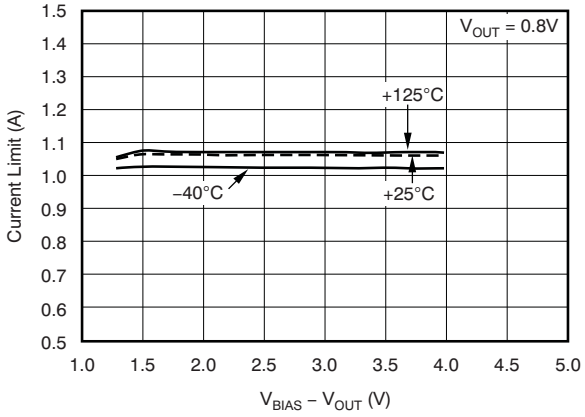

Figure 16. Current Limit vs ($V_{BIAS} - V_{OUT}$)

6.7 Typical Characteristics: $V_{EN} = V_{IN} = 1.8$ V, $V_{OUT} = 1.5$ V

At $T_J = 25°C$, $V_{IN} = V_{OUT(TYP)} + 0.3$ V, $V_{BIAS} = 5$ V, $I_{OUT} = 50$ mA, $V_{EN} = V_{IN} = 1.8$ V, $V_{OUT} = 1.5$ V, $C_{IN} = 1$ µF, $C_{BIAS} = 4.7$ µF, and $C_{OUT} = 10$ µF, unless otherwise noted.

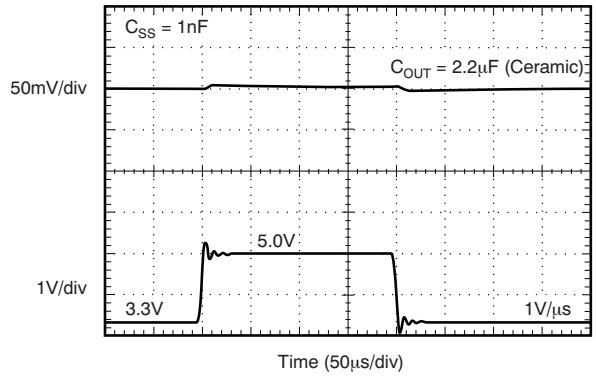

Figure 17. V_{BIAS} Line Transient

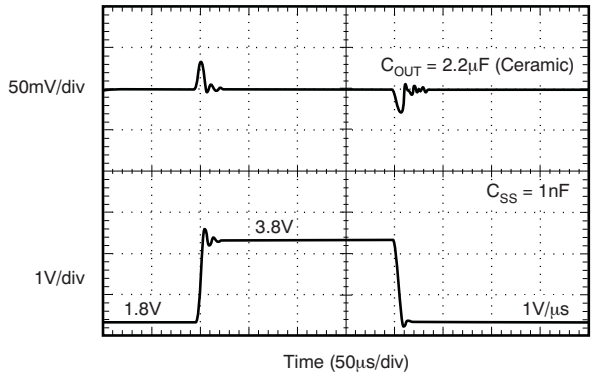

Figure 18. V_{IN} Line Transient

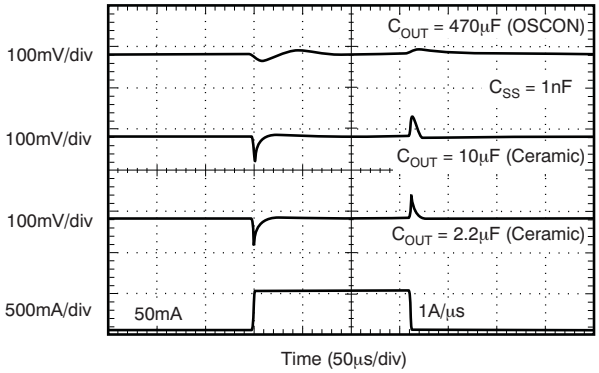

Figure 19. Output Load Transient Response

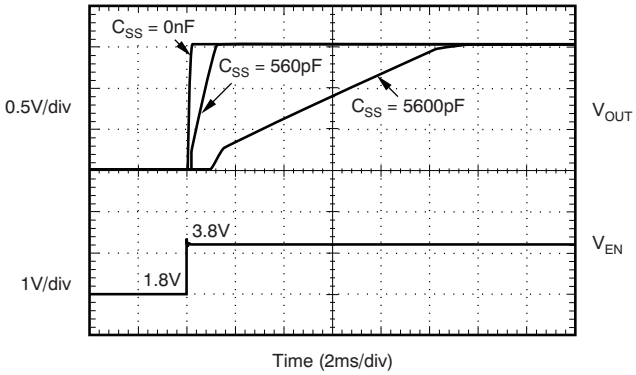

Figure 20. Turnon Response

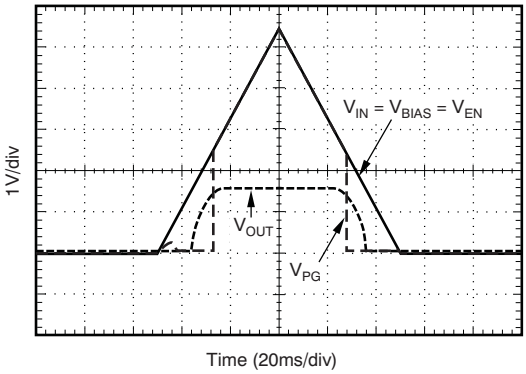

Figure 21. Power Up and Power Down

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7 Detailed Description

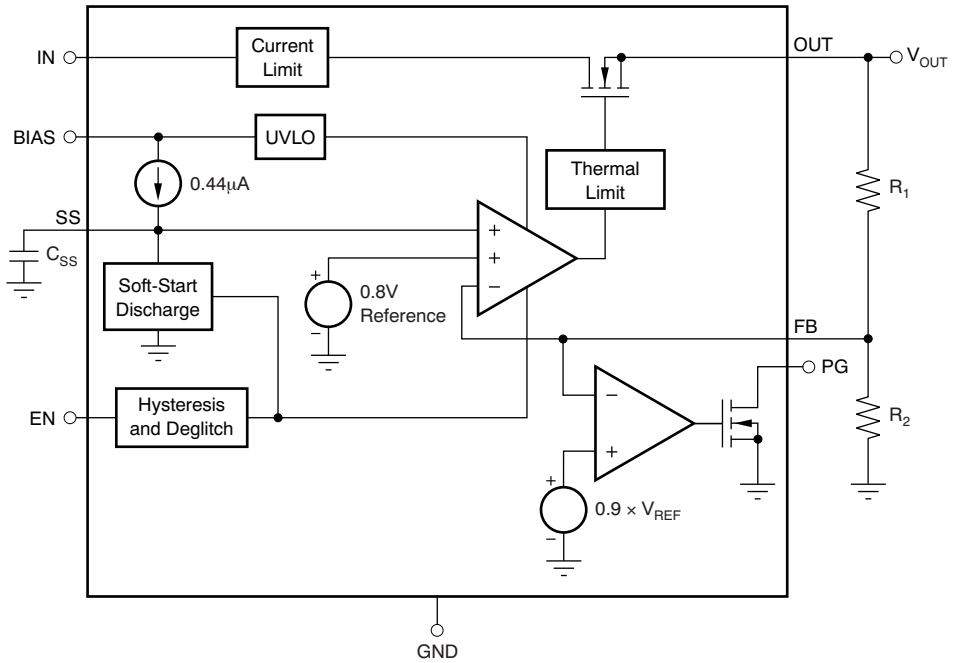
7.1 Overview

The TPS74701 belongs to a family of low-dropout regulators that feature soft-start capability. These regulators use a low current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

The use of an NMOS-pass FET offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS74701 to be stable with any capacitor type of value 2.2 µF or greater. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS74701 features a programmable voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents that may be caused by large capacitive loads. A power good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low VIN and VOUT capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often present in processor-intensive systems.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Programmable Soft-Start

The TPS74701 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor (C_{SS}). This feature is important for many applications because it eliminates power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

To achieve a linear and monotonic soft-start, the TPS74701 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current (I_{SS}), soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}), and can be calculated using Equation 1:

Feature Description (continued)

$$t_{SS} = \frac{(V_{REF} \times C_{SS})}{I_{SS}} \quad (1)$$

If large output capacitors are used, the device current limit (I_{CL}) and the output capacitor may set the start-up time. In this case, the start-up time is given by Equation 2:

$$t_{SSCL} = \frac{(V_{OUT(NOM)} \times C_{OUT})}{I_{CL(MIN)}}$$

where

- $V_{OUT(NOM)}$ is the nominal output voltage
- C_{OUT} is the output capacitance
- $I_{CL(MIN)}$ is the minimum current limit for the device (2)

In applications where monotonic start-up is required, the soft-start time given by Equation 1 should be set greater than Equation 2.

The maximum recommended soft-start capacitor is 0.015 µF. Larger soft-start capacitors can be used, and they do not damage the device; however, the soft-start capacitor discharge circuit may not be able to fully discharge the soft-start capacitor when enabled.

Soft-start capacitors larger than 0.015 µF could be a problem in applications where it is necessary to rapidly pulse the enable pin and still require the device to soft-start from ground. C_{SS} must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. See Table 3 for suggested soft-start capacitor values.

7.3.2 Enable and Shutdown

The enable (EN) pin is active high and is compatible with standard digital signaling levels. V_{EN} below 0.4 V turns the regulator off, while V_{EN} above 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slowly ramping analog signals. This configuration allows the TPS74701 to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50 mV of hysteresis and a deglitch circuit to help avoid on-off cycling as a result of small glitches in the V_{EN} signal.

The enable threshold is typically 0.8 V and varies with temperature and process variations. Temperature variation is approximately –1 mV/°C; process variation accounts for most of the rest of the variation to the 0.4-V and 1.1-V limits. If precise turnon timing is required, a fast rise-time signal must be used to enable the TPS74701.

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, it should be connected as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

7.3.3 Power Good

The power good (PG) pin is an open-drain output and can be connected to any 5.5 V or lower rail through an external pullup resistor. This pin requires at least 1.1 V on V_{BIAS} to have a valid output. The PG output is high-impedance when V_{OUT} is greater than $V_{IT} + V_{HYS}$. If V_{OUT} drops below V_{IT} or if V_{BIAS} drops below 1.9 V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of the PG pin sink current is up to 1 mA, so the pullup resistor for PG should be in the range of 10 kΩ to 1 MΩ. If output voltage monitoring is not needed, the PG pin can be left floating.

7.3.4 Internal Current Limit

The TPS74701 features a factory-trimmed, accurate current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 1 A and maintain regulation. The current limit responds in about 10 µs to reduce the current during a short-circuit fault.

The internal current limit protection circuitry of the TPS74701 is designed to protect against overload conditions. It is not intended to allow operation above the rated current of the device. Continuously running the TPS74701 above the rated current degrades device reliability.

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Feature Description (continued)

7.3.5 Thermal Shutdown

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 40°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS74701 is designed to protect against overload conditions. It is not intended to replace proper heatsinking. Continuously running the TPS74701 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage and bias voltage are both at least at the respective minimum specifications.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{EN}	V_{BIAS}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}(V_{IN})$	$V_{EN} > V_{EN, HI}$	$V_{BIAS} \geq V_{OUT} + 1.39$ V	$I_{OUT} < I_{CL}$	$T_J < 125$°C
Dropout mode	$V_{IN} < V_{OUT(nom)} + V_{DO}(V_{IN})$	$V_{EN} > V_{EN, HI}$	$V_{BIAS} < V_{OUT} + 1.39$ V	—	$T_J < 125$°C
Disabled mode (any true condition disables the device)	$V_{IN} < V_{IN(min)}$	$V_{EN} < V_{EN, LO}$	$V_{BIAS} < V_{BIAS(min)}$	—	$T_J > 165$°C

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 25. See Table 2 for sample resistor values of common output voltages. To achieve the maximum accuracy specifications, R_2 should be less than or equal to 4.99 kΩ.

Table 2. Standard 1% Resistor Values for Programming the Output Voltage(1)

R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

(1) $V_{OUT} = 0.8 \times (1 + R_1/R_2)$.

Table 3. Standard Capacitor Values for Programming the Soft-Start Time(1)

C_{SS}	SOFT-START TIME
Open	0.1 ms
270 pF	0.5 ms
560 pF	1 ms
2.7 nF	5 ms
5.6 nF	10 ms
0.01 µF	18 ms

$$t_{SS}(s) = \frac{V_{REF} \times C_{SS}}{I_{SS}} = \frac{0.8V \times C_{SS}(F)}{0.44\mu A} \quad (1)$$

where $t_{SS}(s)$ = soft-start time in seconds.

8.1.1 Input, Output, and Bias Capacitor Requirements

The device is designed to be stable for all available types and values of output capacitors greater than or equal to 2.2 µF. The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} and V_{BIAS} is 1 µF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7 µF. Good quality, low ESR capacitors should be used on the input; ceramic X5R and X7R capacitors are preferred. These capacitors should be placed as close the pins as possible for optimum performance.

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8.1.2 Transient Response

The TPS74701 was designed to have excellent transient response for most applications with a small amount of output capacitance. In some cases, the transient response may be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300 mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance would do. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient event; see Figure 19 in the *Typical Characteristics: V_{EN} = V_{IN}* section. Because the TPS74701 is stable with output capacitors as low as 2.2 µF, many applications may then need very little capacitance at the LDO output. For these applications, local bypass capacitance for the powered device may be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive, high-value capacitors at the LDO output.

8.1.3 Dropout Voltage

The TPS74701 offers very low dropout performance, making it well-suited for high-current, low V_{IN}/low V_{OUT} applications. The low dropout of the TPS74701 allows the device to be used in place of a DC-DC converter and still achieve good efficiency. This feature provides designers with the power architecture for their applications to achieve the smallest, simplest, and lowest cost solution.

There are two different specifications for dropout voltage with the TPS74701. The first specification (shown in Figure 22) is referred to as *V_{IN} Dropout* and is used when an external bias voltage is applied to achieve low dropout. This specification assumes that V_{BIAS} is at least 1.39 V [(2)] above V_{OUT}, which is the case for V_{BIAS} when powered by a 3.3-V rail with 5% tolerance and with V_{OUT} = 1.5 V. If V_{BIAS} is higher than V_{OUT} +1.39 V[(1)], V_{IN} dropout is less than specified.

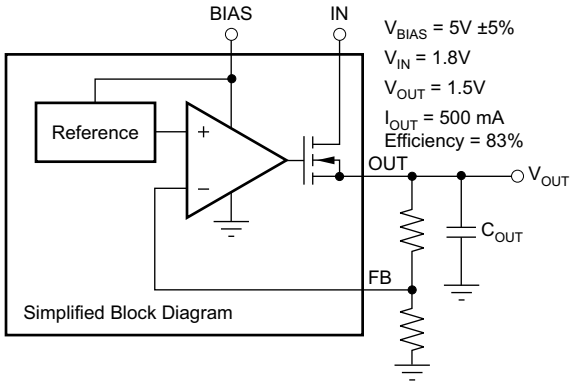

Figure 22. Typical Application of the TPS74701 Using an Auxiliary Bias Rail

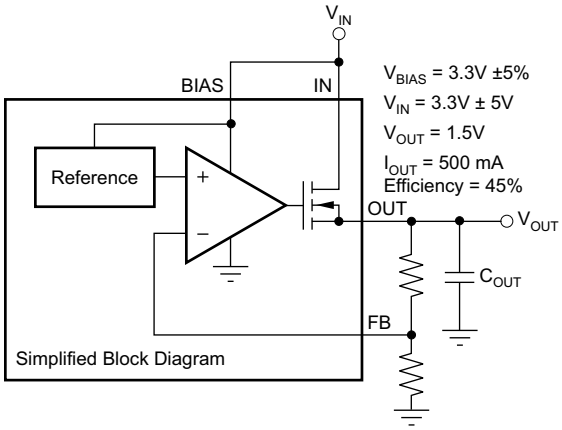

Figure 23. Typical Application of the TPS74701 Without an Auxiliary Bias Rail

(2) 1.62 V is a test condition of this device and can be adjusted by referring to Figure 6.

The second specification (shown in Figure 23) is referred to as *V_{BIAS} Dropout* and applies to applications where IN and BIAS are tied together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass FET; therefore, V_{BIAS} must be 1.39-V above V_{OUT}. Because of this usage, IN and BIAS tied together easily consume huge power. Pay attention not to exceed the power rating of the IC package.

8.1.4 Sequencing Requirements

V_{IN}, V_{BIAS}, and V_{EN} can be sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Connecting EN to IN is acceptable for most applications, as long as V_{IN} is greater than 1.1 V and the ramp rate of V_{IN} and V_{BIAS} is faster than the set soft-start ramp rate. If the ramp rate of the input sources is slower than the set soft-start time, the output tracks the slower supply minus the dropout voltage until it reaches the set output voltage. If EN is connected to BIAS, the device soft-starts as programmed, provided that V_{IN} is present before V_{BIAS}. If V_{BIAS} and V_{EN} are present before V_{IN} is applied and the set soft-start time has expired, then V_{OUT} tracks V_{IN}. If the soft-start time has not expired, the output tracks V_{IN} until V_{OUT} reaches the value set by the charging soft-start capacitor. Figure 24 shows the use of an RC-delay circuit to hold off V_{EN} until V_{BIAS} has ramped. This technique can also be used to drive EN from V_{IN}. An external control signal can also be used to enable the device after V_{IN} and V_{BIAS} are present.

NOTE

When V_{BIAS} and V_{EN} are present and V_{IN} is not supplied, this device outputs approximately 50 µA of current from OUT. Although this condition does not cause any damage to the device, the output current may charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10 kΩ.

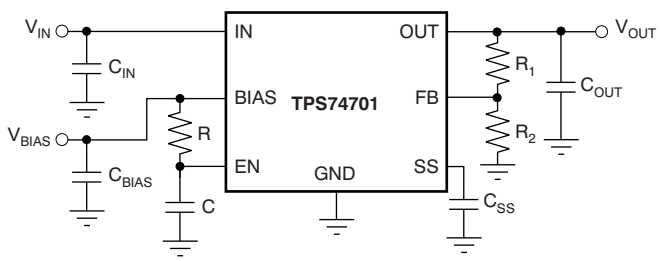

Figure 24. Soft-Start Delay Using an RC Circuit to Enable the Device

8.1.5 Output Noise

The TPS74701 provides low-output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 0.001-µF soft-start capacitor, the output noise is reduced by half and is typically 30 μV_{RMS} for a 1.2-V output (10 Hz to 100 kHz). Further increasing C_{SS} has little effect on noise. Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. The RMS noise with a 0.001-µF soft-start capacitor is given in Equation 3:

$$V_N(\mu V_{RMS}) = 25\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \tag{3}$$

The low-output noise of the TPS74701 makes it a good choice for powering transceivers, PLLs, or other noise-sensitive circuitry.

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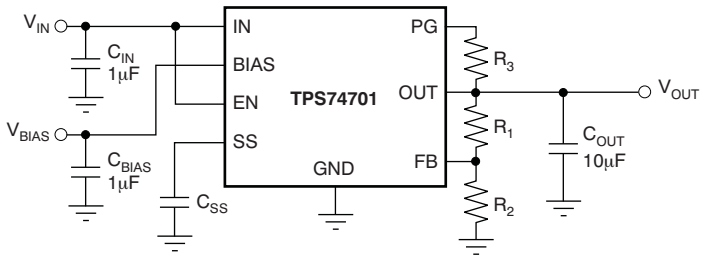
8.2 Typical Application

Figure 25 illustrates the typical application circuit for the TPS74701 adjustable output device.



$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Figure 25. Typical Application Circuit for the TPS74701 (Adjustable)

8.2.1 Design Requirements

Table 4 shows the design parameters for this application.

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VIN	1.8 V ± 10%
VBIAS	3.3 V ±10%
VOUT	1.5 V ± 3%
IOUT	500 mA
Start-up time	< 2 ms

8.2.2 Detailed Design Procedure

1. Select R1 and R2 based on the required output voltage. Table 2 gives example calculations for many common output voltages.
2. Select C_{SS} to be the highest capacitance while still achieving the desired start-up time. Table 3 gives examples of this calculation.
3. Select a minimum of a 2.2-µF ceramic output capacitor. Increased output capacitance will help the output load transient response. Figure 27 gives examples of the load transient response with different output capacitor values and types.

8.2.3 Application Curves

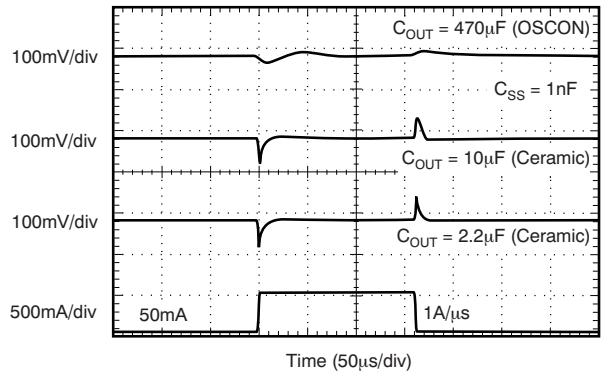


Figure 26. Output Load Transient Response

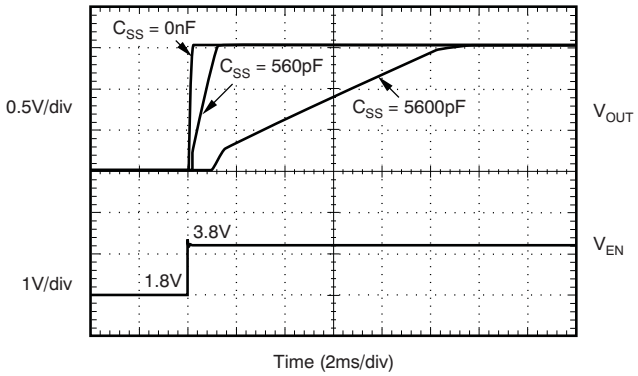


Figure 27. Turnon Response

9 Power Supply Recommendations

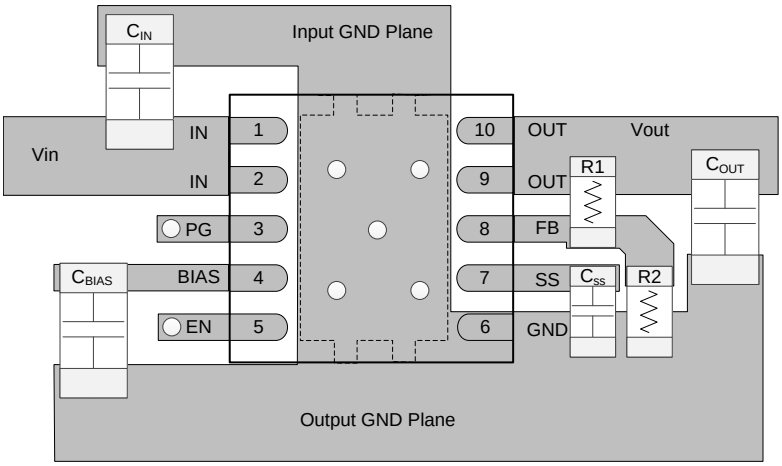
The TPS74701 is designed to operate from an input voltage up to 5.5 V, provided the bias rail is at least 1.39-V higher than the input supply and dropout requirements are met. The bias rail and the input supply should both provide adequate headroom and current for the device to operate normally. Connect a low-output impedance power supply directly to the IN pin of the TPS74701. This supply must have at least 1 µF of capacitance near the IN pin for optimal performance. A supply with similar requirements must also be connected directly to the bias rail with a separate 1-µF or larger capacitor. If the IN pin is tied to the bias pin, a minimum 4.7 µF of capacitance is needed for performance. To increase the overall PSRR of the solution at higher frequencies, use a pi-filter or ferrite bead before the input capacitor.

10 Layout

10.1 Layout Guidelines

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage droop on the input of the device during load transients, connect the capacitance on IN, OUT and BIAS as close as possible to the device. If BIAS is connected to IN, connect BIAS as close to the input supply as possible. This connection minimizes the voltage droop on BIAS during transient conditions and can improve the turnon response.

10.2 Layout Example



Note: C_{IN}, C_{OUT}, and C_{BIAS} are 0603 case size capacitors, while C_{SS}, R_1, and R_2 are 0402 case size.

Figure 28. TPS547 Layout Recommendation

10.3 Power Dissipation

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage drop on the input of the device during load transients, the capacitance on IN and BIAS should be connected as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can therefore improve stability. To achieve optimal transient performance and accuracy, the top side of R_1 in Figure 25 should be connected as close as possible to the load. If BIAS is connected to IN, TI recommends connecting BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage drop on BIAS during transient conditions and can improve the turnon response.

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoiding thermal shutdown and ensuring reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 4:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

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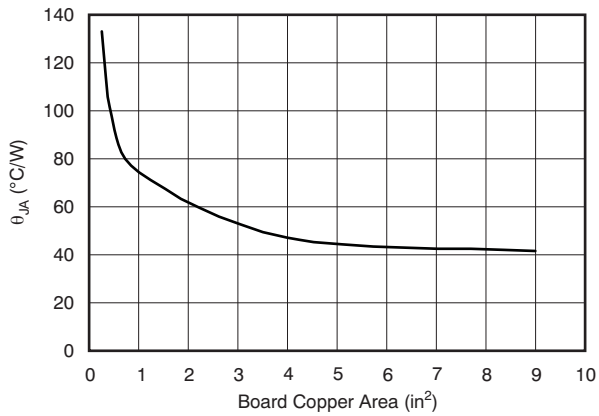
Power Dissipation (continued)

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the SON (DRC) package, the primary conduction path for heat is through the exposed pad to the printed-circuit-board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 5:

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D} \tag{5}$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 29.



Note: θ_{JA} value at board size of 9in^2 (that is, 3 inches × 3 inches) is a JEDEC standard.

Figure 29. θ_{JA} vs Board Size

Figure 29 shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

NOTE

When the device is mounted on an application PCB, TI strongly recommends using Ψ_{JT} and Ψ_{JB}, as explained in the section.

10.4 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 6). For backwards compatibility, an older $\theta_{JC,Top}$ parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D$$

where

- P_D is the power dissipation shown by Equation 5.
- T_T is the temperature at the center-top of the IC package.
- T_B is the PCB temperature measured 1mm away from the IC package *on the PCB surface* (as Figure 31 shows). (6)

Estimating Junction Temperature (continued)

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com.

By looking at Figure 30, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with Equation 6 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

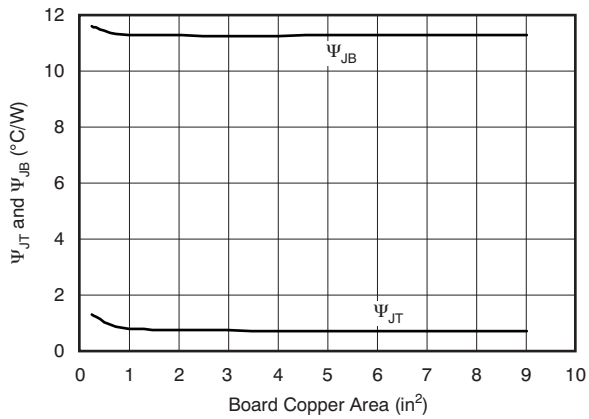


Figure 30. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see application report SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com. For further information, see application report SPRA953, *Semiconductor and IC Package Thermal Metrics*, also available on the TI website.

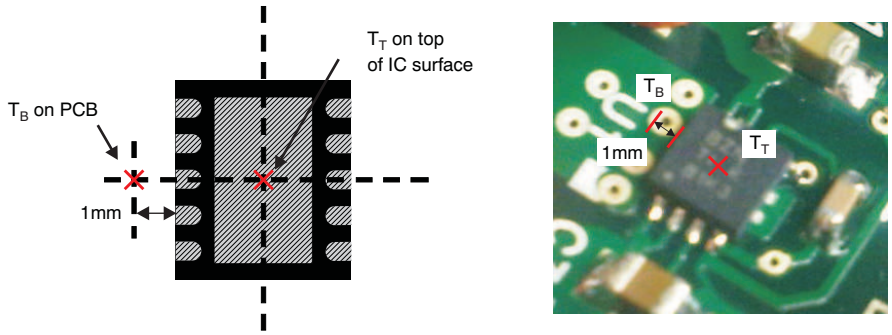


Figure 31. Measuring Points for T_T and T_B

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS74701. The TPS74701EVM-177 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for TPS74701 is available through the product folders under *Simulation Models*.

11.1.2 Device Nomenclature

Table 5. Device Nomenclature(1)

PRODUCT	V_{OUT} (2)
TPS747**xx yyy z**	**xx** is nominal output voltage (for example, 12 = 1.2 V, 15 = 1.5 V, 01 = Adjustable).(3) **YYY** is the package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Fixed output voltages from 0.8 V to 3.3 V are available; minimum order quantities may apply. Contact factory for details and availability.
(3) For fixed 0.8-V operation, tie FB to OUT.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Using New Thermal Metrics*, SBVA025
- *Semiconductor and IC Package Thermal Metrics*, SPRA953

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS74701DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEG	Samples
TPS74701DRCRG4	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEG	Samples
TPS74701DRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEG	Samples
TPS74701DRCTG4	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CEG	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS74701 :

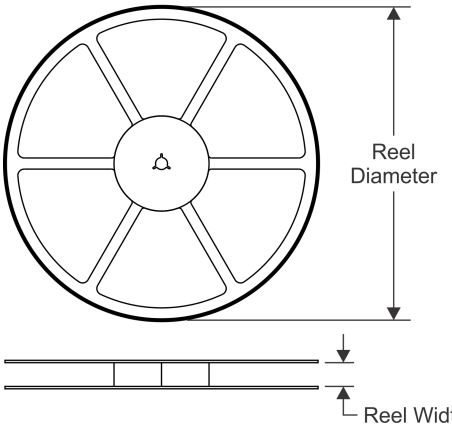
- Automotive: TPS74701-Q1

NOTE: Qualified Version Definitions:

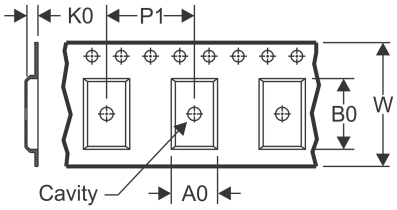
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

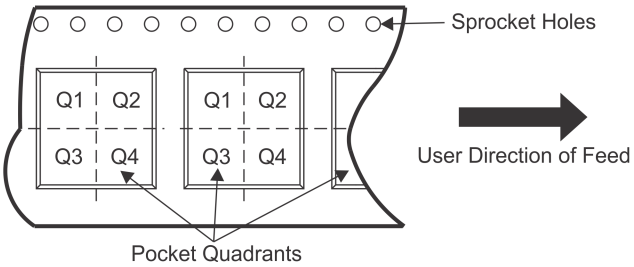


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

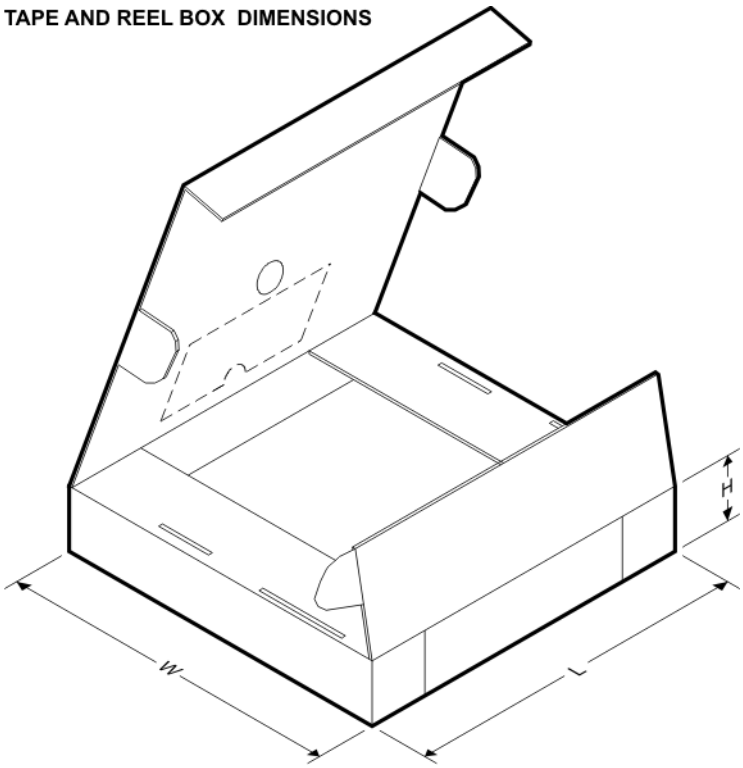
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74701DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74701DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74701DRCR	VSON	DRC	10	3000	853.0	449.0	35.0
TPS74701DRCT	VSON	DRC	10	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

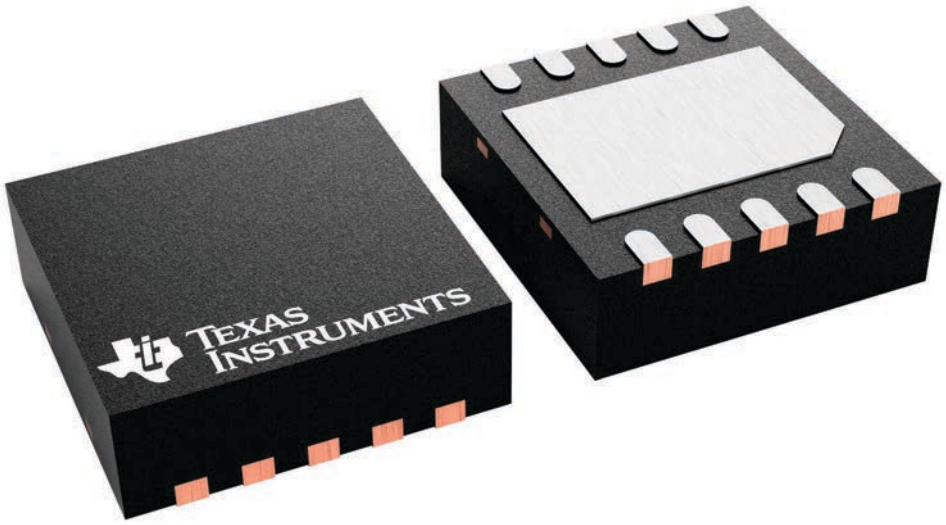
DRC 10

VSON - 1 mm max height

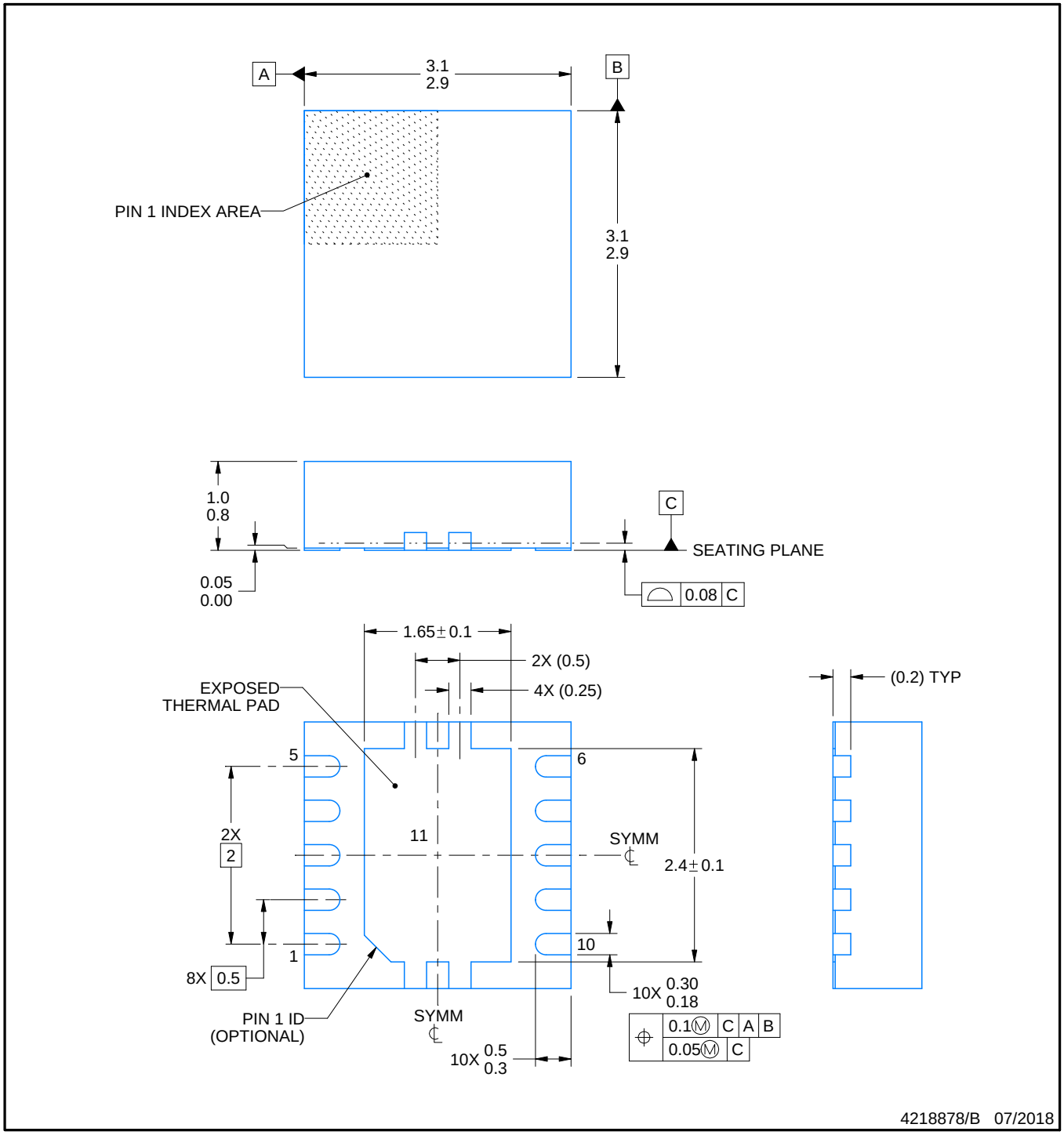
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

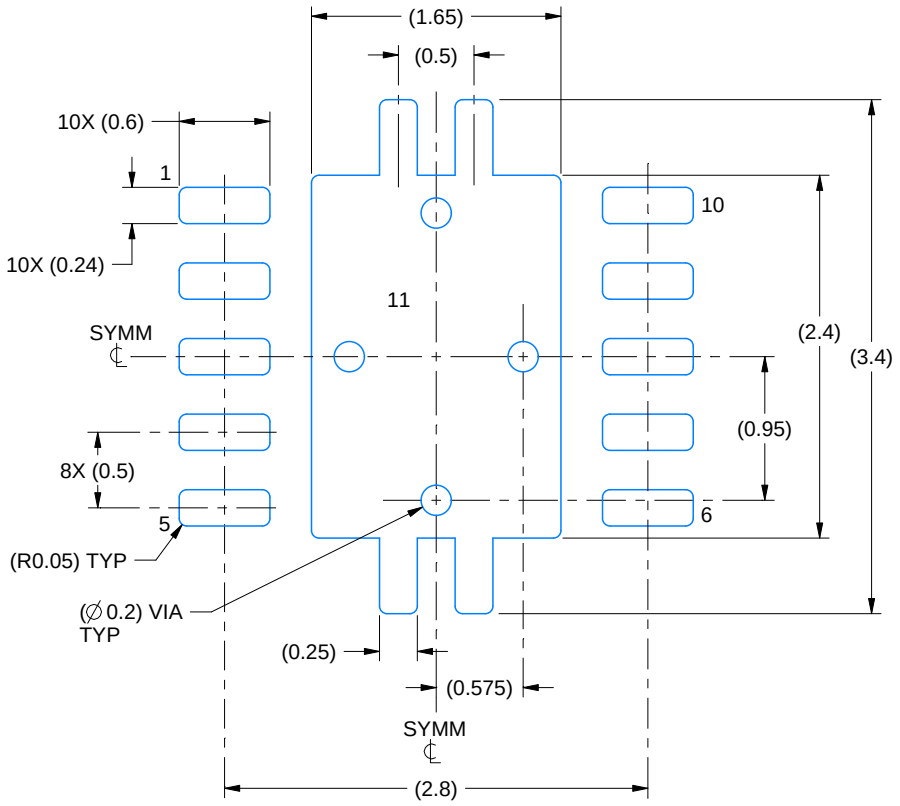


4226193/A

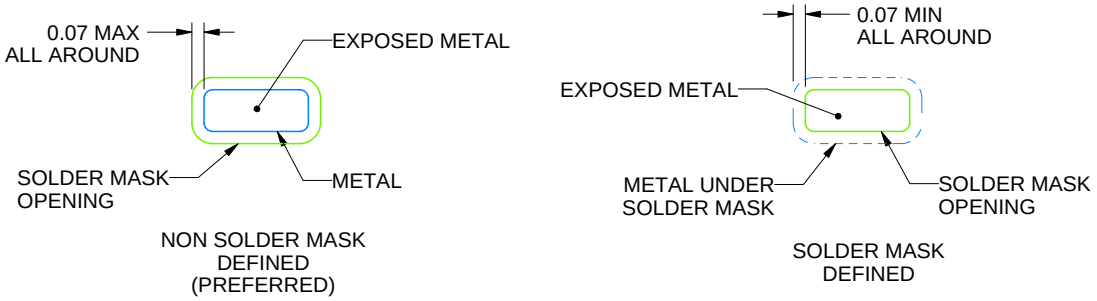


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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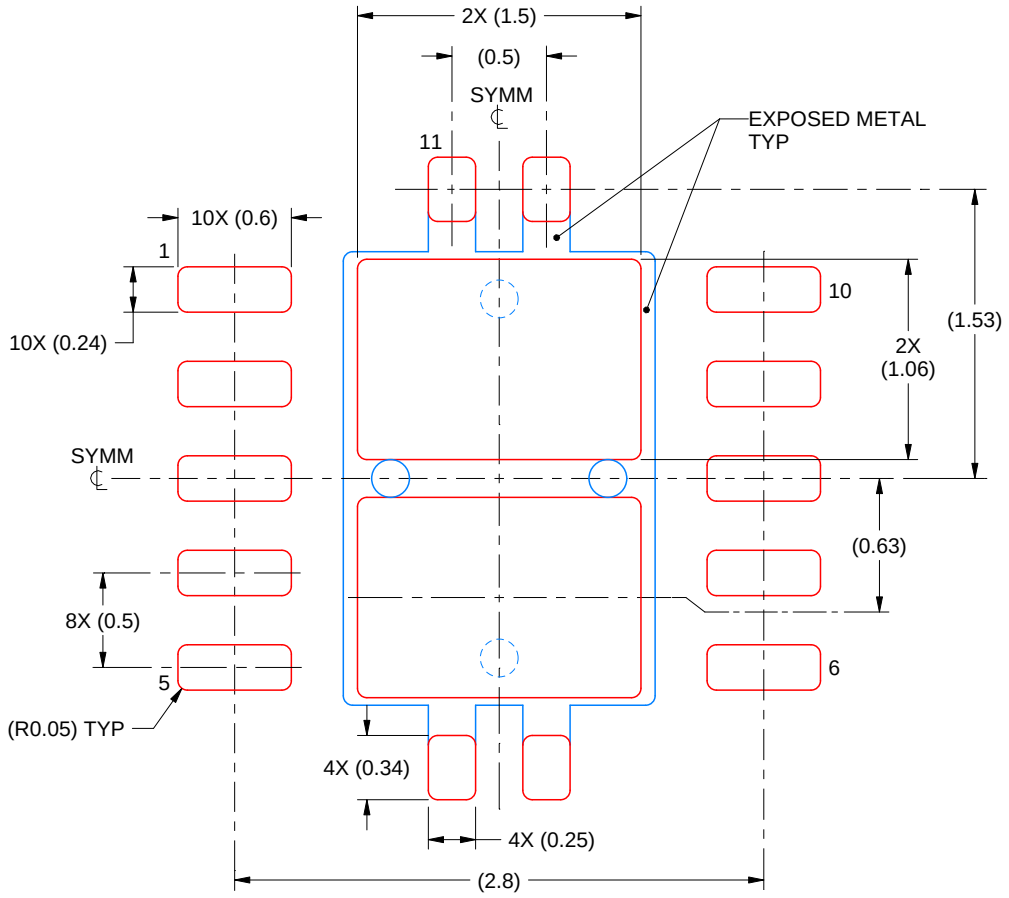
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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