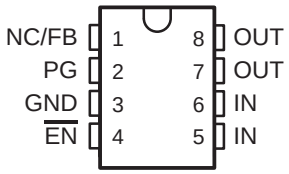
TPS76515, TPS76518, TPS76525, TPS76527 TPS76528, TPS76530, TPS76533, TPS76550, TPS76501 ULTRA-LOW QUIESCIENT CURRENT 150-mA LOW-DROPOUT VOLTAGE REGULATORS

SLVS236 – AUGUST 1999

- **150-mA Low-Dropout Voltage Regulator**
- **Available in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, 5.0-V Fixed Output and Adjustable Versions**
- **Dropout Voltage to 85 mV (Typ) at 150 mA (TPS76550)**
- **Ultra-Low 35-μA Typical Quiescent Current**
- **3% Tolerance Over Specified Conditions for Fixed-Output Versions**
- **Open Drain Power Good**
- **8-Pin SOIC Package**
- **Thermal Shutdown Protection**

D PACKAGE
(TOP VIEW)

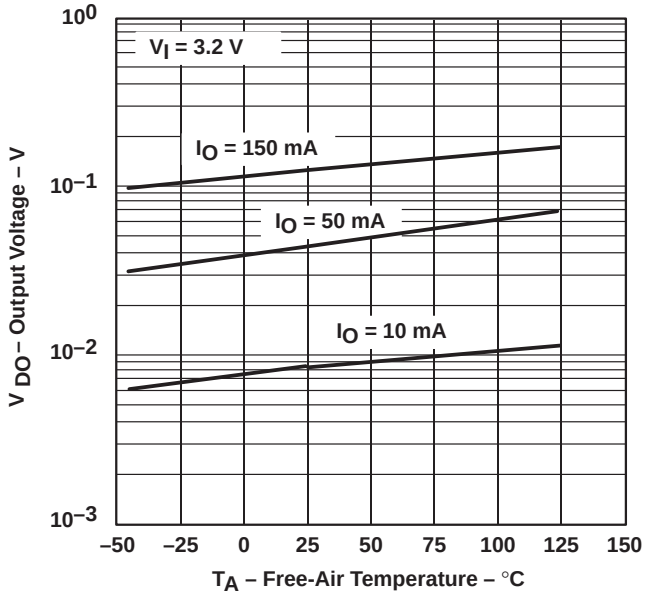


description

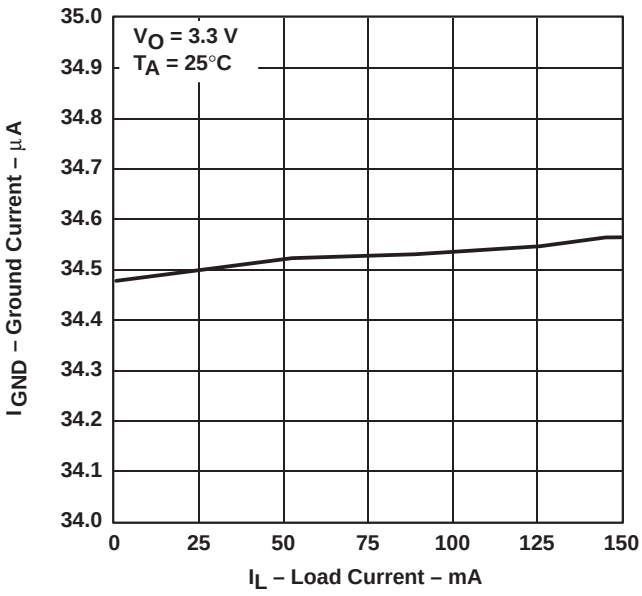
This device is designed to have an ultra-low quiescent current and be stable with a 4.7-μF capacitor. This combination provides high performance at a reasonable cost.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 85 mV at an output current of 150 mA for the TPS76550) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 35 μA over the full range of output current, 0 mA to 150 mA). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{EN}$ (enable) shuts down the regulator, reducing the quiescent current to less than 1 μA (typ).

TPS76533
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE



TPS76533
GROUND CURRENT
vs
LOAD CURRENT



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description (continued)

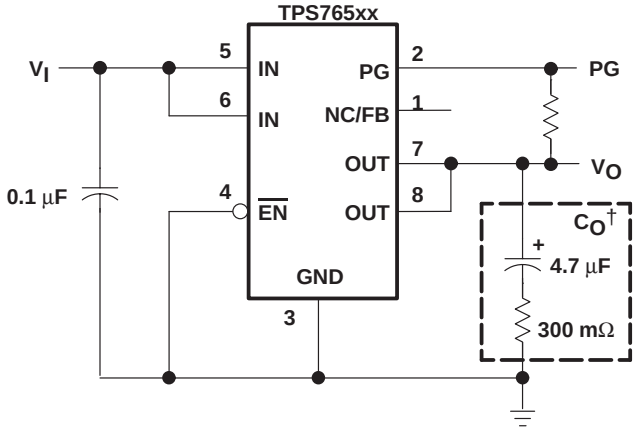
Power good (PG) is an active high output, which can be used to implement a power-on reset or a low-battery indicator.

The TPS765xx is offered in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V and 5.0-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.25 V to 5.5 V). Output voltage tolerance is specified as a maximum of 3% over line, load, and temperature ranges. The TPS765xx family is available in 8 pin SOIC package.

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (V)	PACKAGED DEVICES
	TYP	SOIC (D)
–40°C to 125°C	5.0	TPS76550D
	3.3	TPS76533D
	3.0	TPS76530D
	2.8	TPS76528D
	2.7	TPS76527D
	2.5	TPS76525D
	1.8	TPS76518D
	1.5	TPS76515D
	Adjustable 1.25 V to 5.5 V	TPS76501D

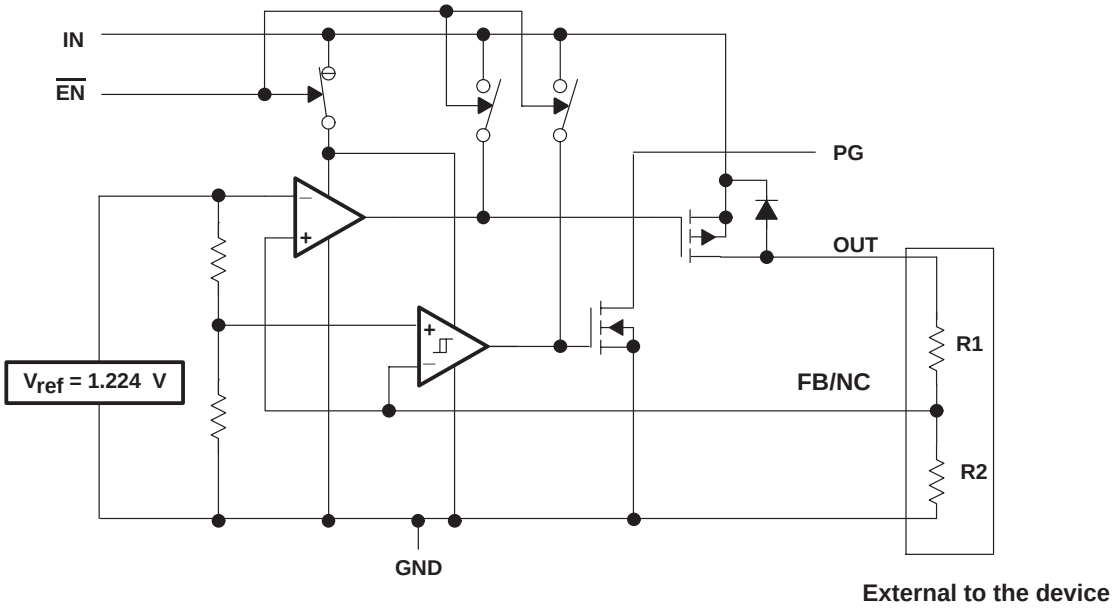
The TPS76501 is programmable using an external resistor divider (see application information). The D package is available taped and reeled. Add an R suffix to the device type (e.g., TPS76501DR).



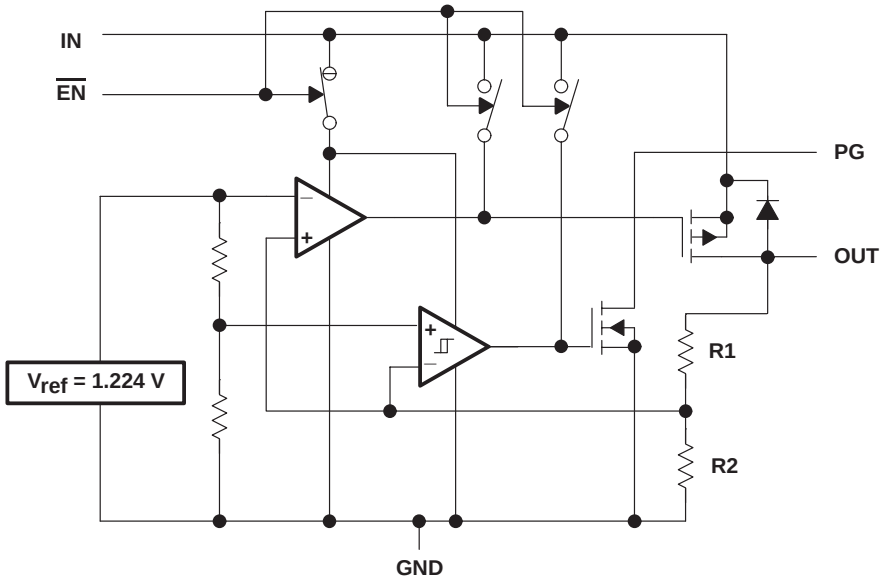
† See application information section for capacitor selection details.

Figure 1. Typical Application Configuration for Fixed Output Options

functional block diagram—adjustable version



functional block diagram—fixed-voltage version



Terminal Functions – SOIC Package

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{EN}$	4	I	Enable input
FB/NC	1	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
IN	5	I	Input voltage
IN	6	I	Input voltage
OUT	7	O	Regulated output voltage
OUT	8	O	Regulated output voltage
PG	2	O	PG output

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_I . . . . . –0.3 V to 13.5 V
Voltage range at $\overline{EN}$ . . . . . –0.3 V to 16.5 V
Maximum PG voltage . . . . . 16.5 V
Peak output current . . . . . Internally limited
Continuous total power dissipation . . . . . See dissipation rating tables
Output voltage, V_O (OUT, FB) . . . . . 7 V
Operating virtual junction temperature range, T_J . . . . . –40°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
ESD rating, HBM . . . . . 2 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	0	568 mW	5.68 mW/°C	312 mW	227 mW
	250	904 mW	9.04 mW/°C	497 mW	361 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I☆	2.7	10	V
Output voltage range, V_O	1.2	5.5	V
Output current, I_O (Note 1)	0	150	mA
Operating virtual junction temperature, T_J (Note 1)	–40	125	°C

☆ To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.
NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

electrical characteristics over recommended operating free-air temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 10$ μA, $\overline{EN} = 0$ V, $C_O = 4.7$ μF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage (10 μA to 150 mA load) (see Note 2)	TPS76501	5.5 V ≥ V_O ≥ 1.25 V,	T_J = 25°C		V_O		V
		5.5 V ≥ V_O ≥ 1.25 V,	T_J = –40°C to 125°C	0.97V_O		1.03V_O	
	TPS76515	T_J = 25°C,	2.7 V < V_{IN} < 10 V		1.5		
		T_J = –40°C to 125°C,	2.7 V < V_{IN} < 10 V	1.455		1.545	
	TPS76518	T_J = 25°C,	2.8 V < V_{IN} < 10 V		1.8		
		T_J = –40°C to 125°C,	2.8 V < V_{IN} < 10 V	1.746		1.854	
	TPS76525	T_J = 25°C,	3.5 V < V_{IN} < 10 V		2.5		
		T_J = –40°C to 125°C,	3.5 V < V_{IN} < 10 V	2.425		2.575	
	TPS76527	T_J = 25°C,	3.7 V < V_{IN} < 10 V		2.7		
		T_J = –40°C to 125°C,	3.7 V < V_{IN} < 10 V	2.619		2.781	
	TPS76528	T_J = 25°C,	3.8 V < V_{IN} < 10 V		2.8		
		T_J = –40°C to 125°C,	3.8 V < V_{IN} < 10 V	2.716		2.884	
	TPS76530	T_J = 25°C,	4.0 V < V_{IN} < 10 V		3.0		
		T_J = –40°C to 125°C,	4.0 V < V_{IN} < 10 V	2.910		3.090	
	TPS76533	T_J = 25°C,	4.3 V < V_{IN} < 10 V		3.3		
		T_J = –40°C to 125°C,	4.3 V < V_{IN} < 10 V	3.201		3.399	
	TPS76550	T_J = 25°C,	6.0 V < V_{IN} < 10 V		5.0		
		T_J = –40°C to 125°C,	6.0 V < V_{IN} < 10 V	4.850		5.150	
Quiescent current (GND current) $\overline{EN}$ = 0V, (see Note 2)		10 μA < I_O < 150 mA,	T_J = 25°C		35		μA
		I_O = 150 mA,	T_J = –40°C to 125°C			50	
Output voltage line regulation ($\Delta V_O/V_O$) (see Notes 2 and 3)		V_O + 1 V < V_I ≤ 10 V,	T_J = 25°C		0.01		%/V
Load regulation		I_O = 10 μA to 150 mA			0.3%		
Output noise voltage		BW = 300 Hz to 50 kHz, C_O = 4.7 μF,	T_J = 25°C		200		μVrms
Output current Limit		V_O = 0 V			0.8	1.2	A
Thermal shutdown junction temperature					150		°C
Standby current		$\overline{EN}$ = V_I,	T_J = 25°C, 2.7 V < V_I < 10 V		1		μA
		$\overline{EN}$ = V_I,	T_J = –40°C to 125°C 2.7 V < V_I < 10 V			10	μA
FB input current	TPS76501	FB = 1.5 V			2		nA
High level enable input voltage				2.0			V
Low level enable input voltage						0.8	V
Power supply ripple rejection (see Note 2)		f = 1 kHz, I_O = 10 μA,	C_O = 4.7 μF, T_J = 25°C		63		dB
PG	Minimum input voltage for valid PG	$I_{O(PG)}$ = 300μA			1.1		V
	Trip threshold voltage	V_O decreasing		92		98	%V_O
	Hysteresis voltage	Measured at V_O			0.5		%V_O
	Output low voltage	V_I = 2.7 V,	$I_{O(PG)}$ = 1mA		0.15	0.4	V
	Leakage current	$V_{(PG)}$ = 5 V				1	μA
Input current (EN)		$\overline{EN}$ = 0 V		–1	0	1	μA
		$\overline{EN}$ = V_I		–1		1	

NOTE: 2. Minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. Maximum IN voltage 10 V.

electrical characteristics over recommended operating free-air temperature range, $V_i = V_{O(typ)} + 1$ V, $I_O = 10$ μA, $\overline{EN} = 0$ V, $C_O = 4.7$ μF (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dropout voltage (See Note 4)	TPS76528	I_O = 150 mA,	T_J = 25°C		190		mV
		I_O = 150 mA,	T_J = –40°C to 125°C			330	
	TPS76530	I_O = 150 mA,	T_J = 25°C		160		
		I_O = 150 mA,	T_J = –40°C to 125°C			280	
	TPS76533	I_O = 150 mA,	T_J = 25°C		140		
		I_O = 150 mA,	T_J = –40°C to 125°C			240	
	TPS76550	I_O = 150 mA,	T_J = 25°C		85		
		I_O = 150 mA,	T_J = –40°C to 125°C			150	

NOTES: 3. If $V_O \le 1.8$ V then $V_{imin} = 2.7$ V, $V_{imax} = 10$ V:

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O\left(V_{imax} - 2.7\ \text{V}\right)}{100} \times 1000$$

If $V_O \ge 2.5$ V then $V_{imin} = V_O + 1$ V, $V_{imax} = 10$ V:

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O\left(V_{imax} - \left(V_O + 1\ \text{V}\right)\right)}{100} \times 1000$$

4. IN voltage equals V_O(Typ) – 100 mV; TPS76501 output voltage set to 3.3 V nominal with external resistor divider. TPS76515, TPS76518, TPS76525, and TPS76527 dropout voltage limited by input voltage range limitations (i.e., TPS76530 input voltage needs to drop to 2.9 V for purpose of this test).

Table of Graphs

		FIGURE
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Output impedance	vs Frequency	12
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Line transient response		15, 17
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Output voltage	vs Time	19
Dropout voltage	vs Input voltage	20
Equivalent series resistance (ESR)	vs Output current	21 – 24
Equivalent series resistance (ESR)	vs Added ceramic capacitance	25, 26

TYPICAL CHARACTERISTICS

TPS76533
OUTPUT VOLTAGE
vs
LOAD CURRENT

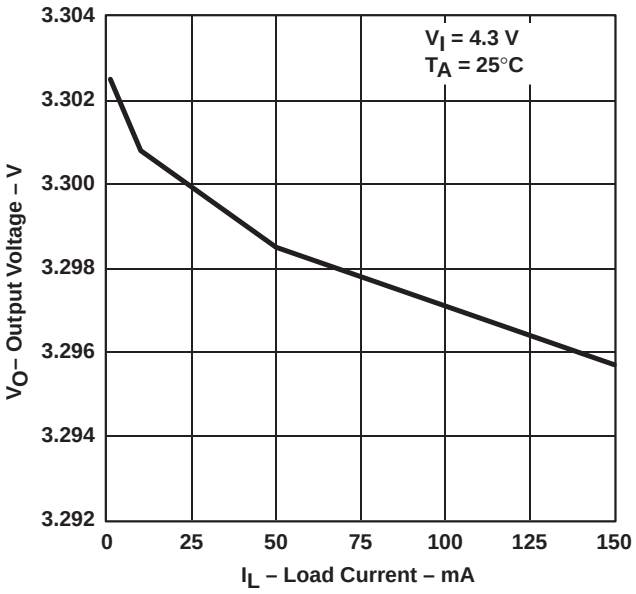


Figure 2

TPS76515
OUTPUT VOLTAGE
vs
LOAD CURRENT

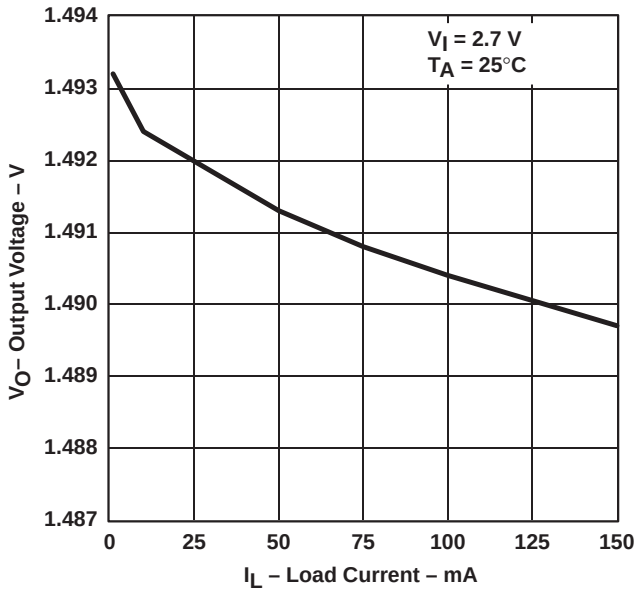


Figure 3

TPS76533
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

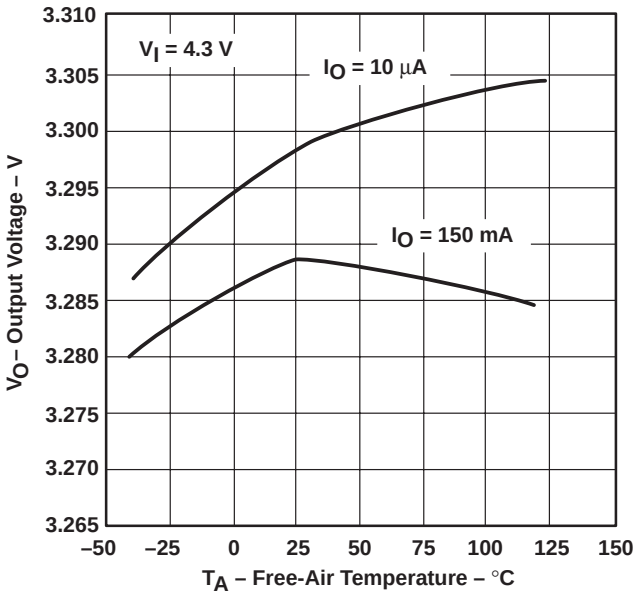


Figure 4

TPS76515
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

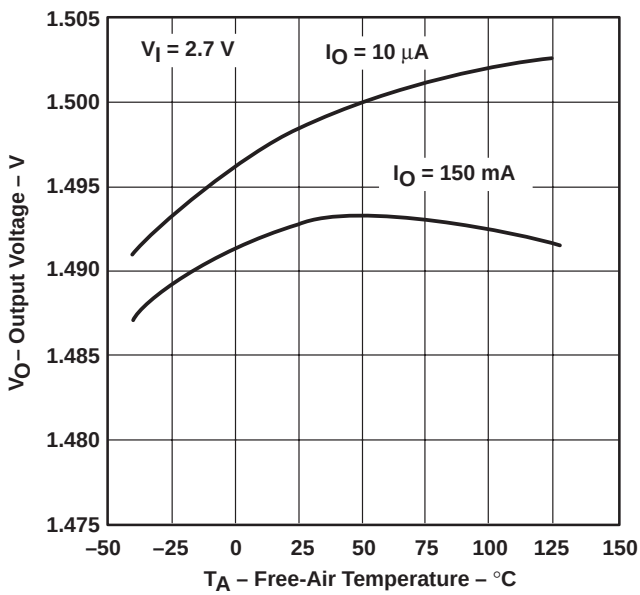


Figure 5

TYPICAL CHARACTERISTICS

TPS76533
GROUND CURRENT
vs
LOAD CURRENT

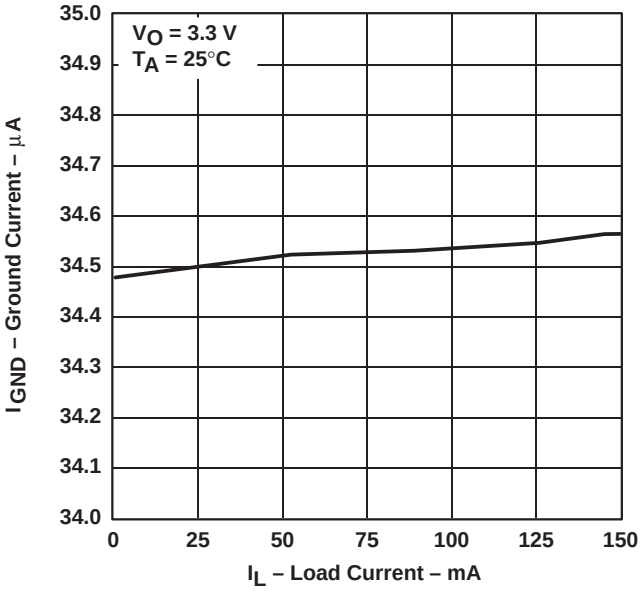


Figure 6

TPS76515
GROUND CURRENT
vs
LOAD CURRENT

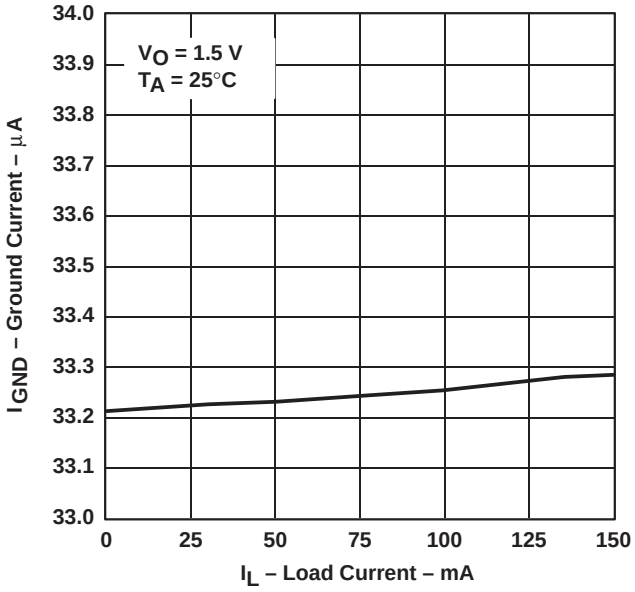


Figure 7

TPS76533
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

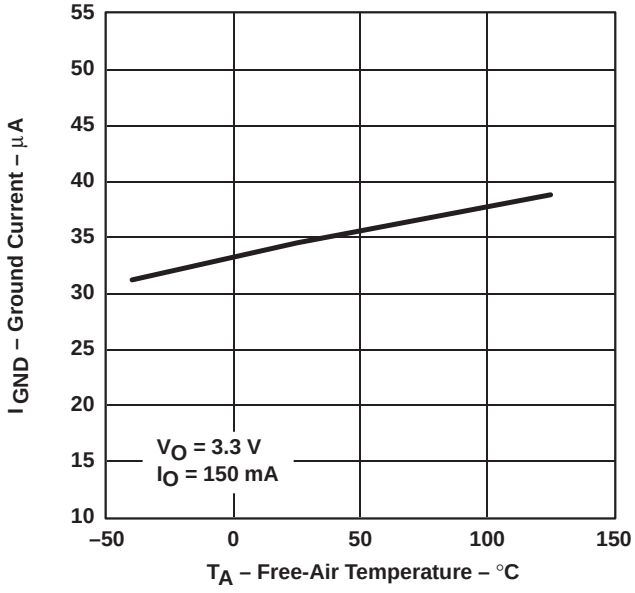


Figure 8

TPS76515
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

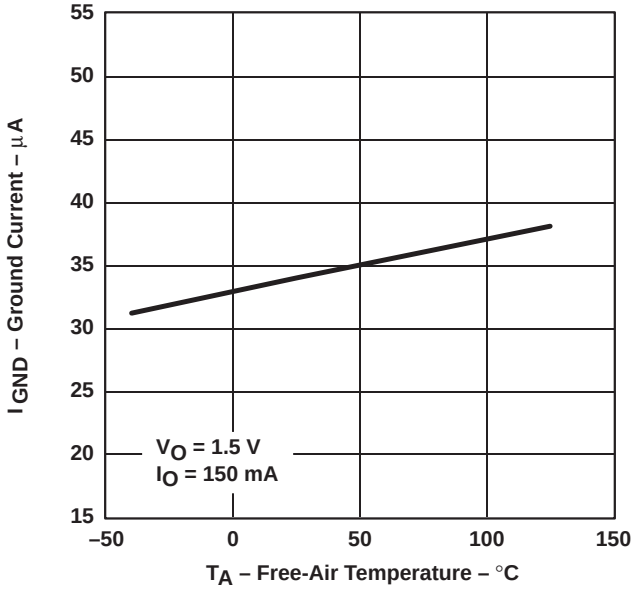


Figure 9

TYPICAL CHARACTERISTICS

TPS76533
POWER SUPPLY RIPPLE REJECTION
vs
FREQUENCY

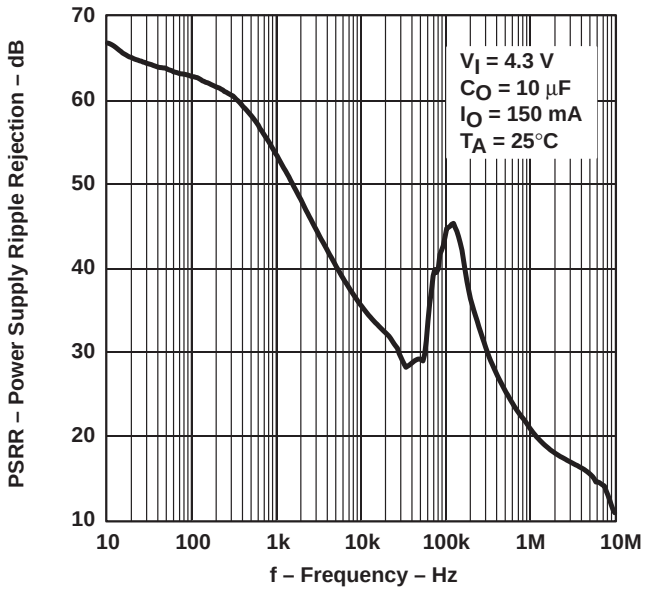


Figure 10

TPS76533
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

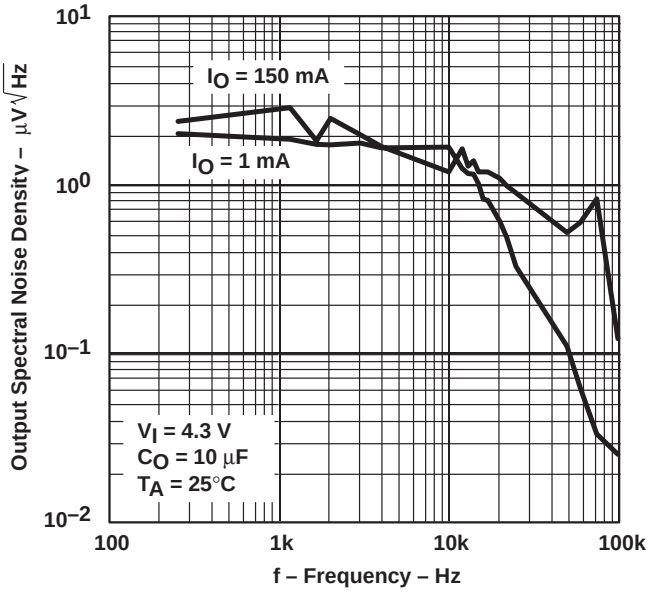


Figure 11

TPS76533
OUTPUT IMPEDANCE
vs
FREQUENCY

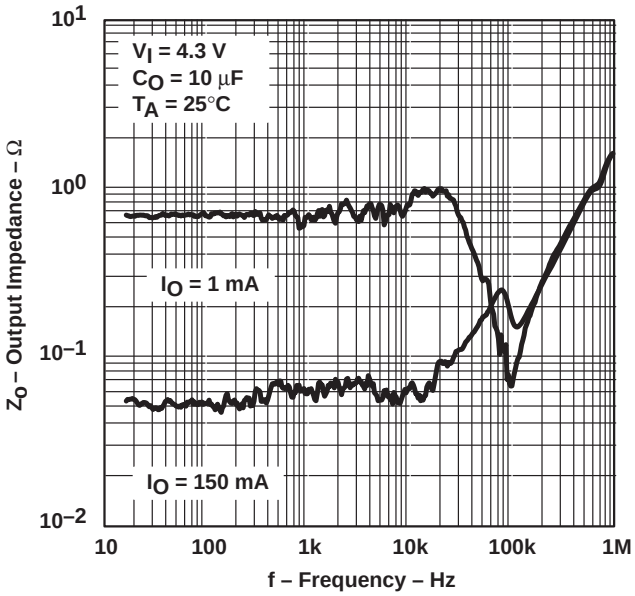


Figure 12

TYPICAL CHARACTERISTICS

TPS76550
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE

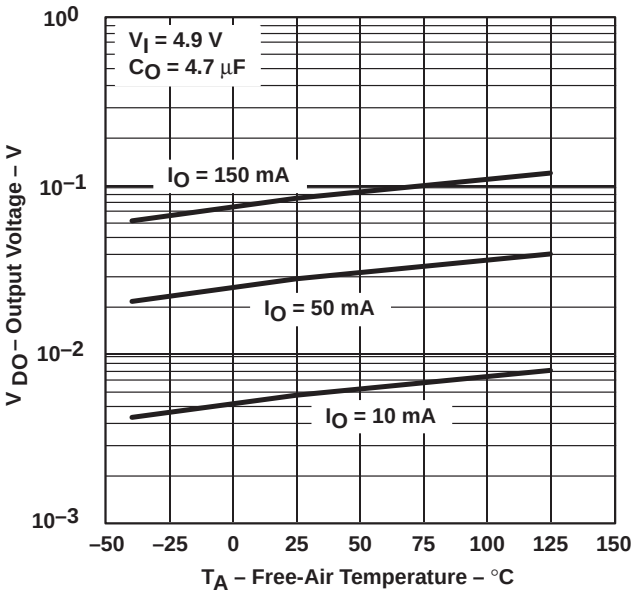


Figure 13

TPS76533
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE

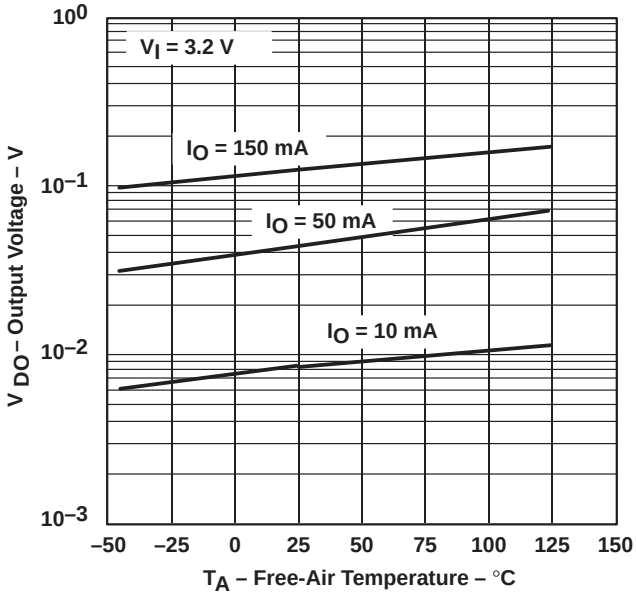


Figure 14

TPS76515
LINE TRANSIENT RESPONSE

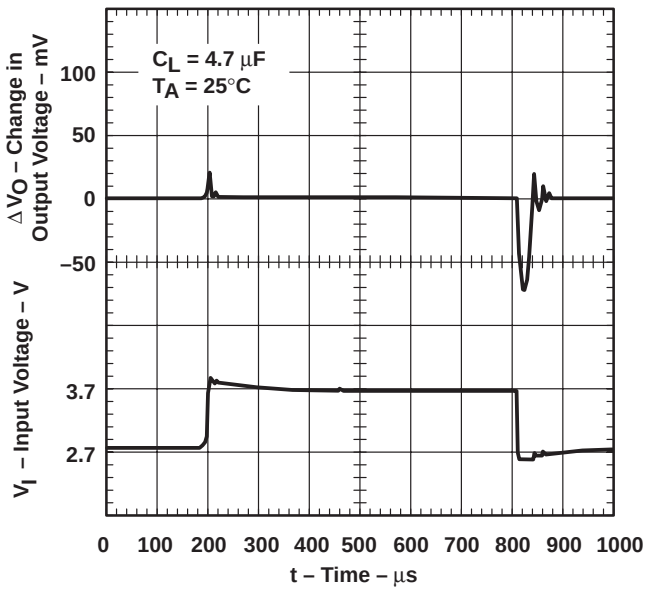


Figure 15

TPS76515
LOAD TRANSIENT RESPONSE

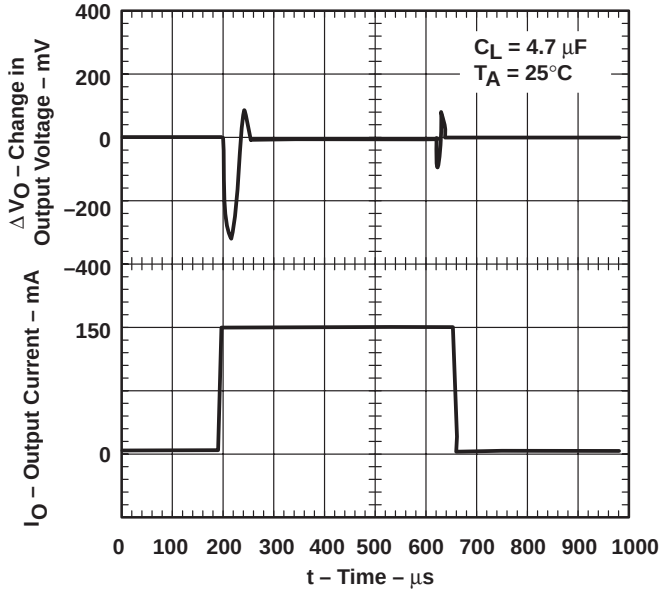


Figure 16

TYPICAL CHARACTERISTICS

TPS76533
LINE TRANSIENT RESPONSE

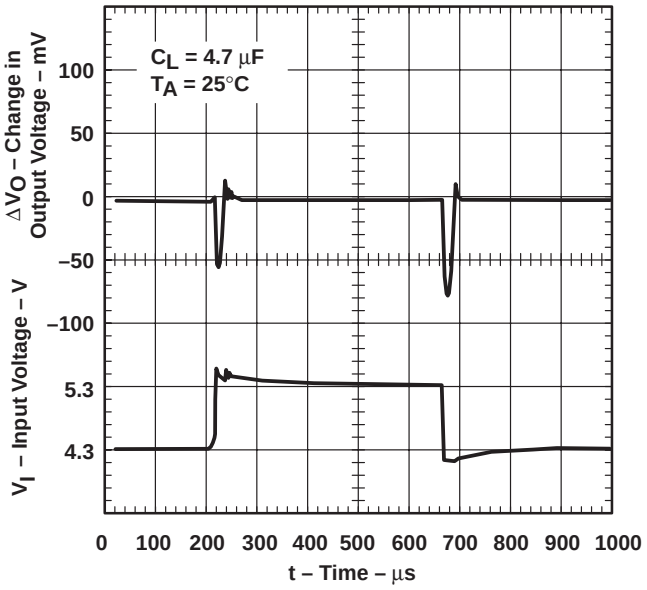


Figure 17

TPS76533
LOAD TRANSIENT RESPONSE

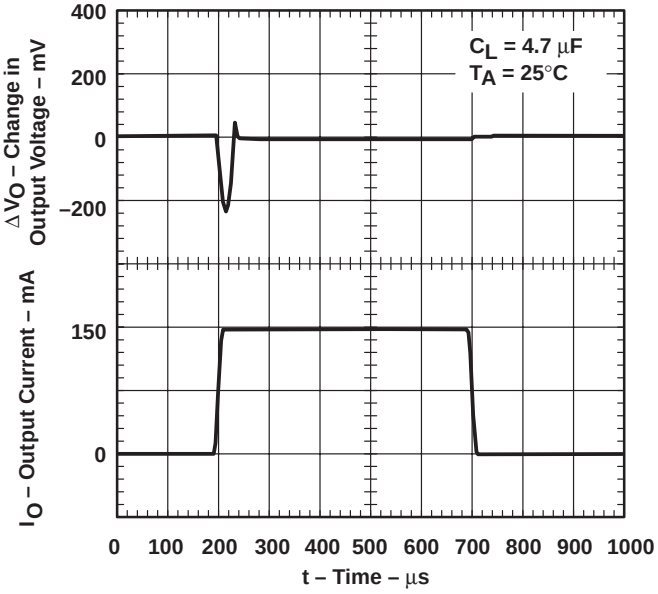


Figure 18

TPS76533
OUTPUT VOLTAGE
vs
TIME (AT STARTUP)

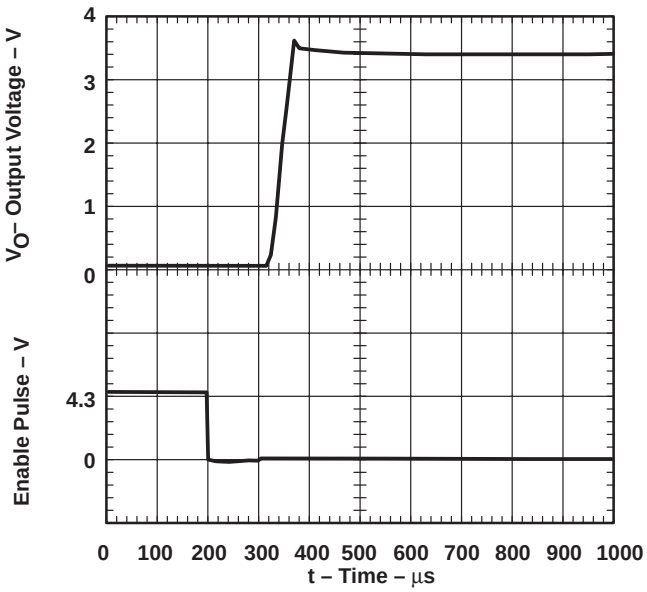


Figure 19

TPS76501
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

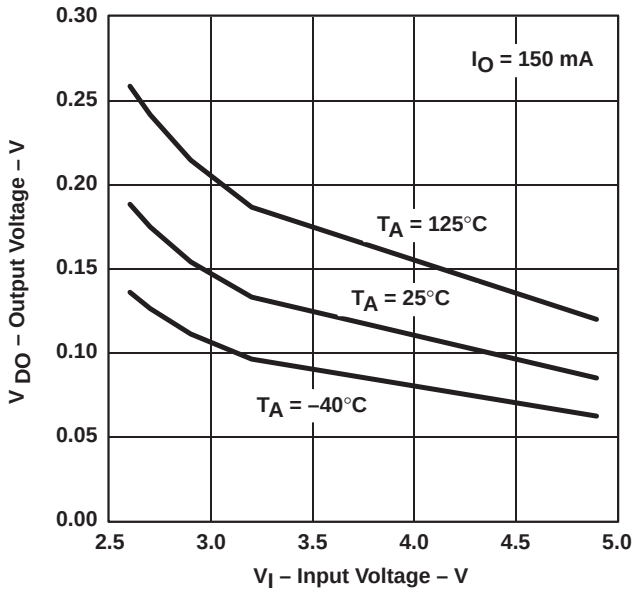


Figure 20

TYPICAL CHARACTERISTICS

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE† vs OUTPUT CURRENT

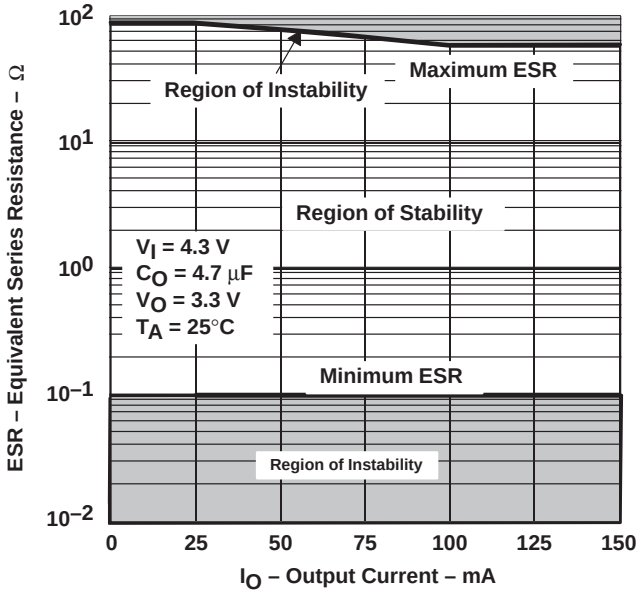


Figure 21

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE† vs OUTPUT CURRENT

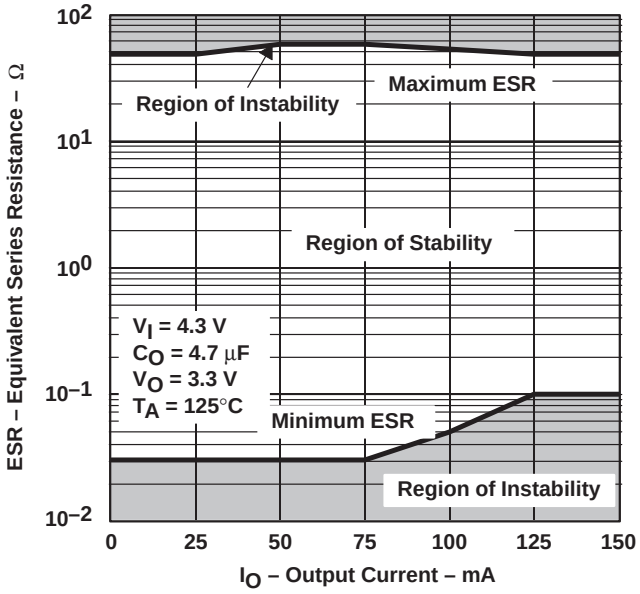


Figure 22

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE† vs OUTPUT CURRENT

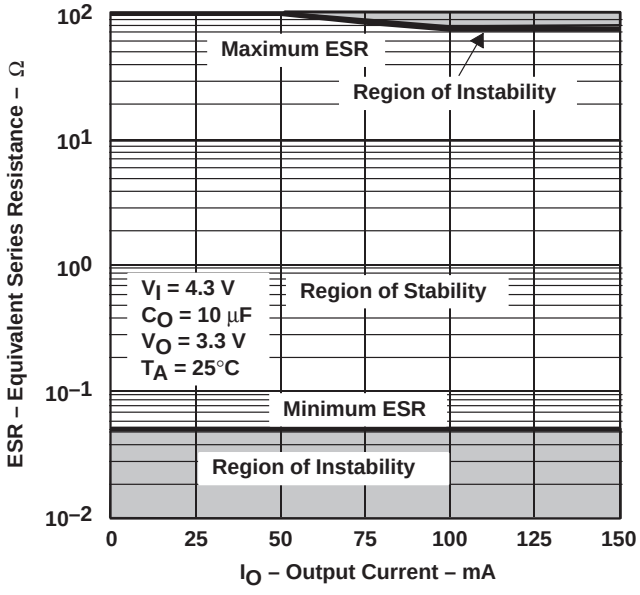


Figure 23

TYPICAL REGION OF STABILITY
EQUIVALENT SERIES RESISTANCE† vs OUTPUT CURRENT

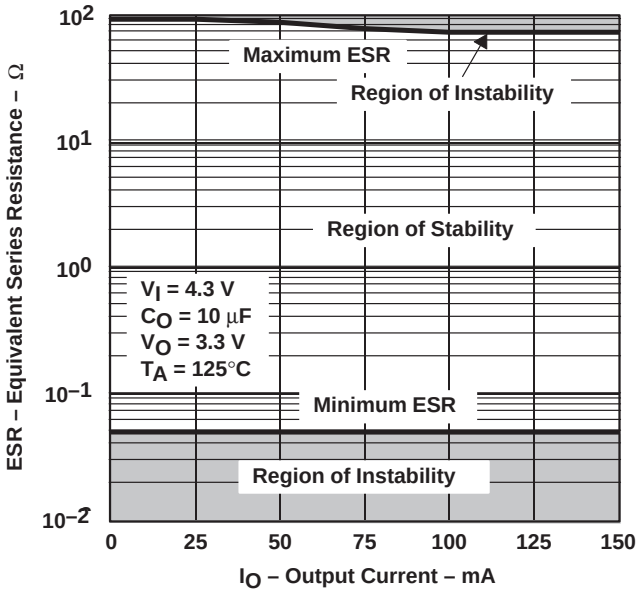


Figure 24

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

TYPICAL CHARACTERISTICS

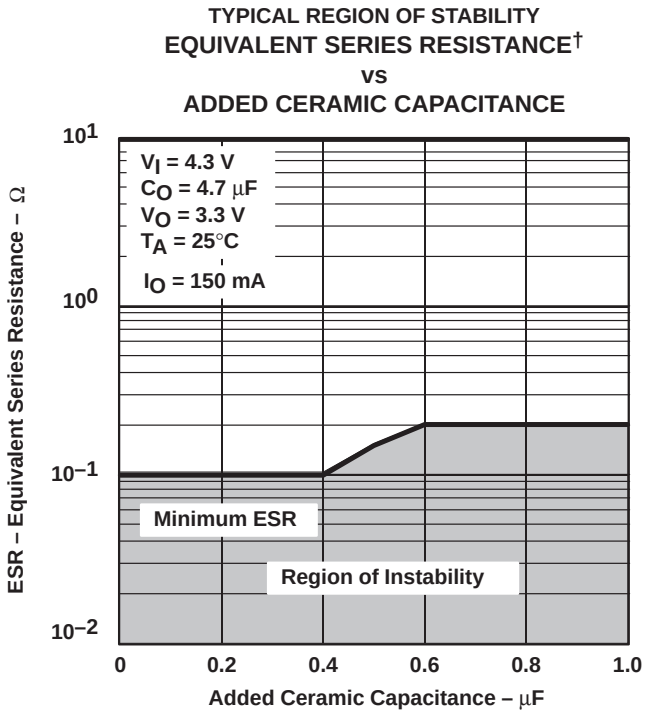


Figure 25

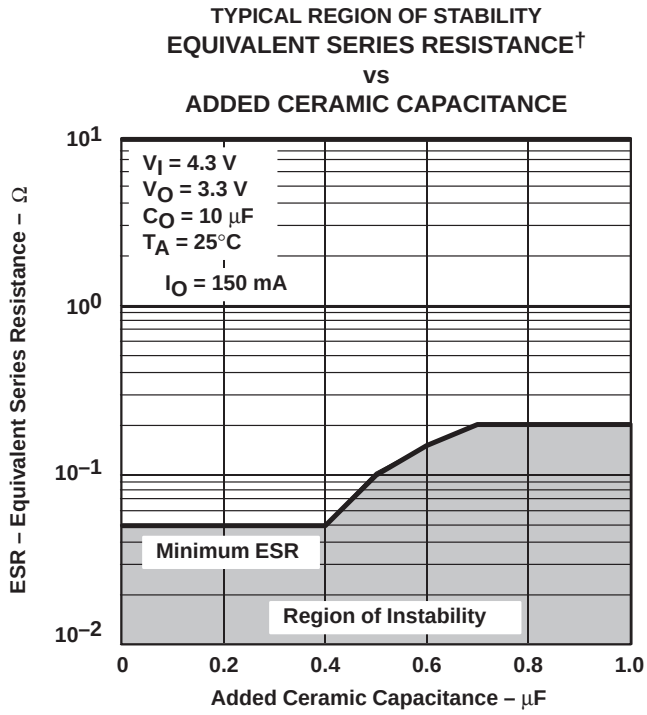


Figure 26

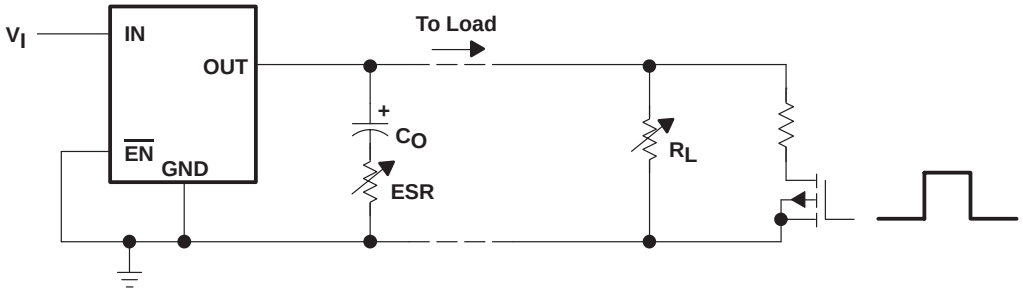


Figure 27. Test Circuit for Typical Regions of Stability (Figures 20 through 23) (Fixed Output Options)

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

APPLICATION INFORMATION

The TPS765xx family includes eight fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 3.0 V, 3.3 V, and 5.0 V), and an adjustable regulator, the TPS76501 (adjustable from 1.25 V to 5.5 V).

device operation

The TPS765xx features very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS765xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS765xx quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS765xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 1 μA (typ). If the shutdown feature is not used, $\overline{EN}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically 160 μs.

minimum load requirements

The TPS765xx family is stable even at zero load; no minimum load is required for operation.

FB - pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option . The output voltage is sensed through a resistor divider network to close the loop as it is shown in Figure 29. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

external capacitor requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 μF or larger) improves load transient response and noise rejection if the TPS765xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS765xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 4.7 μF and the ESR (equivalent series resistance) must be between 300-mΩ and 20-Ω. Capacitor values 4.7 μF or larger are acceptable, provided the ESR is less than 20 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.

APPLICATION INFORMATION

external capacitor requirements (continued)

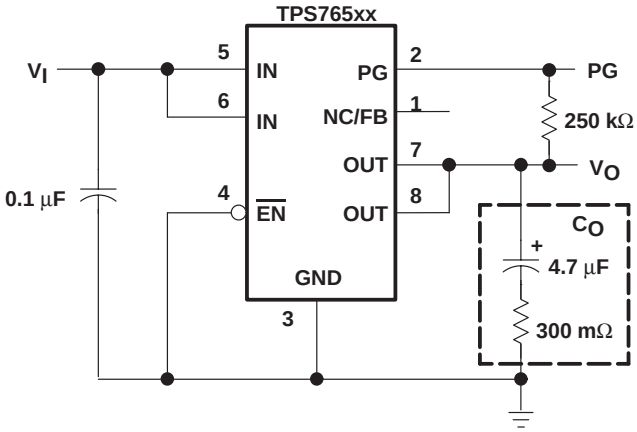


Figure 28. Typical Application Circuit (Fixed Versions)

programming the TPS76501 adjustable LDO regulator

The output voltage of the TPS76501 adjustable regulator is programmed using an external resistor divider as shown in Figure 29. The output voltage is calculated using:

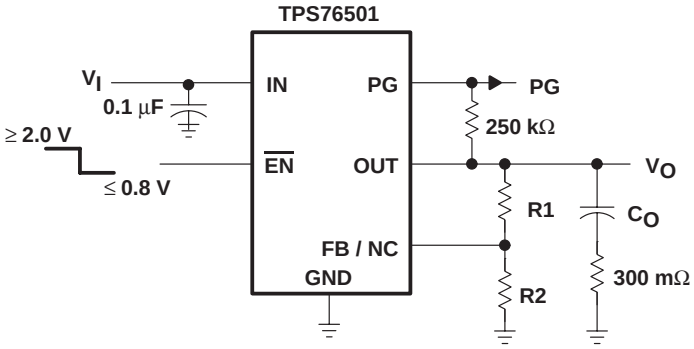
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where

V_{ref} = 1.224 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 7-µA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 kΩ to set the divider current at 7 µA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (2)$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	174	169	kΩ
3.3 V	287	169	kΩ
3.6 V	324	169	kΩ
4.0 V	383	169	kΩ
5.0 V	523	169	kΩ

Figure 29. TPS76501 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

power-good indicator

The TPS765xx features a power-good (PG) output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. PG can be used to drive power-on reset circuitry or used as a low-battery indicator.

regulator protection

The TPS765xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS765xx also features internal current limiting and thermal protection. During normal operation, the TPS765xx limits output current to approximately 0.8 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where

$T_J max$ is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 176°C/W for the 8-terminal SOIC.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62095RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SMC	Samples
TPS62095RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SMC	Samples
TPS62406QDRCRQ1	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	2406Q	Samples
TPS62407QDRCRQ1	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	SHU	Samples
TPS62422QDRCRQ1	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	2422Q	Samples
TPS62423QDRCRQ1	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	2423Q	Samples
TPS62424QDRCRQ1	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	2424Q	Samples
TPS76501D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76501	Samples
TPS76501DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76501	Samples
TPS76515D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76515	Samples
TPS76518D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76518	Samples
TPS76518DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76518	Samples
TPS76518DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76518	Samples
TPS76518DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76518	Samples
TPS76525D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76525	Samples
TPS76528D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76528	Samples
TPS76533D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76533	Samples
TPS76533DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76533	Samples
TPS76533DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76533	Samples
TPS76533DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76533	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS76550D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76550	Samples
TPS76550DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76550	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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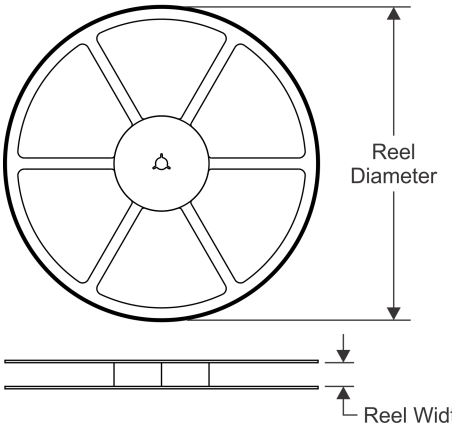
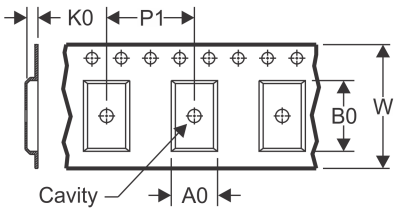
TAPE AND REEL INFORMATION

REEL DIMENSIONS

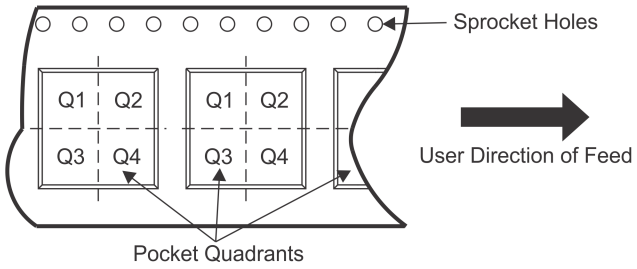


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

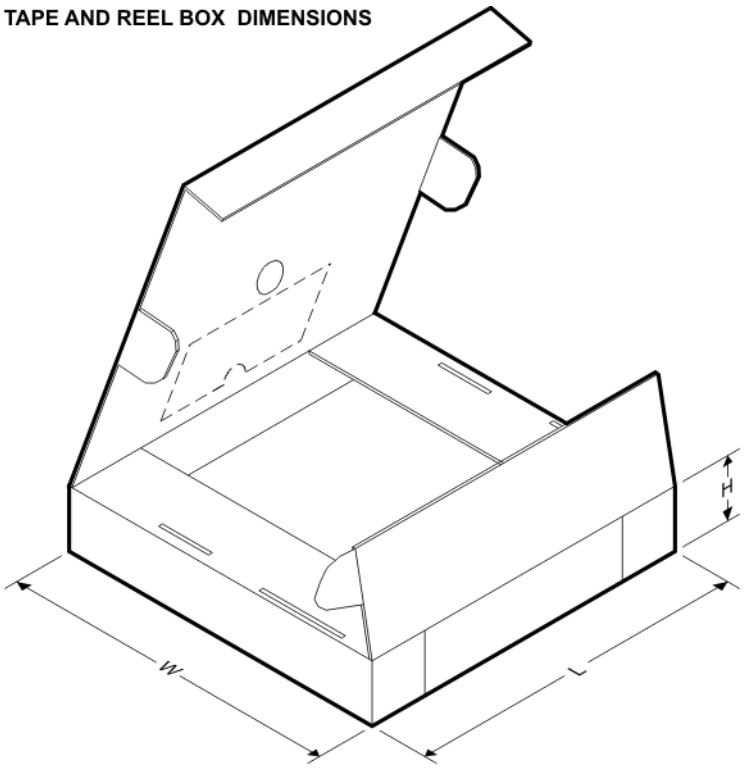
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62095RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62095RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62406QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62407QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62422QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62423QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62424QDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS76501DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76518DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76533DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76550DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

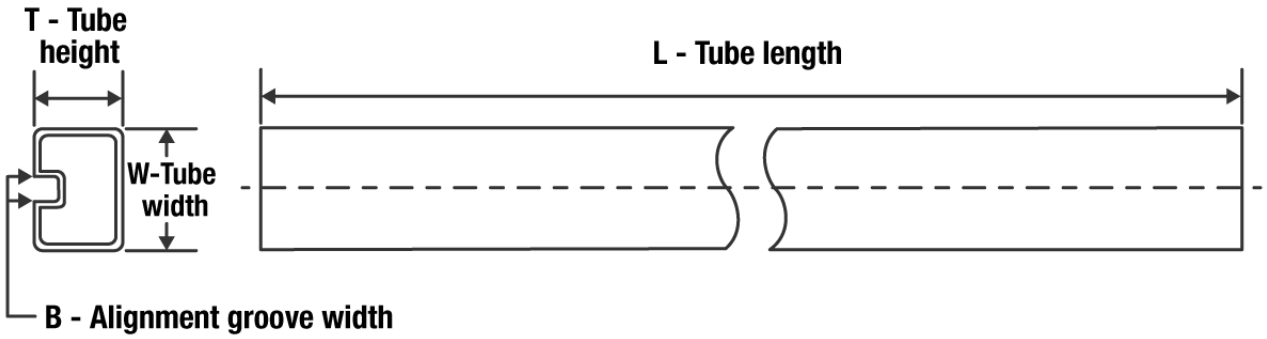
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62095RGTR	VQFN	RGT	16	3000	552.0	367.0	36.0
TPS62095RGTT	VQFN	RGT	16	250	552.0	185.0	36.0
TPS62406QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
TPS62407QDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0
TPS62422QDRCRQ1	VSON	DRC	10	3000	338.0	355.0	50.0
TPS62423QDRCRQ1	VSON	DRC	10	3000	338.0	355.0	50.0
TPS62424QDRCRQ1	VSON	DRC	10	3000	338.0	355.0	50.0
TPS76501DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76518DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76533DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76550DR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE

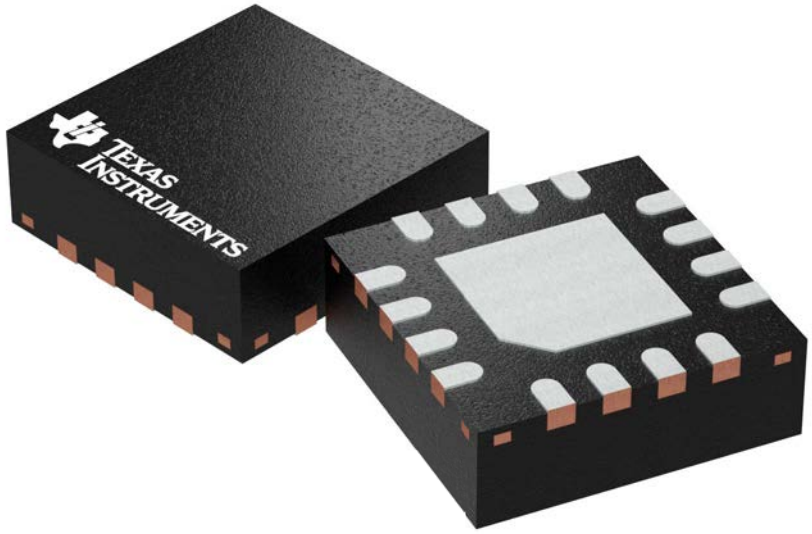


*All dimensions are nominal

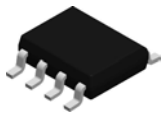
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS62095RGTR	RGT	VQFN	16	3000	381	4.83	2286	0
TPS62095RGTT	RGT	VQFN	16	250	381	4.83	2286	0
TPS76501D	D	SOIC	8	75	505.46	6.76	3810	4
TPS76515D	D	SOIC	8	75	505.46	6.76	3810	4
TPS76518D	D	SOIC	8	75	505.46	6.76	3810	4
TPS76518DG4	D	SOIC	8	75	505.46	6.76	3810	4
TPS76525D	D	SOIC	8	75	505.46	6.76	3810	4
TPS76528D	D	SOIC	8	75	505.46	6.76	3810	4
TPS76533D	D	SOIC	8	75	505.46	6.76	3810	4
TPS76533DG4	D	SOIC	8	75	505.46	6.76	3810	4
TPS76550D	D	SOIC	8	75	505.46	6.76	3810	4

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

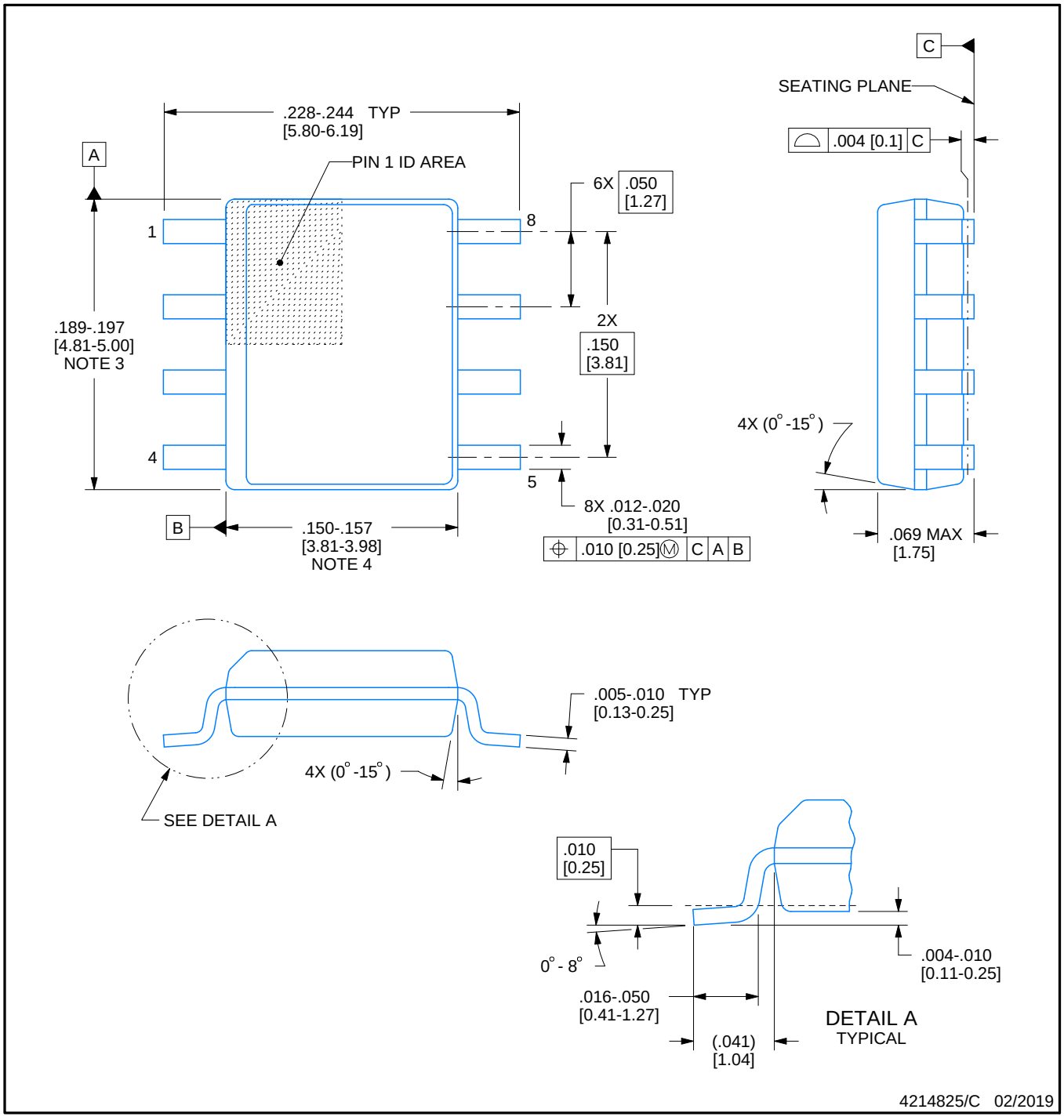


PACKAGE OUTLINE

D0008A

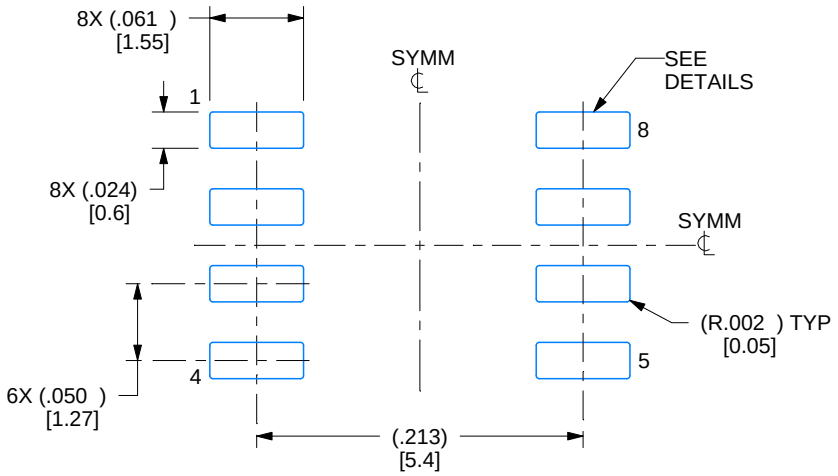
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

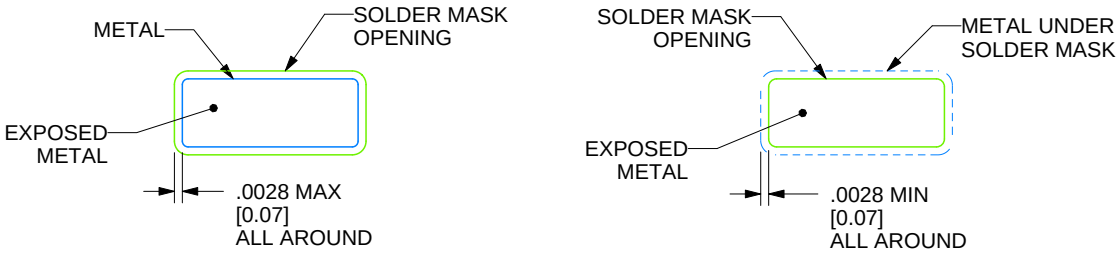


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

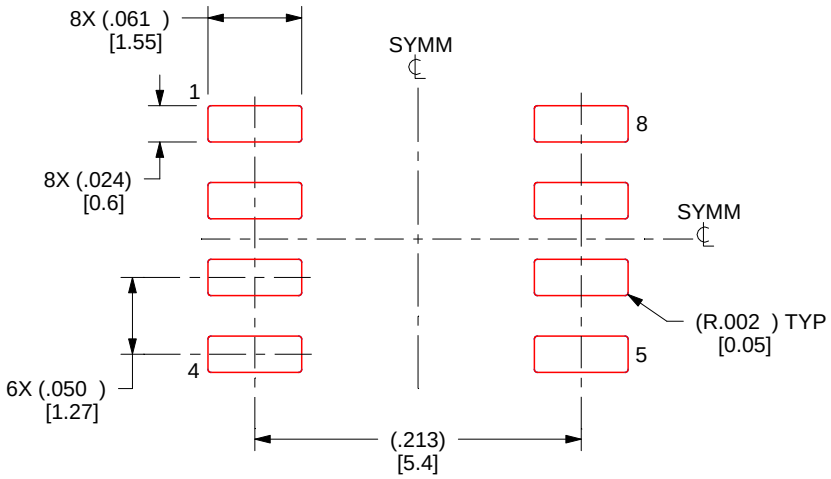
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

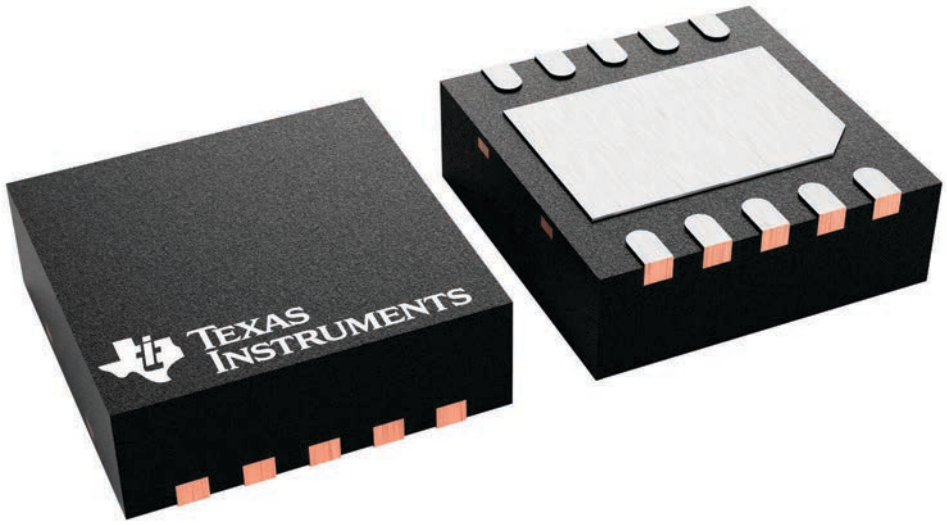
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



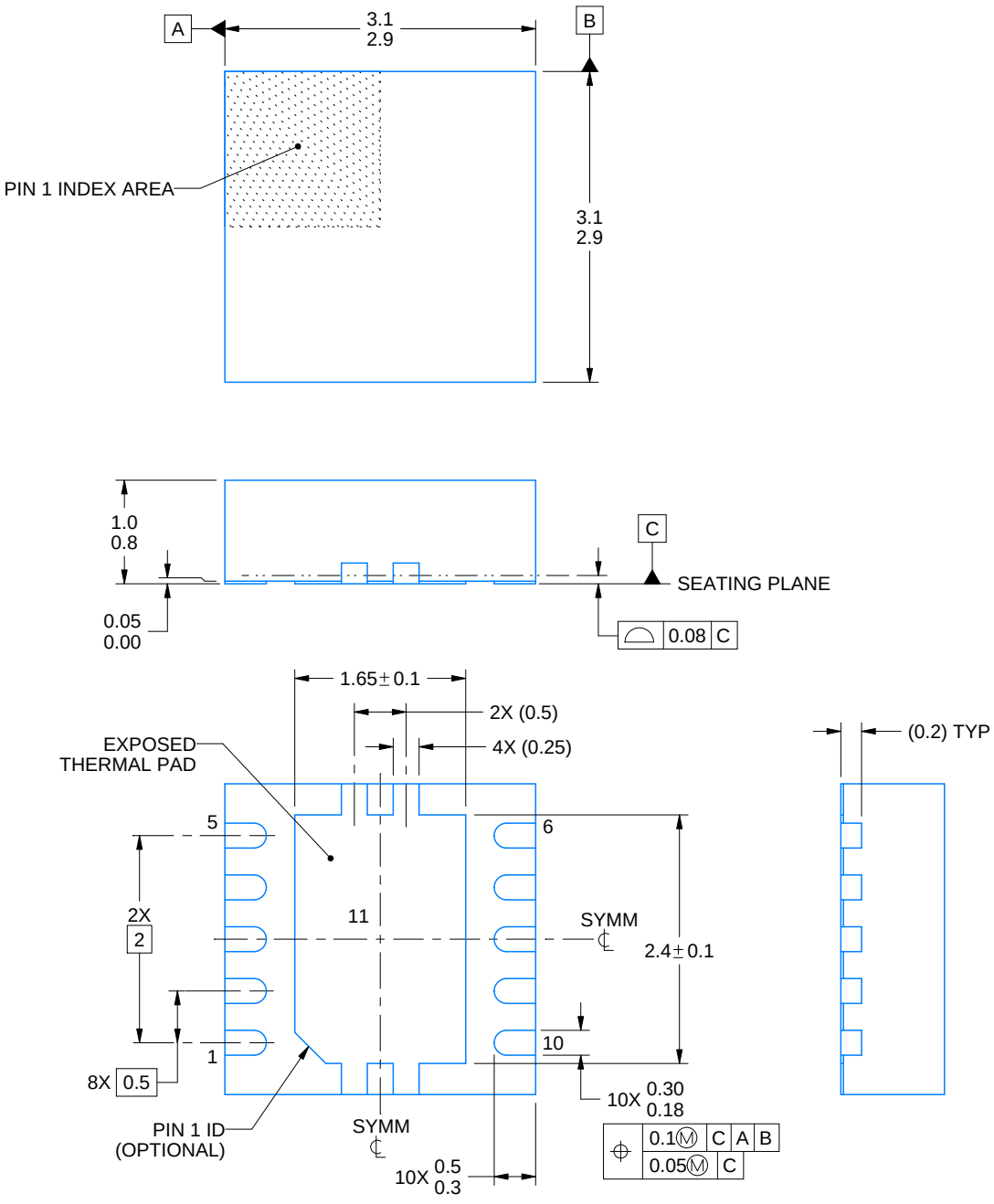
4226193/A

DRC0010J

PACKAGE OUTLINE

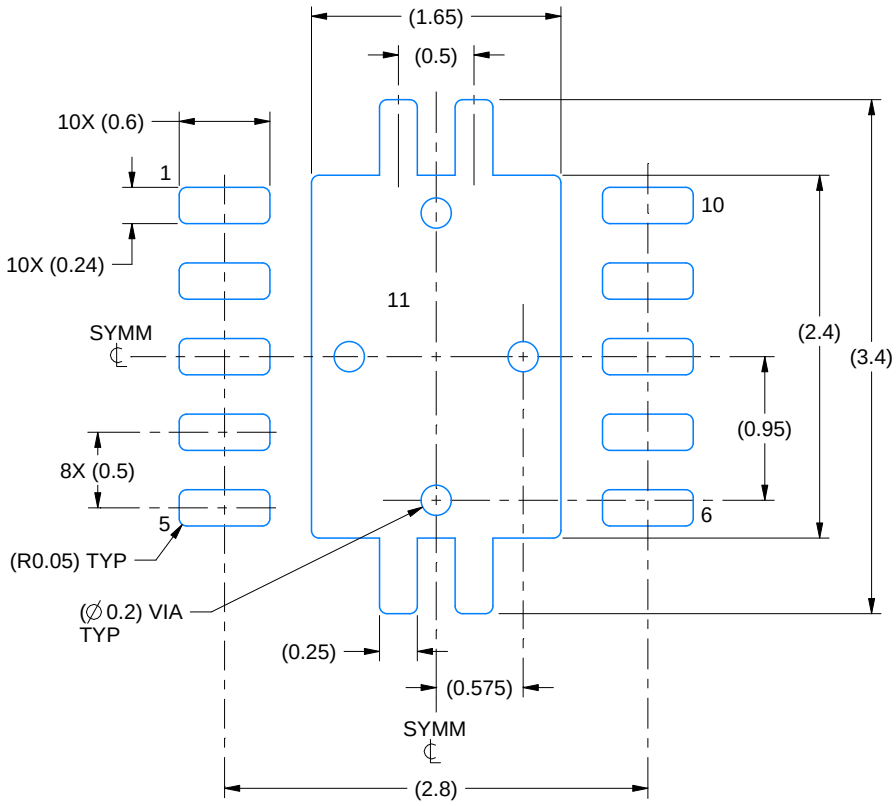
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

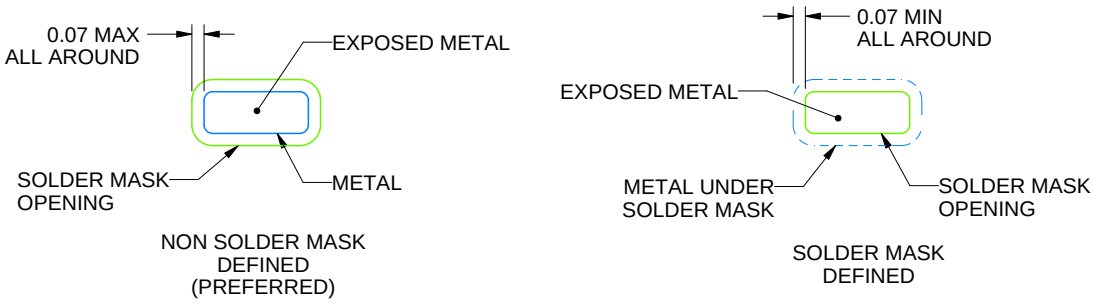


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

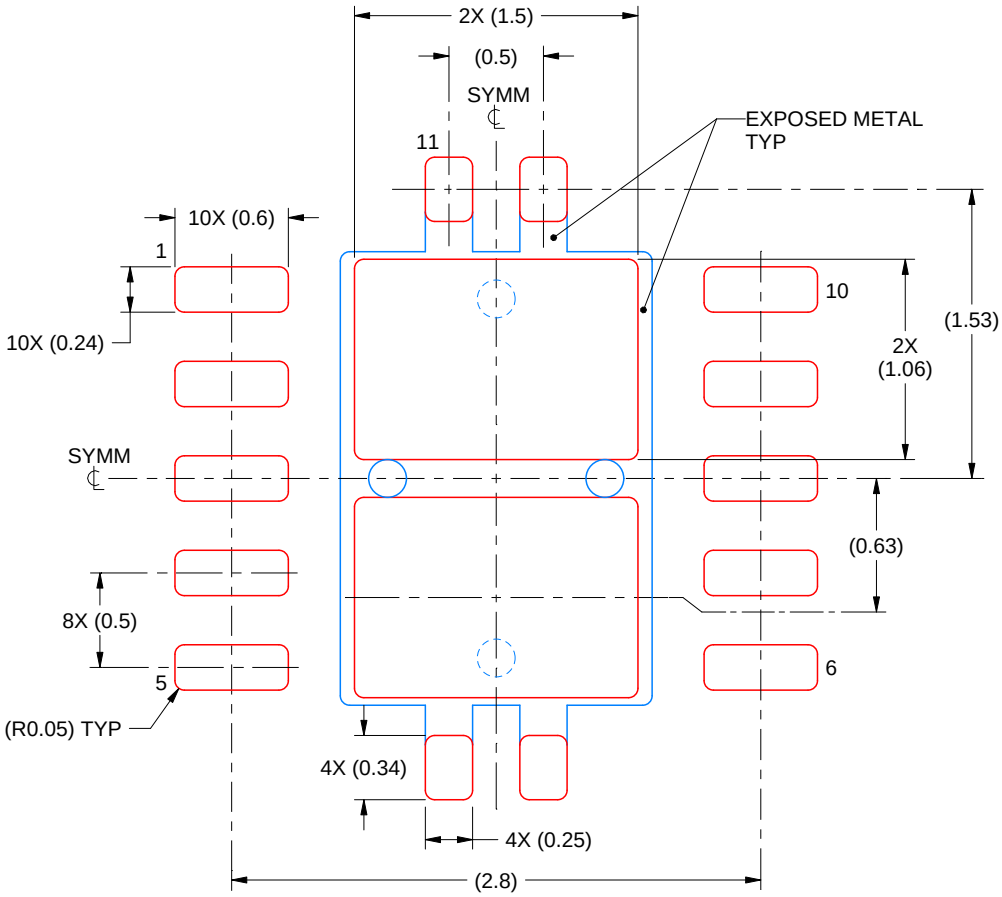
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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