

TPS79901-EP 200mA 低静态电流、超低噪声、高 PSRR 低压降线性稳压器

1 特性

- 带 EN 引脚的 200mA 低压降稳压器
- 提供了多个输出电压版本：
 - 1.2V 至 6.5V 可调输出
- 带有 EN 切换的浪涌电流保护
- 低 I_Q : 40 μ A
- 高 PSRR:
 - 1kHz 时为 66dB
 - 10kHz 时为 51dB
- 与一个低 ESR、2 μ F（典型值）输出电容一起工作时保持稳定
- 出色的负载和线路瞬态响应
- 整体精度（负载、线路和温度）为 2%
- 极低压降：100 mV
- 封装：6 引脚 SON
- 支持国防、航天和医疗应用
 - 受控基线
 - 同一组装和测试场所
 - 同一制造场所
 - 支持军用（-55°C 至 125°C）温度范围
 - 延长的产品生命周期
 - 延长的产品变更通知
 - 产品可追溯性

2 应用范围

- 基站
- 智能手机
- EPOS
- 可穿戴电子产品
- VCO、射频
- 无线 LAN，蓝牙®

3 说明

TPS79901 系列低压降 (LDO)、低功耗线性稳压器能够提供出色的交流性能，同时还能实现极低的接地电流。可提供高电源抑制比 (PSRR)、低噪声、快速启动以及出色的线路和负载瞬态响应，同时消耗极低的 40 μ A（典型值）接地电流。

TPS79901 与陶瓷电容器搭配使用时可保持稳定，并且该器件使用先进的 BiCMOS 制造工艺，能够在输出 200mA 电流时产生 100mV 的典型压降值。TPS79901 使用精密电压基准和反馈环路，可在全部负载、线路、过程和温度变化范围内实现 2% 的总体精度。TPS79901 具有浪涌电流保护功能，当 EN 切换用于启动器件时可立即钳制电流。

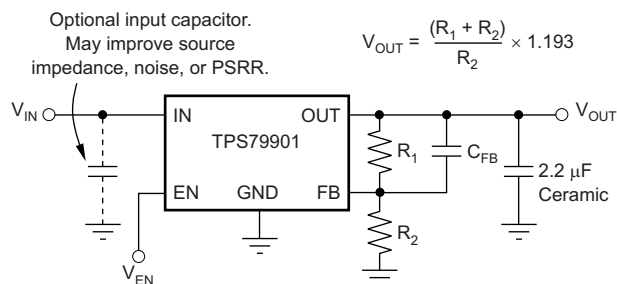
TPS79901 的额定温度范围为 $T_J = -55^\circ\text{C}$ 至 $+125^\circ\text{C}$ ，并采用小型封装，非常适用于手机和 WLAN 卡。

器件信息⁽¹⁾

器件型号	封装	封装尺寸（标称值）
TPS79901-EP	SON (6)	2.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的封装选项附录。

典型应用电路



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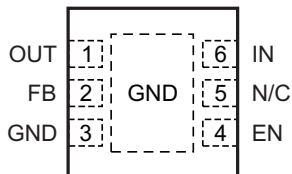
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (September 2017) to Revision A	Page
• 已更改 更改了特性 部分中的内容	1
• 已更改 更改了说明 部分中的内容	1
• Deleted NR from the Pin Functions table	3
• Changed HBM value from ± 2000 : to ± 1500 in the <i>ESD Ratings</i> section	4
• Deleted errant part numbers from the <i>Electrical Characteristics</i> section	5
• Deleted errant part numbers from the <i>Typical Characteristics</i> section	7

5 Pin Configuration and Functions

**DRV Package
6-Pin SON With Exposed Thermal Pad
Top View**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN	6	I	Input supply.
GND	3, Pad	—	Ground. The pad must be tied to GND.
EN	4	I	Driving this pin high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
FB	2	I	Adjustable voltage version only. Feedback; this pin is the input to the control loop error amplifier and sets the output voltage of the device.
OUT	1	O	Output of the regulator. To assure stability, a small ceramic capacitor (total typical capacitance $\geq 2 \mu\text{F}$) is required from this pin to ground.
N/C	5	—	Not internally connected. This pin must either be left open or tied to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage ⁽²⁾	IN	−0.3	7	V
	EN	−0.3	$V_{IN} + 0.3$	
	OUT	−0.3	$V_{IN} + 0.3$	
Current	OUT	Internally limited		mA
Temperature	Operating virtual junction, T_J	−55	150	°C
	Storage temperature range, T_{stg}	−55	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage ⁽¹⁾	2.7		6.5	V
I_{OUT}	Output current	0.5		200	mA
T_J	Operating junction temperature	−55		125	°C

- (1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7 V, whichever is greater.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS799	UNIT
		DRV (SON)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	145.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.2	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

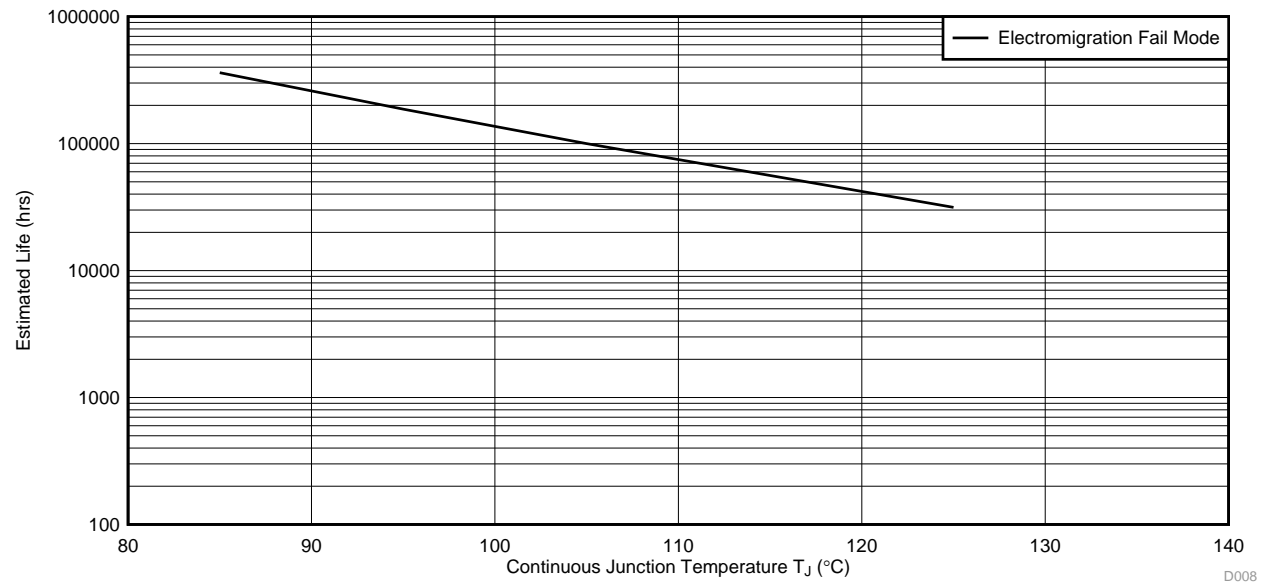
6.5 Electrical Characteristics

at $T_J = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ or 2.7 V , whichever is greater; $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, and $V_{OUT} = 3\text{ V}$ (unless otherwise noted). Typical values are at $T_J = 25^{\circ}\text{C}$.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			2.7		6.5	V
V_{FB}	Internal reference			1.169	1.193	1.217	V
V_{OUT}	Output voltage range			V_{FB}	$6.5 - V_{DO}$		V
	Output accuracy, nominal	$T_J = 25^{\circ}\text{C}$		-1%		1%	
	Output accuracy ⁽¹⁾ over V_{IN} , I_{OUT} , temperature	$V_{OUT} + 0.3\text{ V} \leq V_{IN} \leq 6.5\text{ V}$ $500\text{ }\mu\text{A} \leq I_{OUT} \leq 200\text{ mA}$		-2%	$\pm 1\%$	2%	
$\Delta V_{O(\Delta VI)}$	Line regulation ⁽¹⁾	$V_{OUT(nom)} + 0.3\text{ V} \leq V_{IN} \leq 6.5\text{ V}$			0.02		%/V
$\Delta V_{O(\Delta IO)}$	Load regulation	$500\text{ }\mu\text{A} \leq I_{OUT} \leq 200\text{ mA}$			0.002		%/mA
V_{DO}	Dropout voltage ⁽²⁾ ($V_{IN} = V_{OUT(nom)} - 0.1\text{ V}$)	$I_{OUT} = 200\text{ mA}$	$V_{OUT(nom)} \leq 3.3\text{ V}$		100	175	mV
			$V_{OUT(nom)} \geq 3.3\text{ V}$		90	160	
I_{CL}	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(nom)}$		220	400	600	mA
I_{GND}	Ground pin current	$500\text{ }\mu\text{A} \leq I_{OUT} \leq 200\text{ mA}$			40	60	μA
I_{SHDN}	Shutdown current (I_{GND})	$V_{EN} \leq 0.4\text{ V}$, $2.7\text{ V} \leq V_{IN} \leq 6.5\text{ V}$			0.15	1	μA
I_{FB}	Feedback pin current			-0.5		0.5	μA
PSRR	Power-supply rejection ratio	$V_{IN} = 3.85\text{ V}$, $V_{OUT} = 2.85\text{ V}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, $I_{OUT} = 100\text{ mA}$	$f = 100\text{ Hz}$		70		dB
			$f = 1\text{ kHz}$		66		
			$f = 10\text{ kHz}$		51		
			$f = 100\text{ kHz}$		38		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, $V_{OUT} = 2.85\text{ V}$	$C_{NR} = 0.01\text{ }\mu\text{F}$		$10.5 \times V_{OUT}$		μVRMS
			$C_{NR} = \text{none}$		$94 \times V_{OUT}$		
	Start-up time	$V_{OUT} = 2.85\text{ V}$, $R_L = 14\text{ }\Omega$, $C_{OUT} = 2.2\text{ }\mu\text{F}$	$C_{NR} = 0.001\text{ }\mu\text{F}$		45		μs
			$C_{NR} = 0.047\text{ }\mu\text{F}$		45		
			$C_{NR} = 0.01\text{ }\mu\text{F}$		50		
			$C_{NR} = \text{none}$		50		
$V_{EN(HI)}$	Enable high (enabled)			1.2		V_{IN}	V
$V_{EN(LO)}$	Enable low (shutdown)			0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled	$V_{EN} = V_{IN} = 6.5\text{ V}$			0.03	1	μA
UVLO	Undervoltage lockout	V_{IN} rising		1.90	2.20	2.65	V
	UVLO hysteresis	V_{IN} falling			70		mV
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing			165		$^{\circ}\text{C}$
		Reset, temperature decreasing			145		

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7 V , whichever is greater.

(2) V_{DO} is not measured for $V_{OUT(nom)} < 2.8\text{ V}$ because minimum $V_{IN} = 2.7\text{ V}$.



- (1) See data sheet for absolute maximum and minimum recommended operating conditions.
- (2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
- (3) Enhanced plastic product disclaimer applies.

Figure 1. TPS79901-EP Derating Chart

6.6 Typical Characteristics

at $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ or 2.7 V , whichever is greater; $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, and $V_{OUT} = 3\text{ V}$ (unless otherwise noted). Typical values are at $T_J = 25^\circ\text{C}$.

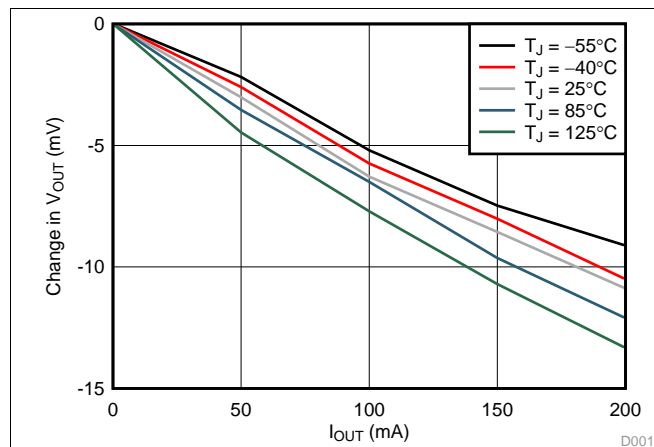


Figure 2. Load Regulation

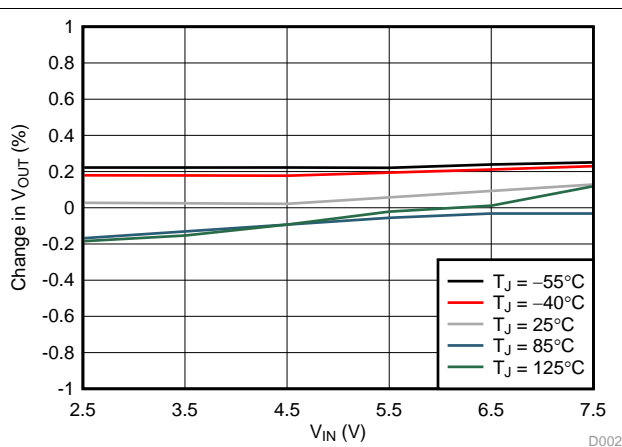


Figure 3. Line Regulation

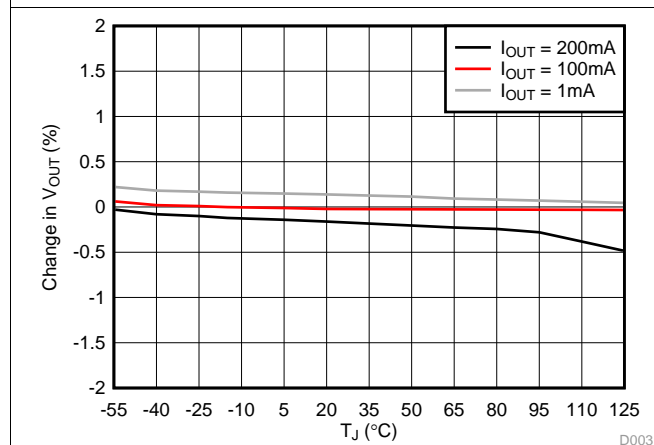


Figure 4. Output Voltage vs Junction Temperature

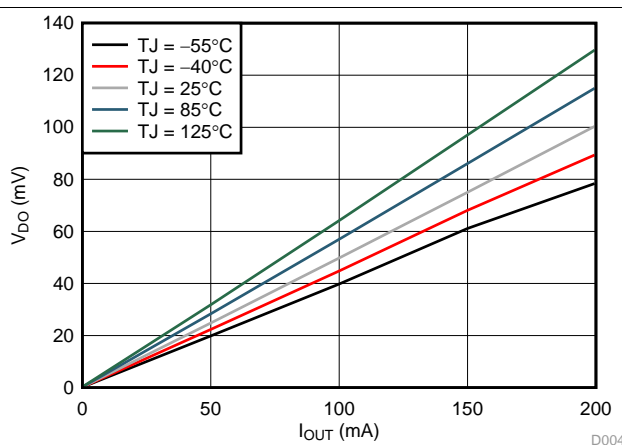


Figure 5. Dropout Voltage vs Output Current

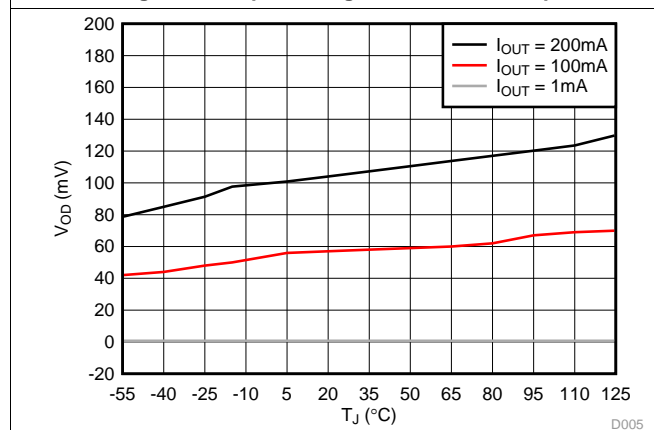


Figure 6. Dropout Voltage vs Junction Temperature

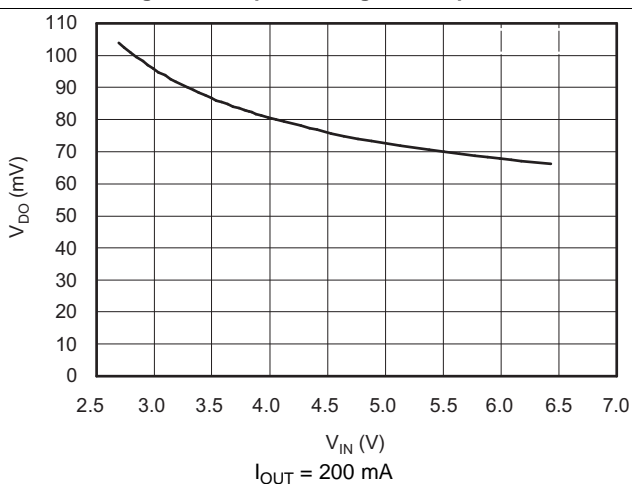


Figure 7. Dropout vs Input Voltage

Typical Characteristics (continued)

at $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ or 2.7 V , whichever is greater; $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, and $V_{OUT} = 3\text{ V}$ (unless otherwise noted). Typical values are at $T_J = 25^\circ\text{C}$.

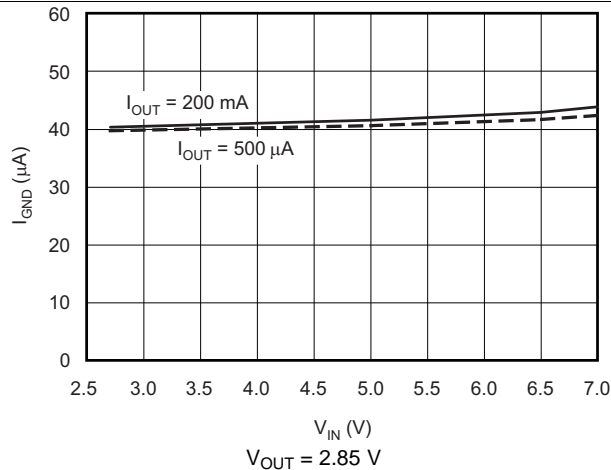


Figure 8. Ground Pin Current vs Input Voltage

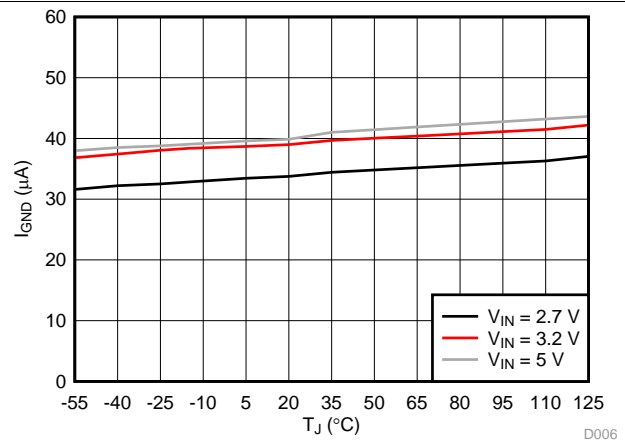


Figure 9. Ground Pin Current vs Junction Temperature

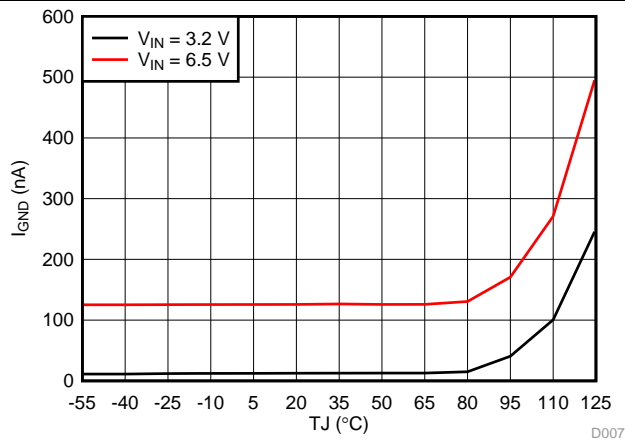


Figure 10. Ground Pin Current (Disabled) vs Junction Temperature

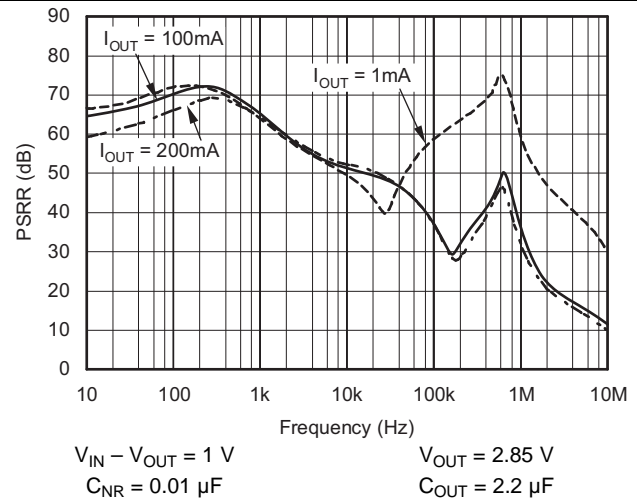


Figure 11. Power-Supply Ripple Rejection vs Frequency

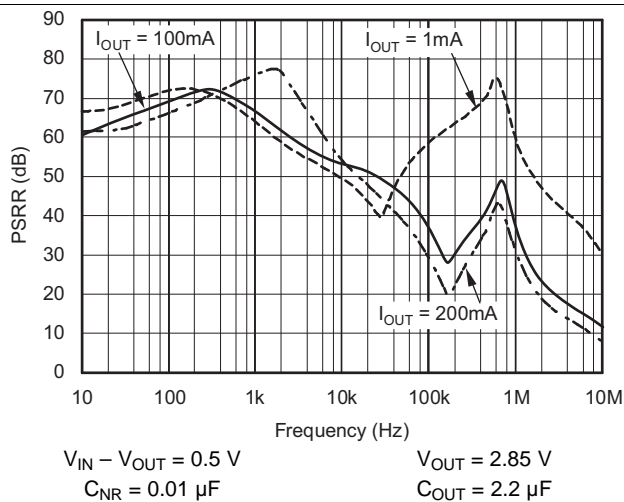


Figure 12. Power-Supply Ripple Rejection vs Frequency

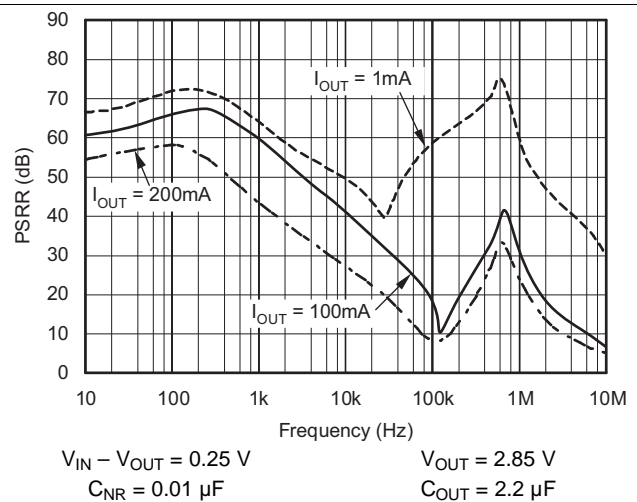


Figure 13. Power-Supply Ripple Rejection vs Frequency

Typical Characteristics (continued)

at $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ or 2.7 V , whichever is greater; $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, and $V_{OUT} = 3\text{ V}$ (unless otherwise noted). Typical values are at $T_J = 25^\circ\text{C}$.

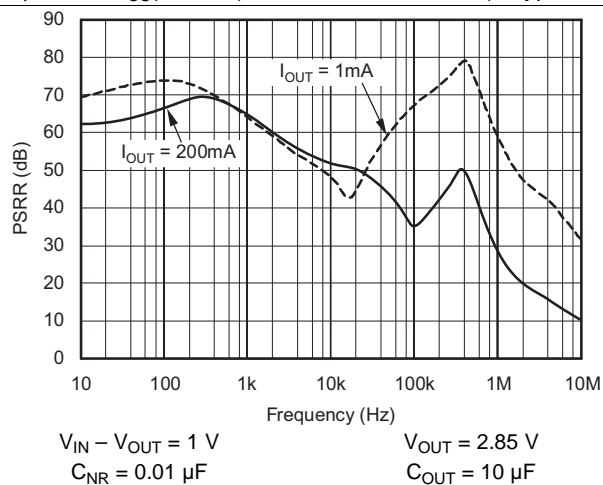


Figure 14. Power-Supply Ripple Rejection vs Frequency

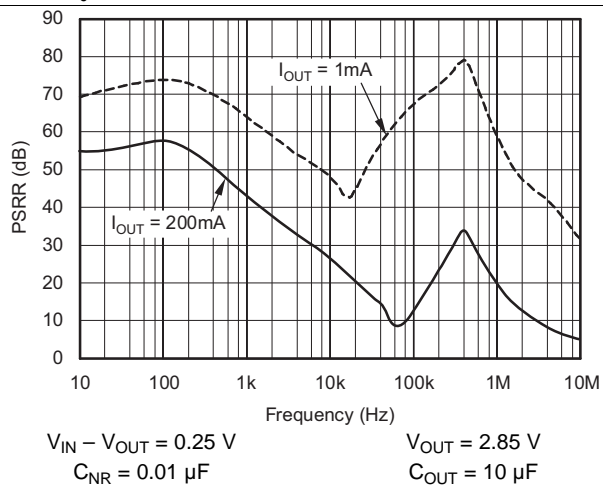


Figure 15. Power-Supply Ripple Rejection vs Frequency

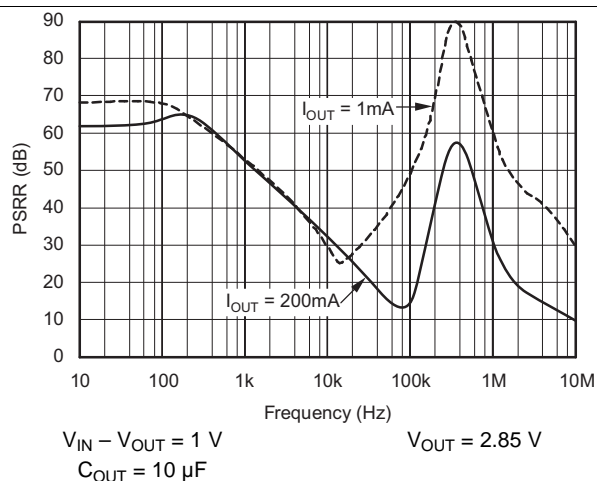


Figure 16. Power-Supply Ripple Rejection vs Frequency

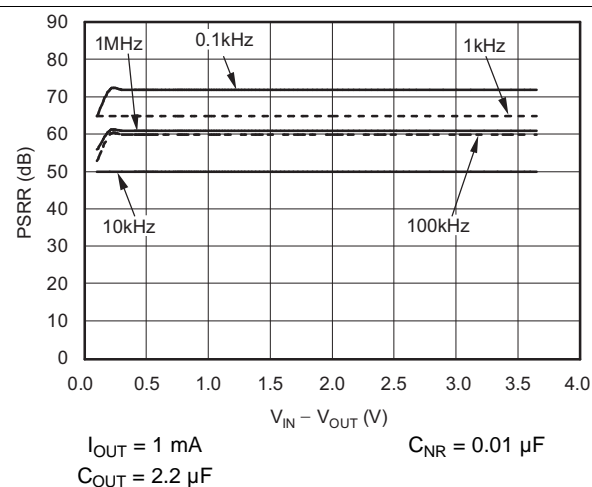


Figure 17. Power-Supply Ripple Rejection vs $V_{IN} - V_{OUT}$

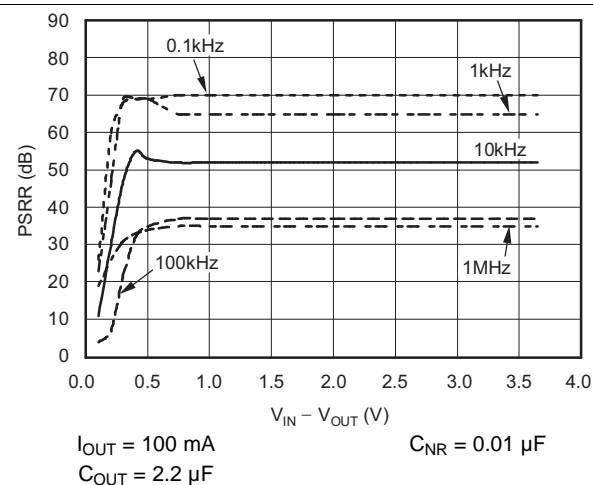


Figure 18. Power-Supply Ripple Rejection vs $V_{IN} - V_{OUT}$

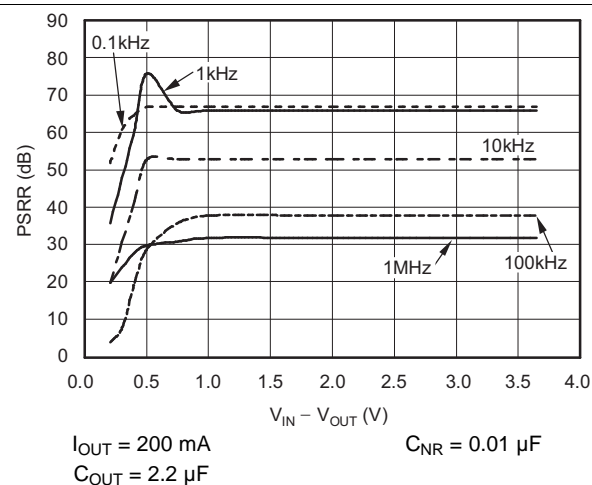
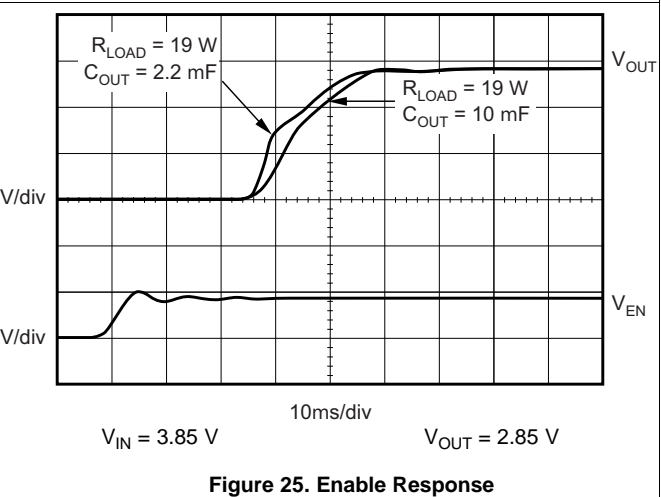
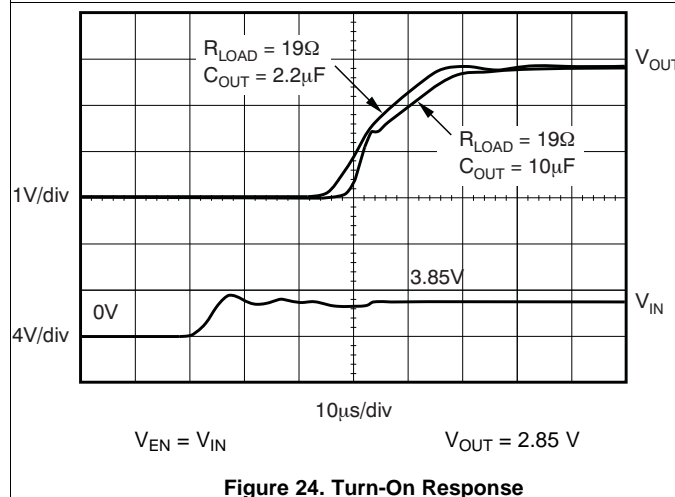
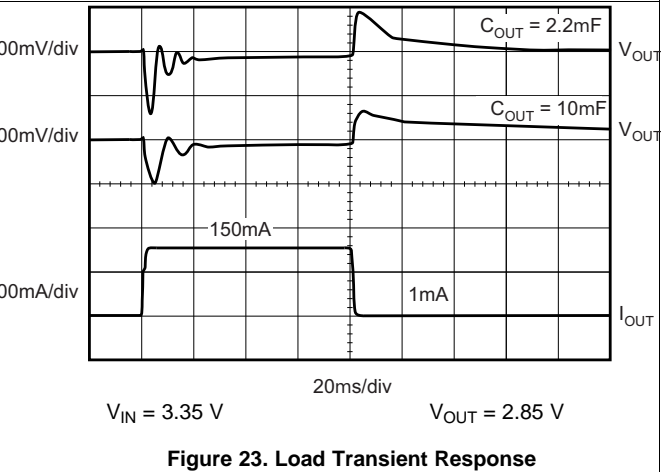
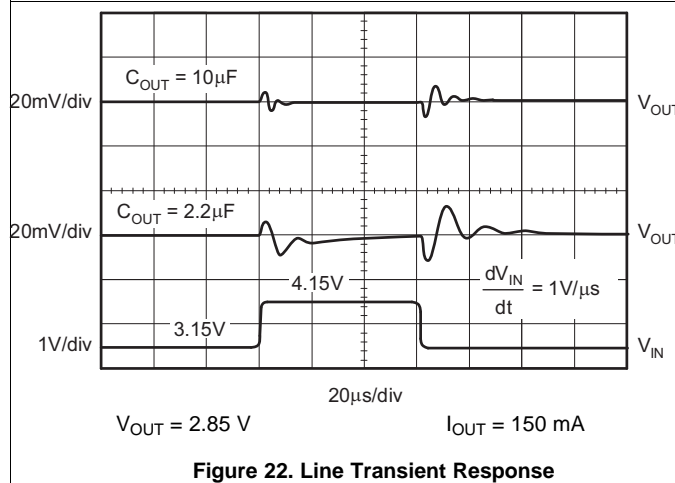
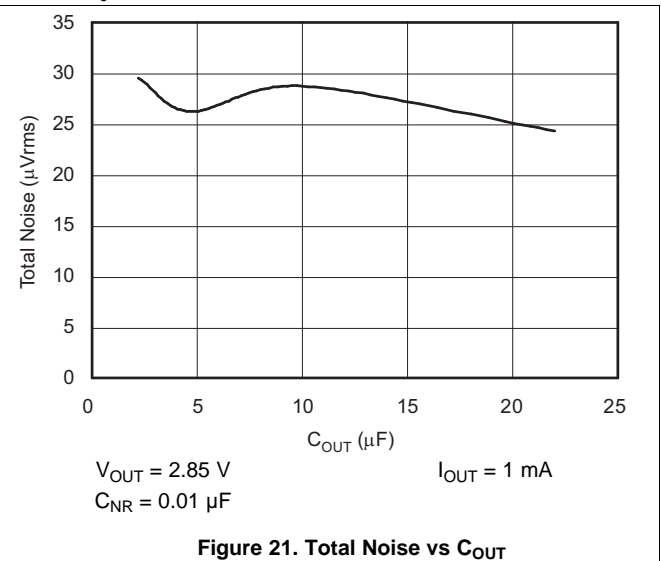
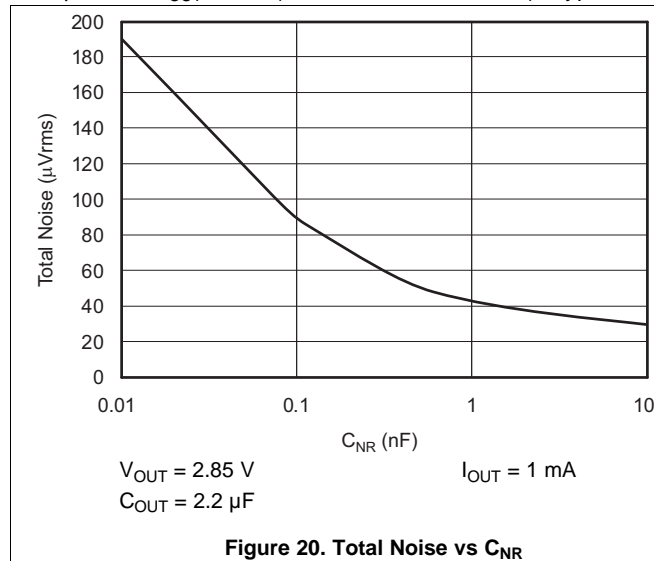


Figure 19. Power-Supply Ripple Rejection vs $V_{IN} - V_{OUT}$

Typical Characteristics (continued)

at $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ or 2.7 V , whichever is greater; $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, and $V_{OUT} = 3\text{ V}$ (unless otherwise noted). Typical values are at $T_J = 25^\circ\text{C}$.



Typical Characteristics (continued)

at $T_J = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.3\text{ V}$ or 2.7 V , whichever is greater; $I_{OUT} = 1\text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, and $V_{OUT} = 3\text{ V}$ (unless otherwise noted). Typical values are at $T_J = 25^{\circ}\text{C}$.

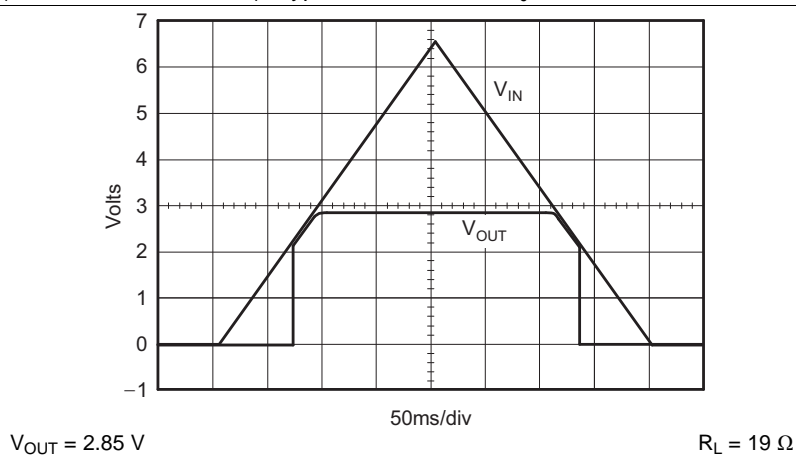


Figure 26. Power-Up and Power-Down

7 Detailed Description

7.1 Overview

The TPS79901 low-dropout (LDO) regulator combines the high performance required of many RF and precision analog applications with ultra-low-current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection at very low headroom ($V_{IN} - V_{OUT}$). A noise-reduction pin is provided to bypass noise generated by the band-gap reference and to improve PSRR, while a quick-start circuit quickly charges this capacitor at start-up. The combination of high performance and low ground current also make these devices an excellent choice for portable applications. All versions have thermal and overcurrent protection, and are fully specified from -55°C to $+125^{\circ}\text{C}$.

The TPS79901 also features inrush current protection with an EN toggle start-up, and overshoot detection at the output. When the EN toggle is used to start the device, current limit protection is immediately activated, restricting the inrush current to the device. If voltage at the output overshoots 5% from the nominal value, a pulldown resistor reduces the voltage to normal operating conditions, as shown in the [Functional Block Diagram](#).

7.2 Functional Block Diagram

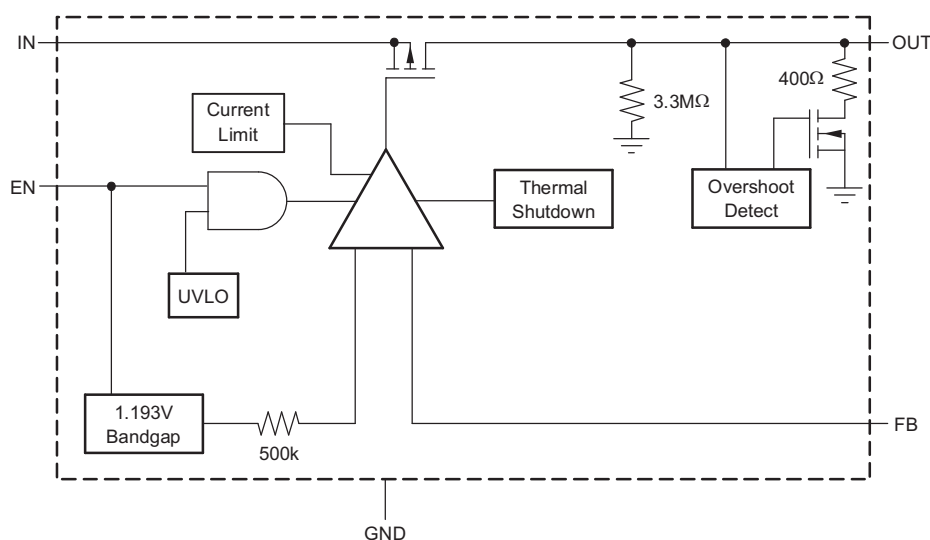


Figure 27. Adjustable-Voltage Versions

7.3 Feature Description

7.3.1 Internal Current Limit

The TPS79901 internal current limit helps protect the regulator during fault conditions. In current limit mode, the output sources a fixed amount of current that is largely independent of the output voltage. For reliable operation, do not operate the device in a current-limit state for extended periods of time.

The PMOS pass element in the TPS79901 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited; therefore, if extended reverse voltage operation is anticipated, external limiting may be required.

7.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

Feature Description (continued)

7.3.3 Start Up

The TPS79901 uses a start-up circuit to quickly charge the noise reduction capacitor, C_{NR} , if present (see the [Functional Block Diagram](#)). This circuit allows for the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate for this configuration.

Note that for fastest start-up, apply V_{IN} first, and then drive the enable pin (EN) high. If EN is tied to IN, start-up is somewhat slower. The start-up switch is closed for approximately 135 μ s. To ensure that C_{NR} is fully charged during start-up, use a 0.01- μ F or smaller capacitor.

7.3.4 Undervoltage Lockout (UVLO)

The TPS79901 use an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that undershoot transients are typically ignored on the input if these transients are less than 50 μ s in duration.

7.4 Device Functional Modes

Driving EN over 1.2-V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode, thus reducing the operating current to 150 nA, nominal.

8 Application and Implementation

NOTE

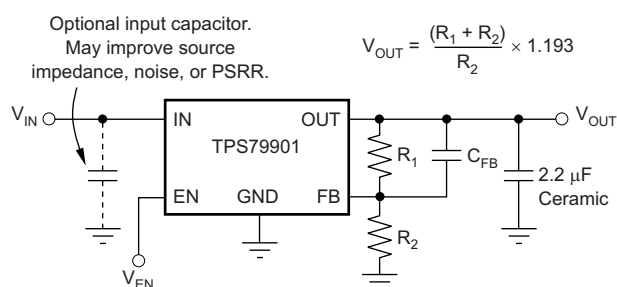
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS79901 LDO regulator provides high PSRR while maintaining ultra-low-current consumption. The device also features inrush current protection and overshoot detection at the output.

8.2 Typical Applications

Figure 28 shows the basic circuit connections.



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Figure 28. Typical Application Circuit for Adjustable Voltage Version

8.2.1 Design Requirements

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND terminal current, and power the load.

Typical Applications (continued)

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-μF to 1-μF low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-μF input capacitor may be necessary to ensure stability.

The TPS79901 is designed to be stable with standard ceramic capacitors with values of 2.2 μF or greater. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR must be less than 1 Ω.

8.2.2.2 Output Noise

In most LDOs, the band gap is the dominant noise source. If a noise-reduction capacitor (C_{NR}) is used with the TPS79901, the band gap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01-μF noise reduction capacitor. To further optimize noise, equivalent series resistance of the output capacitor can be set to approximately 0.2 Ω. This configuration maximizes phase margin in the control loop, reducing total output noise by up to 10%.

Noise can be referred to the feedback point; with $C_{NR} = 0.01 \mu\text{F}$ total noise is approximately given by [Equation 1](#):

$$V_N = \frac{10.5 \mu\text{V}_{\text{RMS}}}{V} \times V_{\text{OUT}} \quad (1)$$

8.2.2.3 Dropout Voltage

The TPS79901 uses a PMOS pass transistor to achieve a low-dropout voltage. When $(V_{\text{IN}} - V_{\text{OUT}})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and $r_{\text{DS(on)}}$ of the PMOS pass element is the input-to-output resistance. Because the PMOS device behaves like a resistor in dropout, V_{DO} approximately scales with the output current.

As with any linear regulator, PSRR degrades as $(V_{\text{IN}} - V_{\text{OUT}})$ approaches dropout. This effect is illustrated in [Figure 11](#) through [Figure 19](#) in the [Typical Characteristics](#) section.

8.2.2.4 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude, but increases the duration of the transient response. The transient response of the TPS799 is enhanced by an active pulldown device that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pulldown device behaves like a 350-Ω resistor to ground.

8.2.2.5 Minimum Load

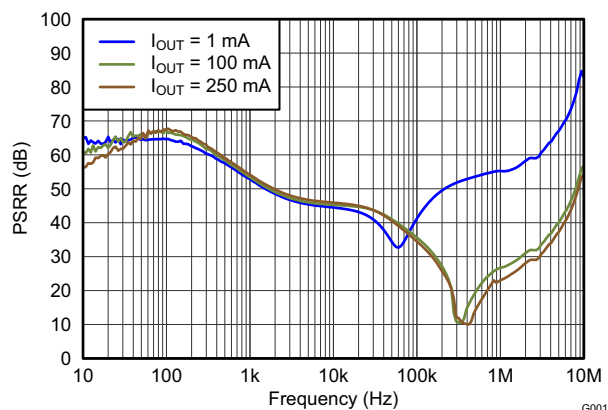
The TPS79901 is stable with no output load. To meet the specified accuracy, a minimum load of 500 μA is required. With loads less than 500 μA at junction temperatures near 125°C, the output can drift up enough to cause the output pulldown device to turn on. The output pulldown device limits voltage drift to 5% typically; however, ground current can increase by approximately 50 μA. In typical applications, the junction cannot reach high temperatures at light loads because there is no noticeable dissipated power. The specified ground current is then valid at no load in most applications.

8.2.2.6 Feedback Capacitor Requirements

The feedback capacitor, C_{FB} , shown in [Figure 28](#) is required for stability. For a parallel combination of R_1 and R_2 equal to 250 kΩ, any value from 3 pF to 1 nF can be used. Values below 5 pF should be used to ensure fast startup; values above 47 pF can be used to implement an output voltage soft-start. Larger value capacitors also improve noise slightly. The TPS79901 is stable in unity-gain configuration (OUT tied to FB) without C_{FB} .

Typical Applications (continued)

8.2.3 Application Curve



$$C_{OUT} = 2.2 \mu F$$

$$C_{NR} = 0.01 \mu F$$

Figure 29. Power-Supply Rejection Ratio vs Frequency

8.3 Do's and Don'ts

Do place at least one 2.2- μF ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Do connect a 0.1- μF to 1- μF low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator.

Do not exceed the absolute maximum ratings.

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 2.7 V and 6.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply is well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device. In addition, connect the bypass capacitor directly to the GND pin of the device.

10.1.2 Thermal Information

10.1.2.1 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage resulting from overheating.

Layout Guidelines (continued)

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection triggers at least 35°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS799 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the device into thermal shutdown degrades device reliability.

10.1.2.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the [Thermal Information](#) table near the front of this data sheet. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element, as shown in [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} \quad (2)$$

10.1.2.3 Package Mounting

Solder pad footprint recommendations for the TPS799 are available from the TI's website at www.ti.com.

10.2 Layout Example

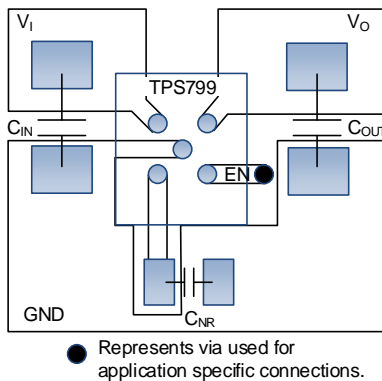


Figure 30. Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

提供了一个评估模块 (EVM)，您可以借此来对使用 TPS799 时的电路性能进行初始评估。可通过德州仪器 (TI) 网站上的产品文件夹申请获取 TPS799 评估模块 (EVM)，也可以[直接从 TI 网上商店](#)购买。

11.1.1.2 Spice 模型

分析模拟电路和系统的性能时，使用 SPICE 模型对电路性能进行计算机仿真非常有用。您可以从产品文件夹中的仿真模型下获取 TPS799 的 SPICE 模型。

11.2 文档支持

11.2.1 相关文档

相关文档如下：

- 应用报告：《使用新的热度量指标》，[SBVA025](#)
- 应用报告：《IC 封装热度量指标》，[SPRA953](#)
- 《TPS799xxEVM-105 用户指南》，[SLVU130](#)

11.3 接收文档更新通知

要接收文档更新通知，请转至 TI.com 上的器件产品文件夹。单击右上角的[通知我](#)进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

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设计支持 TI 参考设计支持 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79901MDRVTEP	ACTIVE	WSO	DRV	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	17L	Samples
V62/17614-01XE	ACTIVE	WSO	DRV	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	17L	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79901MDRVTEP	WSO	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

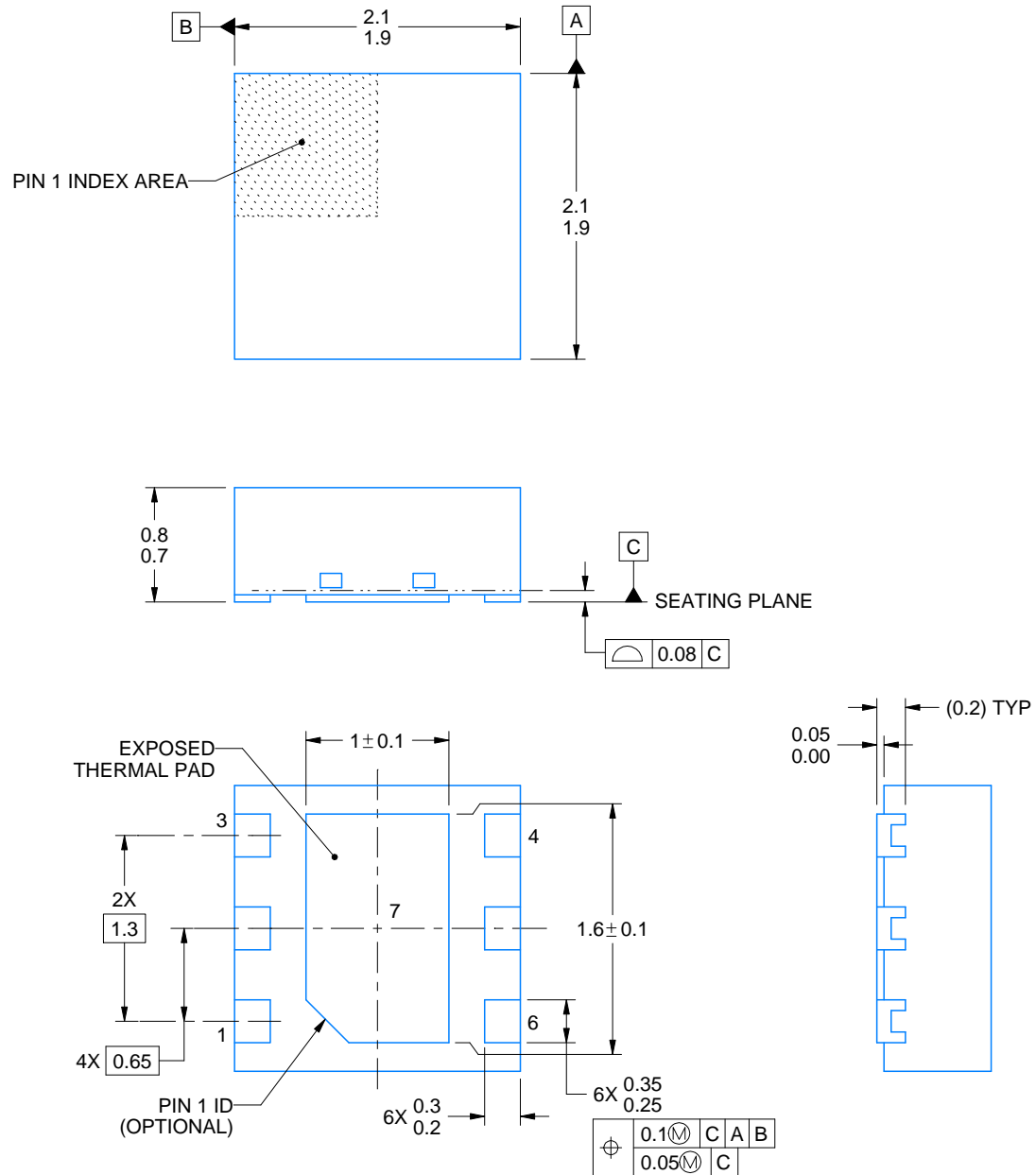
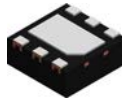


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79901MDRVTEP	WSON	DRV	6	250	200.0	183.0	25.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

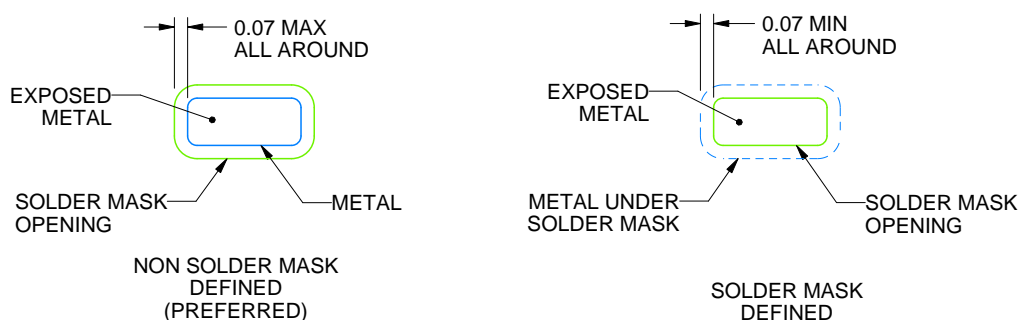
DRV0006D

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

4225563/A 12/2019

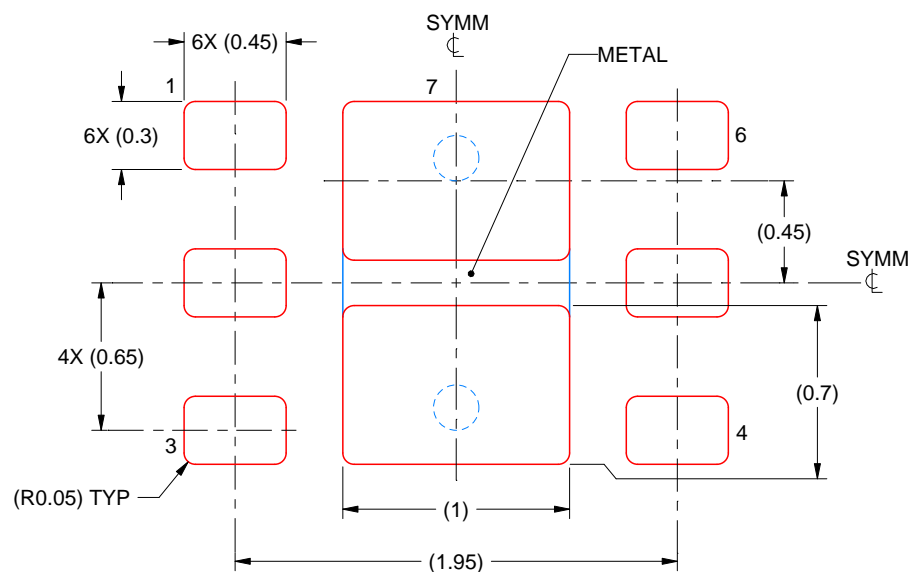
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

DRV0006D

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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