TEXAS INSTRUMENTS

TPS7A4501, TPS7A4515, TPS7A4518, TPS7A4525, TPS7A4533

SLVS720F – JUNE 2008 – REVISED NOVEMBER 2015

TPS7A45xx Low-Noise Fast-Transient-Response 1.5-A Low-Dropout Voltage Regulators

1 Features

- Optimized for Fast Transient Response
- Output Current: 1.5 A
- High Output Voltage Accuracy: 1% at 25°C
- Dropout Voltage: 300 mV
- Low Noise: 35 μV_{RMS} (10 Hz to 100 kHz)
- High Ripple Rejection: 68 dB at 1 kHz
- 1-mA Quiescent Current
- No Protection Diodes Needed
- Controlled Quiescent Current in Dropout
- Fixed Output Voltages: 1.5 V, 1.8 V, 2.5 V, 3.3 V
- Adjustable Output from 1.21 V to 20 V (TPS7A4501 Only)
- Less Than 1-µA Quiescent Current in Shutdown
- Stable With 10-µF Ceramic Output Capacitor
- Reverse-Battery Protection
- Reverse Current Protection

2 Applications

- Industrial
- Wireless Infrastructure
- Radio-Frequency Systems

3 Description

The TPS7A45xx devices are low-dropout (LDO) regulators optimized for fast transient response. The device can supply 1.5 A of output current with a dropout voltage of 300 mV. Operating quiescent current is 1 mA, dropping to less than 1 µA in shutdown. Quiescent current is well controlled; it does not rise in dropout as with many other regulators. In addition to fast transient response, the TPS7A45xx regulators have very-low output noise, which makes them ideal for sensitive RF supply applications.

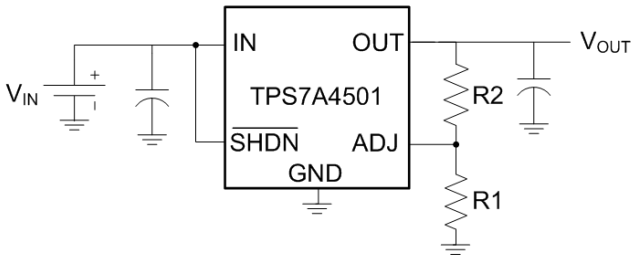
Output voltage range is from 1.21 to 20 V. The TPS7A45xx regulators are stable with output capacitance as low as 10 µF. Small ceramic capacitors can be used without the necessary addition of ESR as is common with other regulators. Internal protection circuitry includes reverse-battery protection, current limiting, thermal limiting, and reverse-current protection. The devices are available in fixed output voltages of 1.5 V, 1.8 V, 2.5 V, 3.3 V, and as an adjustable device with a 1.21-V reference voltage.

Device Information(1)

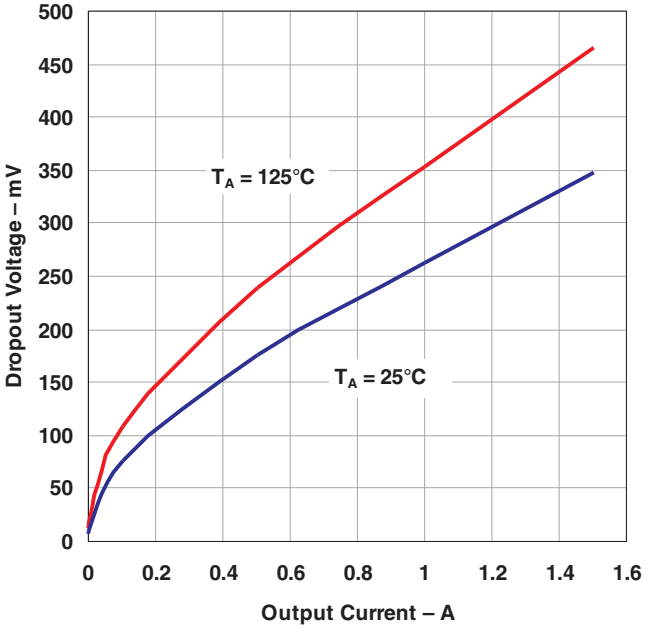
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A45xx	SOT-223 (6)	6.50 mm × 7.06 mm
	TO-263 (5)	10.16 mm × 15.24 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Dropout Voltage vs Output Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (August 2014) to Revision F — **Page**

- Corrected the body sizes listed for the packages ... 1
- Moved T_{stg} to *Absolute Maximum Ratings* table and changed *Handling Ratings* to *ESD Ratings* table ... 4
- Relocated *Thermal Considerations* and *Calculating Junction Temperature* to *Layout* ... 24
- Added *Community Resources* ... 26

Changes from Revision D (August 2011) to Revision E — **Page**

- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision C (December 2010) to Revision D — **Page**

- Replaced the *Dissipation Ratings* table with the *Thermal Information* table ... 5

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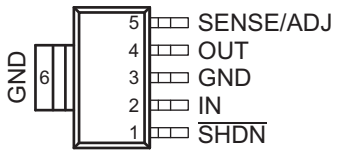
5 Device Comparison Table

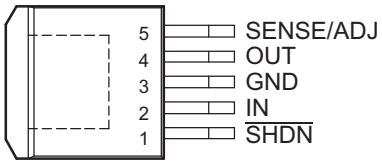
DEVICE	OUTPUT VOLTAGE	PIN 5
TPS7A4501	Adjustable	ADJ
TPS7A4515	1.5 V	SENSE
TPS7A4518	1.8 V	SENSE
TPS7A4525	2.5 V	SENSE
TPS7A4533	3.3 V	SENSE

6 Pin Configuration and Functions

DCQ Package
6-Pin SOT-223
Top View



KTT Package
6-Pin TO-263
Top View



Pin Functions

PIN		DESCRIPTION
NO.	NAME	
1	$\overline{\text{SHDN}}$	Shutdown. $\overline{\text{SHDN}}$ is used to put the TPS7A45xx regulators into a low-power shutdown state. The output is off when $\overline{\text{SHDN}}$ is pulled low. $\overline{\text{SHDN}}$ can be driven by 5-V logic, 3-V logic or open-collector logic with a pullup resistor. The pullup resistor is required to supply the pullup current of the open-collector gate, normally several microamperes, and $\overline{\text{SHDN}}$ current, typically 3 µA. If unused, $\overline{\text{SHDN}}$ must be connected to V_{IN}. The device is in the low-power shutdown state if $\overline{\text{SHDN}}$ is not connected.
2	IN	Input. Power is supplied to the device through IN. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor (ceramic) in the range of 1 µF to 10 µF is sufficient. The TPS7A45xx regulators are designed to withstand reverse voltages on IN with respect to ground and on OUT. In the case of a reverse input, which can happen if a battery is plugged in backwards, the device acts as if there is a diode in series with its input. There is no reverse current flow into the regulator, and no reverse voltage appears at the load. The device protects both itself and the load.
3	GND	Ground. For the KTT package, the exposed thermal pad is connected to GND and must be soldered to the PCB for rated thermal performance.
4	OUT	Output. The output supplies power to the load. A minimum output capacitor (ceramic) of 10 µF is required to prevent oscillations. Larger output capacitors are required for applications with large transient loads to limit peak voltage transients.
5	ADJ	Adjust. For the adjustable version only (TPS7A4501), this is the input to the error amplifier. ADJ is internally clamped to ±7 V. It has a bias current of 3 µA that flows into the pin. ADJ voltage is 1.21 V referenced to ground, and the output voltage range is 1.21 V to 20 V.
5	SENSE	Sense. For fixed-voltage versions (TPS7A4515, TPS7A4518, TPS7A4525, and TPS7A4533), SENSE is the input to the error amplifier. Optimum regulation is obtained at the point where SENSE is connected to the OUT pin of the regulator. In critical applications, small voltage drops are caused by the resistance (R_P) of PCB traces between the regulator and the load. These may be eliminated by connecting SENSE to the output at the load as shown in Figure 32. Note that the voltage drop across the external PCB traces adds to the dropout voltage of the regulator. SENSE bias current is 600 µA at the rated output voltage. SENSE can be pulled below ground (as in a dual supply system in which the regulator load is returned to a negative supply) and still allow the device to start and operate.
6	GND	Ground. DCQ package only.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating virtual-junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage, V_{IN}	IN	–20	20	V
	OUT	–20	20	
	Input-to-output differential (2)	–20	20	
	SENSE	–20	20	
	ADJ	–7	7	
	$\overline{SHDN}$	–20	20	
Output short-circuit duration, t_{short}			Indefinite	
Maximum lead temperature (10-s soldering time), T_{lead}			300	°C
Maximum junction temperature, T_{JMAX}			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to conditions beyond the recommended operating maximum for extended periods may affect device reliability.
(2) Absolute maximum input-to-output differential voltage cannot be achieved with all combinations of rated IN pin and OUT pin voltages. With the IN pin at 20 V, the OUT pin may not be pulled below 0 V. The total measured voltage from IN to OUT can not exceed ±20 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 1000 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage range (1)	V_{OUT} + V_{DO}	20	V
V_{IH}	SHDN high-level input voltage	2	20	V
V_{IL}	SHDN low-level input voltage		0.25	V
T_J	Recommended operating junction temperature range	–40	125	°C

(1) TPS7A4501, TPS7A4515, and TPS7A4518 may require a higher minimum input voltage under some output voltage/load conditions as indicated under *Electrical Characteristics*.

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7.4 Thermal Information

THERMAL METRIC (1) (2)		TPS7A45xx		UNIT
		KTT (TO-263)	DCQ (SOT-223)	
		5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28.0	50.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.0	31.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.4	5.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.9	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.4	5.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.3	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

7.5 Electrical Characteristics

Over recommended operating temperature range T_J = –40 to 125°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_J	MIN	TYP (2)	MAX	UNIT
V_{IN}	Minimum input voltage (3) (4)	I_{LOAD} = 0.5 A		25°C		1.9		V
		I_{LOAD} = 1.5 A		Full range		2.1	2.5	
V_{OUT}	Regulated output voltage (5)	TPS7A4515	V_{IN} = 2.21 V, I_{LOAD} = 1 mA	25°C	1.485	1.5	1.515	V
			V_{IN} = 2.5 V to 20 V, I_{LOAD} = 1 mA to 1.5 A	Full range	1.447	1.5	1.545	
		TPS7A4518	V_{IN} = 2.3 V, I_{LOAD} = 1 mA	25°C	1.782	1.8	1.818	
			V_{IN} = 2.8 V to 20 V, I_{LOAD} = 1 mA to 1.5 A	Full range	1.737	1.8	1.854	
		TPS7A4525	V_{IN} = 3 V, I_{LOAD} = 1 mA	25°C	2.475	2.5	2.525	
			V_{IN} = 3.5 V to 20 V, I_{LOAD} = 1 mA to 1.5 A	Full range	2.412	2.5	2.575	
		TPS7A4533	V_{IN} = 3.8 V, I_{LOAD} = 1 mA	25°C	3.266	3.3	3.333	
			V_{IN} = 4.3 V to 20 V, I_{LOAD} = 1 mA to 1.5 A	Full range	3.2	3.3	3.4	
V_{ADJ}	ADJ pin voltage (3) (5)	TPS7A4501	V_{IN} = 2.21 V, I_{LOAD} = 1 mA	25°C	1.197	1.21	1.222	V
			V_{IN} = 2.5 V to 20 V, I_{LOAD} = 1 mA to 1.5 A	Full range	1.174	1.21	1.246	
	Line regulation	TPS7A4515	ΔV_{IN} = 2.21 V to 20 V, I_{LOAD} = 1 mA	Full range		2	6	mV
		TPS7A4518	ΔV_{IN} = 2.3 V to 20 V, I_{LOAD} = 1 mA	Full range		2.5	7	
		TPS7A4525	ΔV_{IN} = 3 V to 20 V, I_{LOAD} = 1 mA	Full range		3	10	
		TPS7A4533	ΔV_{IN} = 3.8 V to 20 V, I_{LOAD} = 1 mA	Full range		3.5	10	
		TPS7A4501 (3)	ΔV_{IN} = 2.21 V to 20 V, I_{LOAD} = 1 mA	Full range		1.5	3	

(1) The TPS7A45xx regulators are tested and specified under pulse load conditions such that $T_J \approx T_A$. They are fully tested at T_A = 25°C. Performance at –40 and 125°C is specified by design, characterization, and correlation with statistical process controls.
(2) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
(3) The TPS7A4501 is tested and specified for these conditions with the ADJ pin connected to the OUT pin.
(4) For the TPS7A4501, TPS7A4515 and TPS7A4518, dropout voltages are limited by the minimum input voltage specification under some output voltage/load conditions.
(5) Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.

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Electrical Characteristics (continued)

Over recommended operating temperature range T_J = –40 to 125°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_J	MIN	TYP (2)	MAX	UNIT
	Load regulation	TPS7A4515	V_{IN} = 2.5 V, ΔI_{LOAD} = 1 mA to 1.5 A	25°C		2	9	mV
				Full range			18	
		TPS7A4518	V_{IN} = 2.8 V, ΔI_{LOAD} = 1 mA to 1.5 A	25°C		2	10	
				Full range			20	
		TPS7A4525	V_{IN} = 3.5 V, ΔI_{LOAD} = 1 mA to 1.5 A	25°C		2.5	15	
				Full range			30	
		TPS7A4533	V_{IN} = 4.3 V, ΔI_{LOAD} = 1 mA to 1.5 A	25°C		3	20	
				-40 to +85 °C			30	
				Full range			70	
		TPS7A4501 (3)	V_{IN} = 2.5 V, ΔI_{LOAD} = 1 mA to 1.5 A	25°C		2	8	
				-40 to +85 °C			8	
				Full range			18	
V_{DO}	Dropout voltage (4) (6) (7) $V_{IN} = V_{OUT(NOMINAL)}$	I_{LOAD} = 1 mA		25°C		0.02	0.05	V
				Full range			0.06	
		I_{LOAD} = 100 mA		25°C		0.085	0.10	
				Full range			0.13	
		I_{LOAD} = 500 mA		25°C		0.17	0.180	
				Full range			0.250	
		I_{LOAD} = 1.5 A		25°C		0.300	0.350	
				Full range			0.450	
I_{GND}	GND pin current (7) (8) $V_{IN} = V_{OUT(NOMINAL)}$ + 1	I_{LOAD} = 0 mA		Full range		1	1.5	mA
		I_{LOAD} = 1 mA		Full range		1.1	1.6	
		I_{LOAD} = 100 mA		Full range		3.3	3.5	
		I_{LOAD} = 500 mA		Full range		15	17	
		I_{LOAD} = 1.5 A		Full range		80	90	
e_N	Output voltage noise	C_{OUT} = 10 µF, I_{LOAD} = 1.5 A, B_W = 10 Hz to 100 kHz		25°C		35		μV_{RMS}
I_{ADJ}	ADJ pin bias current (3) (9)			25°C		3	7	µA
	Shutdown threshold	V_{OUT} = OFF to ON		Full range		0.9	2	V
		V_{OUT} = ON to OFF		Full range	0.25	0.75		
$I_{\overline{SHDN}}$	$\overline{SHDN}$ pin current	$V_{\overline{SHDN}}$ = 0 V		25°C		0.01	1	µA
		$V_{\overline{SHDN}}$ = 20 V		25°C		3	20	
	Quiescent current in shutdown	V_{IN} = 6 V, $V_{\overline{SHDN}}$ = 0 V		25°C		0.01	1	µA
	Ripple rejection	$V_{IN} – V_{OUT}$ = 1.5 V (avg), V_{RIPPLE} = 0.5 V_{P-P}, f_{RIPPLE} = 120 Hz, I_{LOAD} = 0.75 A		25°C		68		dB
I_{LIMIT}	Current limit	V_{IN} = 7 V, V_{OUT} = 0 V		25°C		2		A
		$V_{IN} = V_{OUT(NOMINAL)}$ + 1		Full range	1.6			
I_{IL}	Input reverse leakage current	V_{IN} = –20 V, V_{OUT} = 0 V		Full range			300	µA

(6) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is equal to: $V_{IN} – V_{DROPOUT}$.
(7) To satisfy requirements for minimum input voltage, the TPS7A4501 is tested and specified for these conditions with an external resistor divider (two 4.12-kΩ resistors) for an output voltage of 2.4 V. The external resistor divider adds a 300-µA DC load on the output.
(8) GND pin current is tested with V_{IN} = ($V_{OUT(NOMINAL)}$ + 1 V) and a current source load. The GND pin current decreases at higher input voltages.
(9) ADJ pin bias current flows into the ADJ pin.

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Electrical Characteristics (continued)

Over recommended operating temperature range T_J = –40 to 125°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_J	MIN	TYP (2)	MAX	UNIT
I_{RO}	Reverse output current (10)	TPS7A4515	V_{OUT} = 1.5 V, V_{IN} < 1.5 V	25°C		600	1000	µA
		TPS7A4518	V_{OUT} = 1.8 V, V_{IN} < 1.8 V	25°C		600	1000	
		TPS7A4525	V_{OUT} = 2.5 V, V_{IN} < 2.5 V	25°C		600	1000	
		TPS7A4533	V_{OUT} = 3.3 V, V_{IN} < 3.3 V	25°C		600	1000	
		TPS7A4501	V_{OUT} = 1.21 V, V_{IN} < 1.21 V	25°C		300	500	

(10) Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out the GND pin.

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7.6 Typical Characteristics

Typical characteristics apply to all TPS7A45xx devices unless otherwise noted.

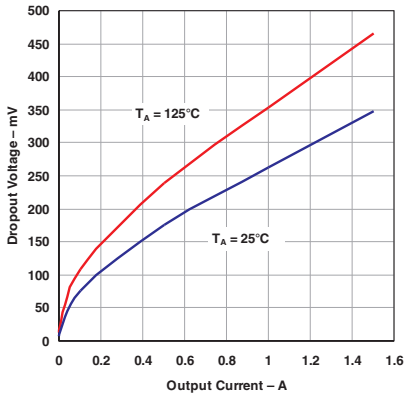


Figure 1. Dropout Voltage vs Output Current

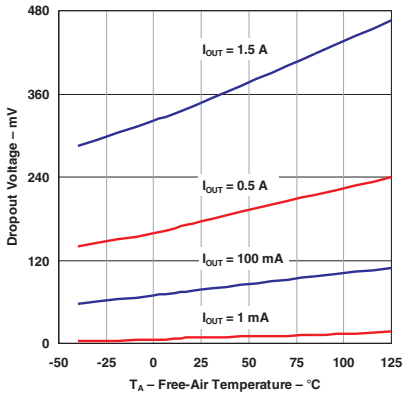
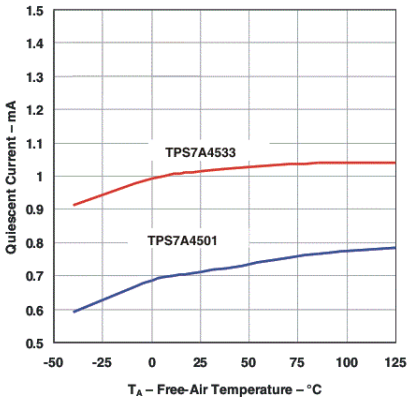
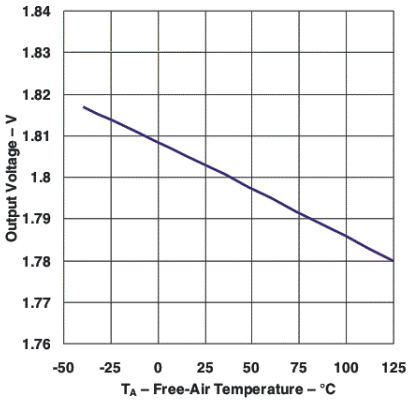


Figure 2. Dropout Voltage vs Temperature



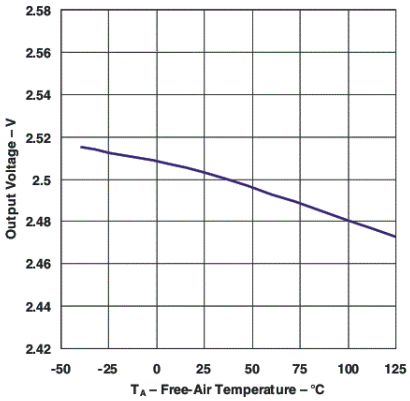
V_{IN} = 6 V I_{OUT} = 0 A V_{SHDN} = VIN

Figure 3. Quiescent Current vs Temperature



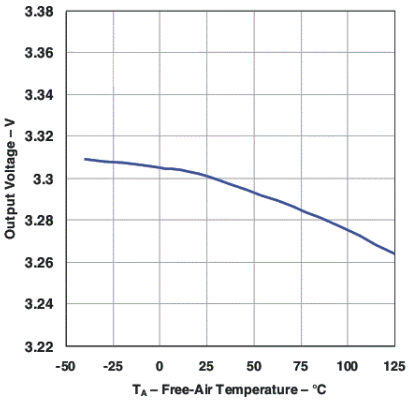
I_{OUT} = 1 mA TPS7A4518

Figure 4. TPS7A4518 Output Voltage vs Temperature



I_{OUT} = 1 mA TPS7A4525

Figure 5. TPS7A4525 Output Voltage vs Temperature



I_{OUT} = 1 mA TPS7A4533

Figure 6. TPS7A4533 Output Voltage vs Temperature

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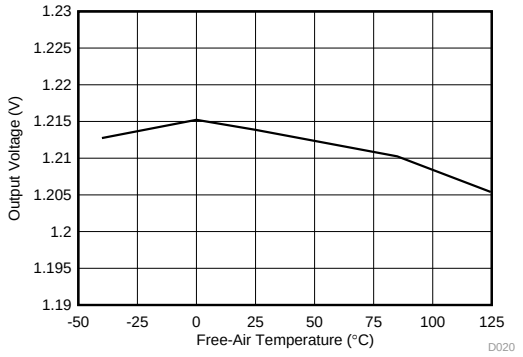
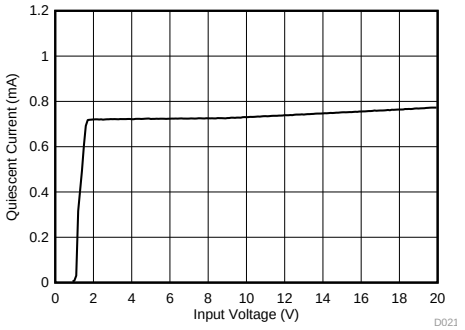
Typical Characteristics (continued)

Typical characteristics apply to all TPS7A45xx devices unless otherwise noted.



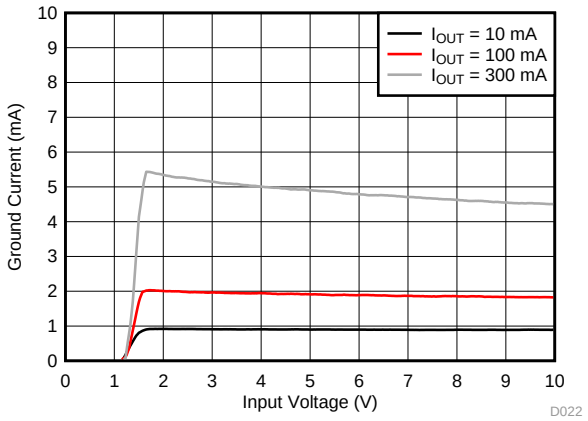
I_{OUT} = 1 mA V_{IN} = 6 V

Figure 7. TPS7A4501 Output Voltage vs Temperature



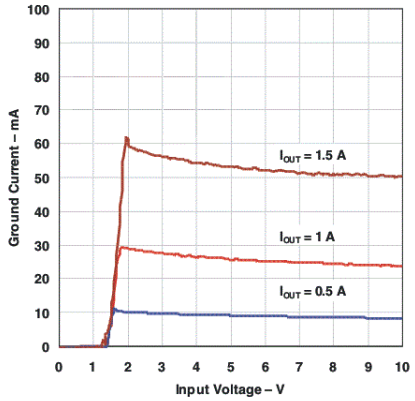
T_J = 25°C R_{OUT} = 4.3 kΩ
V_{SHDN} = V_{IN}

Figure 8. Quiescent Current vs Input Voltage



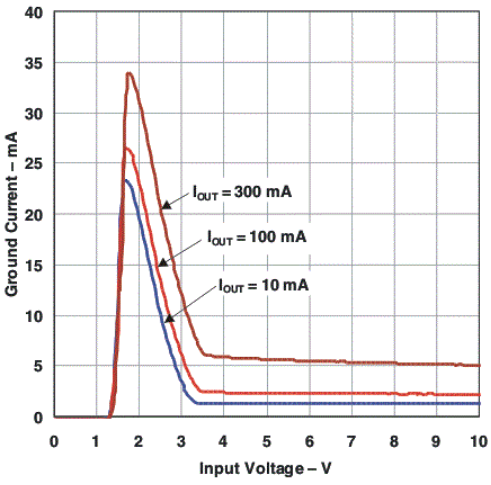
T_J = 25°C V_{OUT} = 1.21 V
V_{SHDN} = V_{IN}

Figure 9. TPS7A4501 Ground Current vs Input Voltage



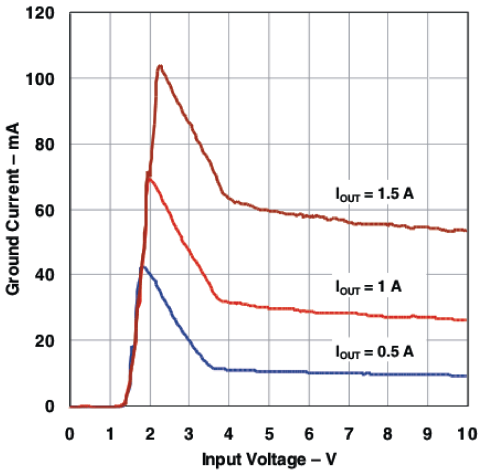
T_J = 25°C V_{OUT} = 1.21 V
V_{SHDN} = V_{IN}

Figure 10. TPS7A4501 Ground Current vs Input Voltage



T_J = 25°C V_{SHDN} = V_{IN}

Figure 11. TPS7A4533 Ground Current vs Input Voltage



T_J = 25°C V_{SHDN} = V_{IN}

Figure 12. TPS7A4533 Ground Current vs Input Voltage

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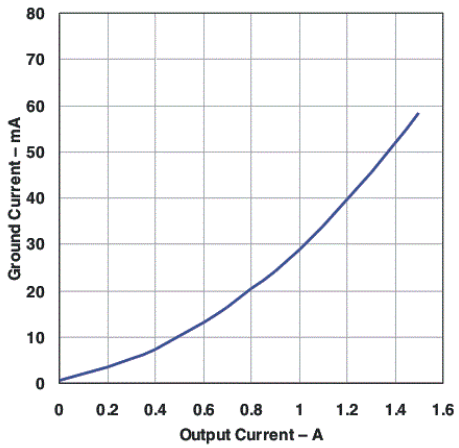
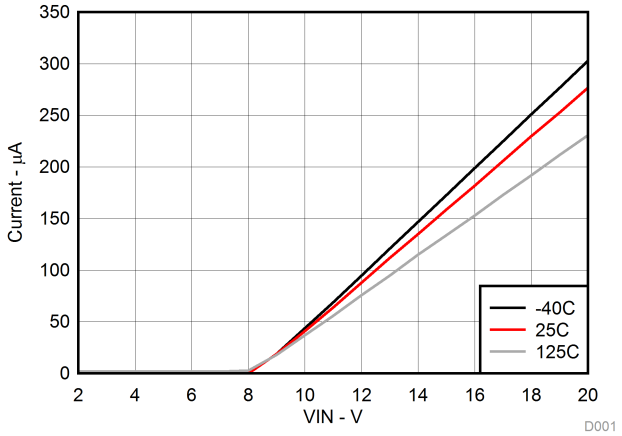
Typical Characteristics (continued)

Typical characteristics apply to all TPS7A45xx devices unless otherwise noted.



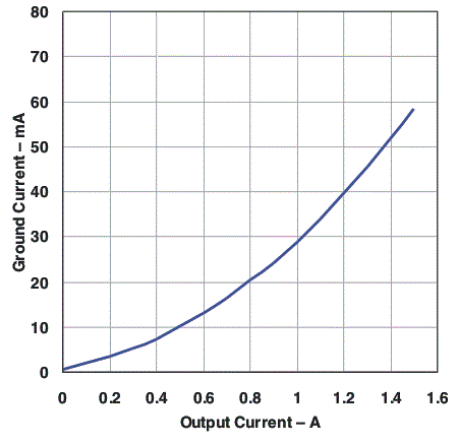
$V_{IN} = V_{OUT}(nom) + 1$

Figure 13. Ground Current vs Output Current



$V_{SHDN} = 0$ V

Figure 14. Quiescent Current in Shutdown vs Input Voltage



$V_{SHON} = 0$ V

Figure 15. $\overline{SHDN}$ Pin Current (I_{SHDN}) vs Temperature

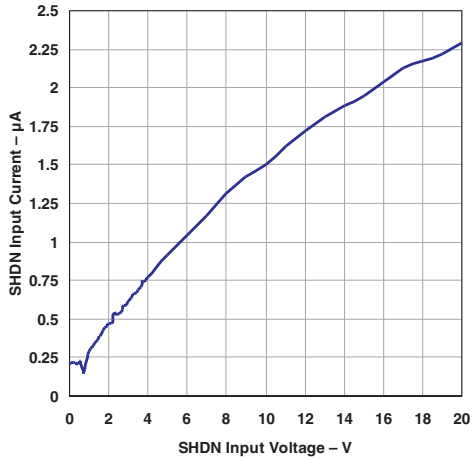
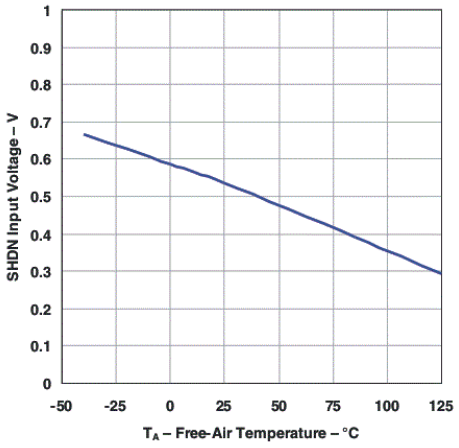
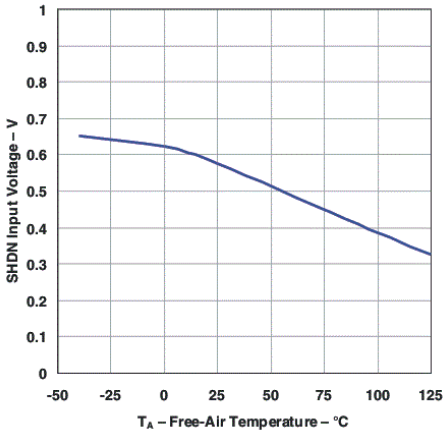


Figure 16. $\overline{SHDN}$ Pin Current (I_{SHDN}) vs $\overline{SHDN}$ Input Voltage



$I_{OUT} = 1$ mA

Figure 17. $\overline{SHDN}$ Threshold (OFF to ON) vs Temperature



$I_{OUT} = 1$ mA

Figure 18. $\overline{SHDN}$ Threshold (ON to OFF) vs Temperature

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Typical Characteristics (continued)

Typical characteristics apply to all TPS7A45xx devices unless otherwise noted.

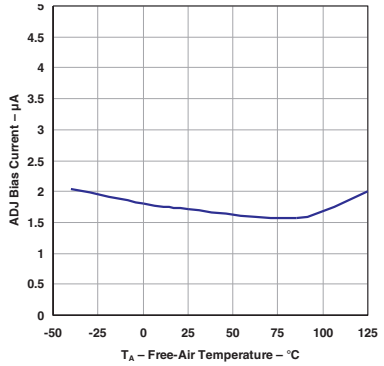
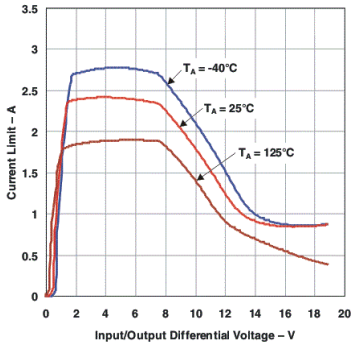
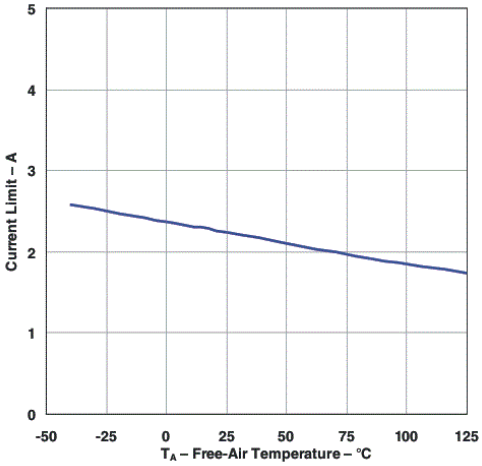


Figure 19. ADJ Bias Current vs Temperature



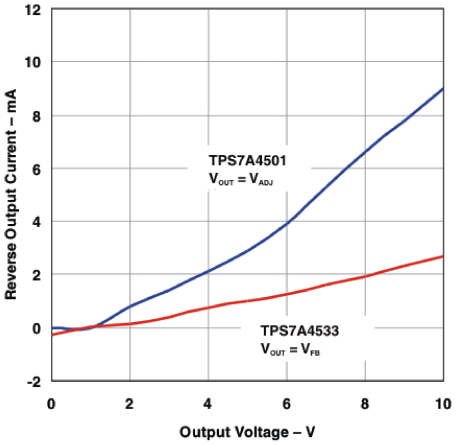
ΔV_{OUT} = 100 mV

Figure 20. Current Limit vs Input-to-Output Differential Voltage



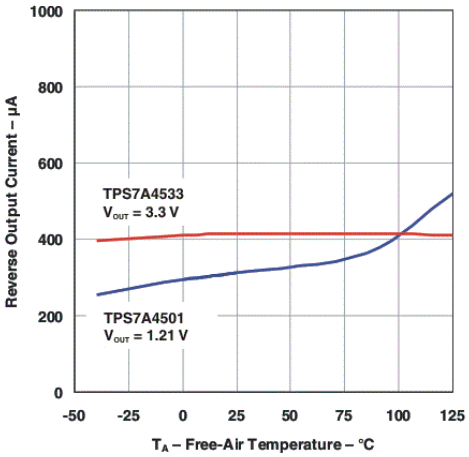
V_{IN} = 7 V V_{OUT} = 0 V

Figure 21. Current Limit vs Temperature



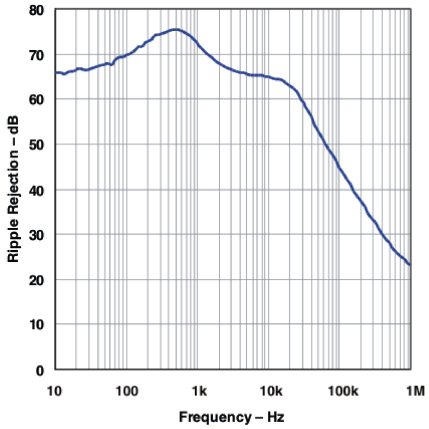
T_J = 25°C V_{IN} = 0 V
Current flows into OUT pin

Figure 22. Reverse Output Current vs Output Voltage



V_{IN} = 0 V

Figure 23. Reverse Output Current vs Temperature



V_{RIPPLE} = 0.05 V_{PP} C_{IN} = 0 T_A = 25°C
V_{IN} = 2.7 V C_{OUT} = 10 µF (ceramic)

Figure 24. Ripple Rejection vs Frequency

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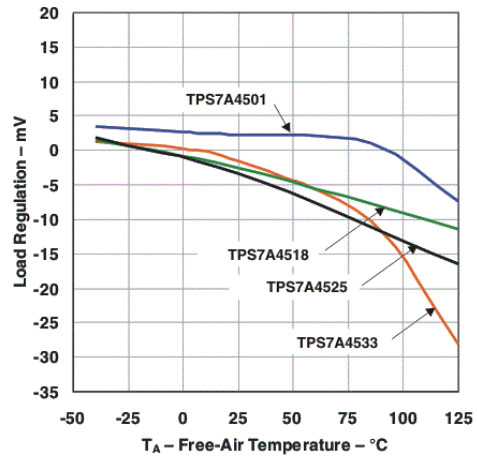
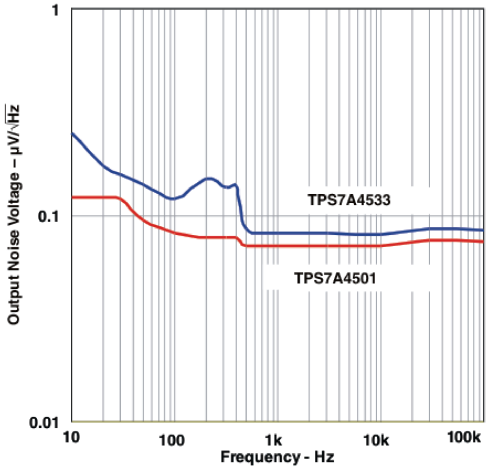
Typical Characteristics (continued)

Typical characteristics apply to all TPS7A45xx devices unless otherwise noted.



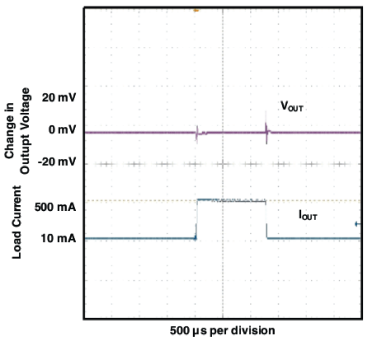
I_{OUT} = 1.5 A

Figure 25. Load Regulation vs Temperature



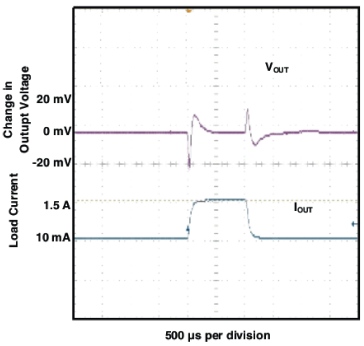
C_{OUT} = 10 µF (ceramic) I_{OUT} = 1.5 A

Figure 26. Output Noise Voltage vs Frequency



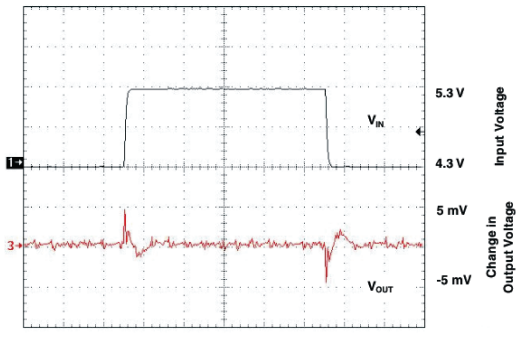
V_{IN} = 4.3 V C_{IN} = 10 µF
C_{OUT} = 10 µF (ceramic)

Figure 27. Load Transient Response



V_{IN} = 4.3 V C_{IN} = 10 µF
C_{OUT} = 10 µF (ceramic)

Figure 28. Load Transient Response



I_{OUT} = 1.5 A C_{IN} = 10 µF
C_{OUT} = 10 µF (ceramic)

Figure 29. Line Transient Response

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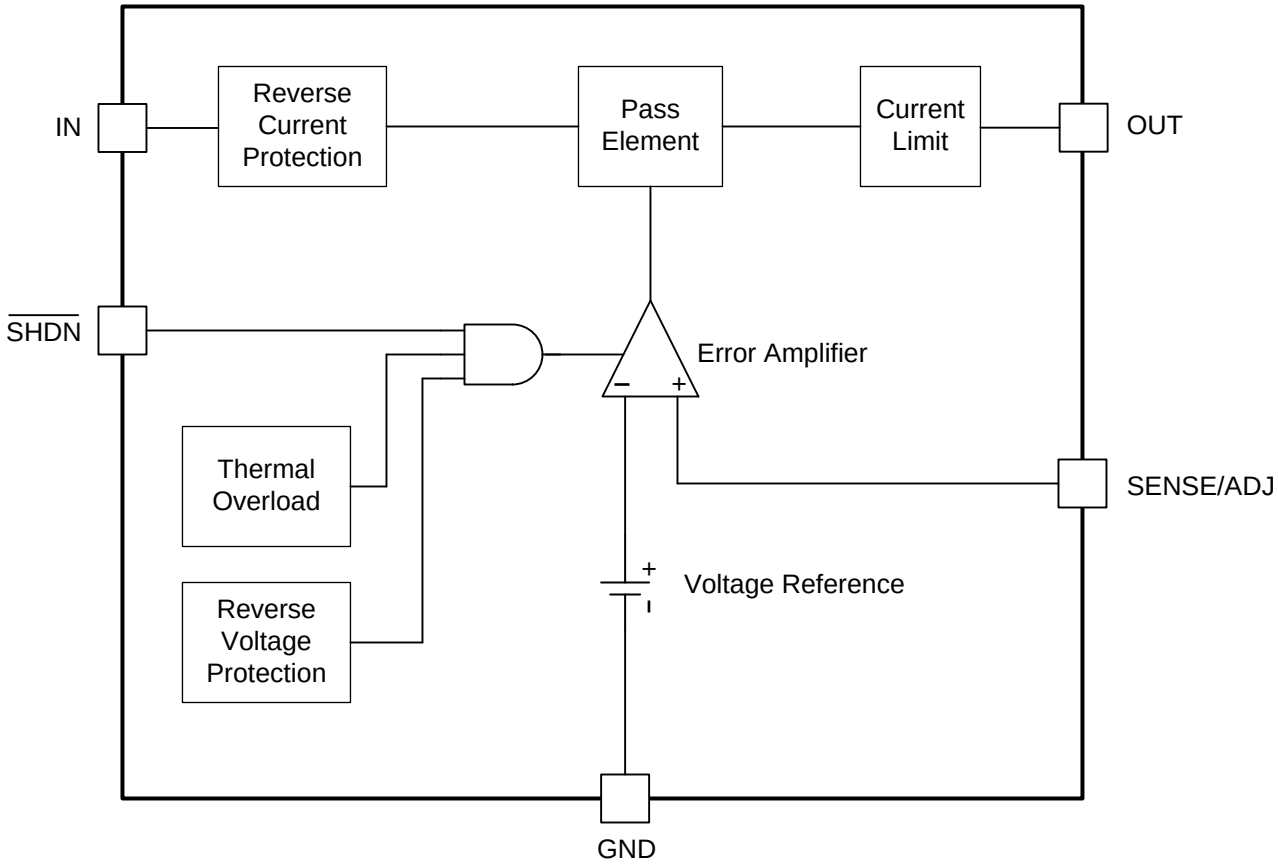
8 Detailed Description

8.1 Overview

The TPS7A45xx series are 1.5-A low-dropout regulators optimized for fast transient response. The devices are capable of supplying 1.5 A at a dropout voltage of 300 mV. The low operating quiescent current (1 mA) drops to less than 1 µA in shutdown. In addition to the low quiescent current, the TPS7A45xx regulators incorporate several protection features that make them ideal for use in battery-powered systems. The devices are protected against both reverse input and reverse output voltages. In battery-backup applications where the output can be held up by a backup battery when the input is pulled to ground, the TPS7A45xx acts as if it has a diode in series with its output and prevents reverse current flow. Additionally, in dual-supply applications where the regulator load is returned to a negative supply, the output can be pulled below ground by as much as (20 V – VIN) and still allow the device to start and operate.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Adjustable Operation

The TPS7A4501 has an adjustable output voltage range of 1.21 V to 20 V. The output voltage is set by the ratio of two external resistors as shown in Figure 30. The device maintains the voltage at the ADJ pin at 1.21 V referenced to ground. The current in R1 is then equal to (1.21 V/R1), and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 3 µA at 25°C, flows through R2 into the ADJ pin. The output voltage can be calculated using the formula shown in Equation 1. The value of R1 should be less than 4.17 kΩ to minimize errors in the output voltage caused by the ADJ pin bias current. Note that in shutdown the output is turned off, and the divider current is zero.

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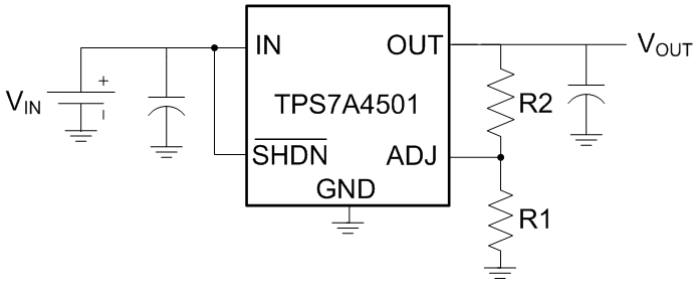

Figure 30. Adjustable Operation

The output voltage can be set using the following equations:

$$V_{OUT} = 1.21V(1+\frac{R2}{R1}) + I_{ADJ} \times R2 \quad (1)$$

V_{ADJ} = 1.21 V (2)

I_{ADJ} = 3 µA at 25°C (3)

Output Range = 1.21 to 20 V (4)

8.3.2 Fixed Operation

The TPS7A45xx can be used in a fixed voltage configuration. The SENSE/ADJ pin should be connected to OUT for proper operation. An example of this is shown in Figure 31. The TPS7A4501 can also be used in this configuration for a fixed output voltage of 1.21 V.

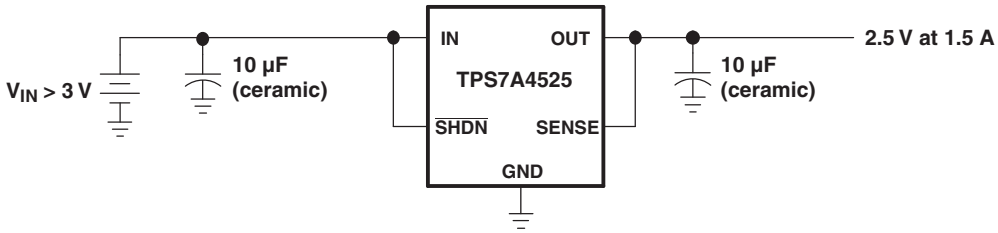

Figure 31. 3.3 to 2.5 V Regulator

During fixed voltage operation, the SENSE/ADJ pin can be used for a Kelvin connection if routed separately to the load. This allows the regulator to compensate for voltage drop across parasitic resistances (RP) between the output and the load. This becomes more crucial with higher load currents.

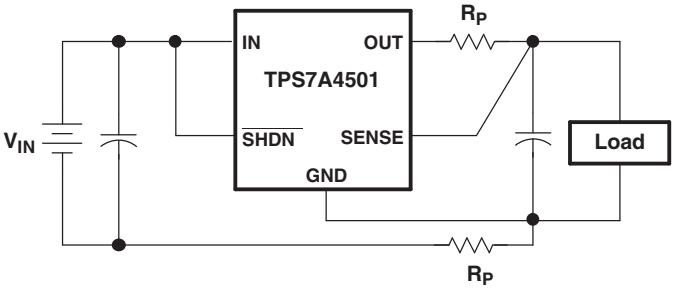

Figure 32. Kelvin Sense Connection

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8.3.3 Overload Recovery

Like many IC power regulators, the TPS7A45xx has safe operating area protection. The safe area protection decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During start up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein removal of an output short does not allow the output voltage to recover. Other regulators also exhibit this phenomenon, so it is not unique to the TPS7A45xx.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations occur immediately after the removal of a short circuit or when the shutdown pin is pulled high after the input voltage has already been turned on. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply may need to be cycled down to zero and brought up again to make the output recover.

8.3.4 Output Voltage Noise

The TPS7A45xx regulators have been designed to provide low output voltage noise over the 10-Hz to 100-kHz bandwidth while operating at full load. Output voltage noise is typically 35 nV/$\sqrt{\text{Hz}}$ over this frequency bandwidth for the TPS7A4501 (adjustable version). For higher output voltages (generated by using a resistor divider), the output voltage noise is gained up accordingly. This results in RMS noise over the 10-Hz to 100-kHz bandwidth of 14 μV_{RMS} for the TPS7A4501, increasing to 38 μV_{RMS} for the TPS7A4533.

Higher values of output voltage noise may be measured when care is not exercised with regard to circuit layout and testing. Crosstalk from nearby traces can induce unwanted noise onto the output of the TPS7A45xx. Power-supply ripple rejection must also be considered; the TPS7A45xx regulators do not have unlimited power-supply rejection and pass a small portion of the input noise through to the output.

8.3.5 Protection Features

The TPS7A45xx regulators incorporate several protection features which make them ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the devices are protected against reverse input voltages, reverse output voltages and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C.

The input of the device withstands reverse voltages of 20 V. Current flow into the device is limited to less than 1 mA (typically less than 100 µA), and no negative voltage appears at the output. The device protects both itself and the load. This provides protection against batteries that can be plugged in backward.

The output of the TPS7A45xx can be pulled below ground without damaging the device. If the input is left open circuit or grounded, the output can be pulled below ground by 20 V. For fixed voltage versions, the output acts like a large resistor, typically 5 kΩ or higher, limiting current flow to typically less than 600 µA. For adjustable versions, the output acts like an open circuit; no current flows out of the pin. If the input is powered by a voltage source, the output sources the short-circuit current of the device and protects itself by thermal limiting. In this case, grounding the $\overline{\text{SHDN}}$ pin turns off the device and stops the output from sourcing the short-circuit current.

The ADJ pin of the adjustable device can be pulled above or below ground by as much as 7 V without damaging the device. If the input is left open circuit or grounded, the ADJ pin acts like an open circuit when pulled below ground and like a large resistor (typically 5 kΩ) in series with a diode when pulled above ground.

In situations where the ADJ pin is connected to a resistor divider that would pull the ADJ pin above its 7-V clamp voltage if the output is pulled high, the ADJ pin input current must be limited to less than 5 mA. For example, a resistor divider is used to provide a regulated 1.5-V output from the 1.21-V reference when the output is forced to 20 V. The top resistor of the resistor divider must be chosen to limit the current into the ADJ pin to less than 5 mA when the ADJ pin is at 7 V. The 13-V difference between OUT and ADJ divided by the 5-mA maximum current into the ADJ pin yields a minimum top resistor value of 2.6 kΩ.

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In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open circuit.

When the IN pin of the TPS7A45xx is forced below the OUT pin or the OUT pin is pulled above the IN pin, input current typically drops to less than 2 µA. This can happen if the input of the device is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the SHDN pin has no effect on the reverse output current when the output is pulled above the input.

8.4 Device Functional Modes

Table 1 shows the functional modes for the TPS7A45xx.

Table 1. Device Modes

SHDN	DEVICE STATE
H	Regulated voltage
L	Shutdown

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some design considerations for implementing this device in various applications.

9.1.1 Output Capacitance and Transient Response

The TPS7A45xx regulators are designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 10 µF with an ESR of 3 Ω or less is recommended to prevent oscillations. Larger values of output capacitance can decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the TPS7A45xx, increase the effective output capacitor value.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients. When used with a 5-V regulator, a 10-µF Y5V capacitor can exhibit an effective value as low as 1 µF to 2 µF over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

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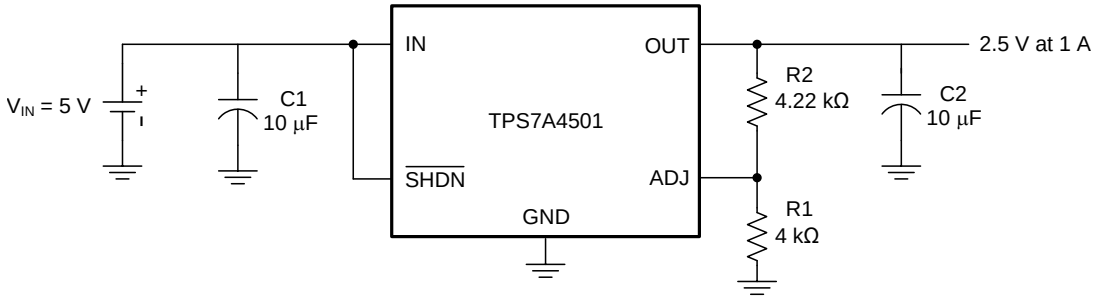
9.2 Typical Applications

9.2.1 Adjustable Output Operation



NOTE: All capacitors are ceramic.

Figure 33. Adjustable Output Voltage Operation

9.2.1.1 Design Requirements

Table 2 shows the design requirements.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage (V_{IN})	5.0 V
Output voltage (V_{OUT})	2.5 V
Output current (I_{OUT})	0 to 1 A
Load regulation	1%

9.2.1.2 Detailed Design Procedure

The TPS7A4501 has an adjustable output voltage range of 1.21 to 20 V. The output voltage is set by the ratio of two external resistors R1 and R2 as shown in Figure 33. The device maintains the voltage at the ADJ pin at 1.21 V referenced to ground. The current in R1 is then equal to (1.21 V/R1), and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 3 µA at 25°C, flows through R2 into the ADJ pin. The output voltage can be calculated using Equation 5.

$$V_{OUT} = 1.21V\left(1+\frac{R2}{R1}\right)+I_{ADJ}\times R2 \quad (5)$$

The value of R1 should be less than 4.17 kΩ to minimize errors in the output voltage caused by the ADJ pin bias current. Note that in shutdown the output is turned off, and the divider current is zero. For an output voltage of 2.50 V, R1 will be set to 4.0 kΩ. R2 is then found to be 4.22 kΩ using the equation above.

$$V_{OUT} = 1.21V\left(1+\frac{4.22k\Omega}{4.0k\Omega}\right)+3\mu A\times 4.22k\Omega \quad (6)$$

$$V_{OUT} = 2.50\ V \quad (7)$$

The adjustable device is tested and specified with the ADJ pin tied to the OUT pin for an output voltage of 1.21 V. Specifications for output voltages greater than 1.21 V are proportional to the ratio of the desired output voltage to 1.21 V: V_{OUT}/1.21 V. For example, load regulation for an output current change of 1 mA to 1.5 A is –2 mV (typ) at V_{OUT} = 1.21 V. At V_{OUT} = 2.50 V, the typical load regulation is:

(2.50 V/1.21 V)(–2 mV) = –4.13 mV (8)

Figure 34 shows the actual change in output is about 3 mV for a 1-A load step. The maximum load regulation at 25°C is –8 mV. At V_{OUT} = 2.50 V, the maximum load regulation is:

(2.50 V/1.21 V)(–8 mV) = –16.53 mV (9)

Because 16.53 mV is only 0.7% of the 2.5 V output voltage, the load regulation will meet the design requirements.

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9.2.1.3 Application Curve

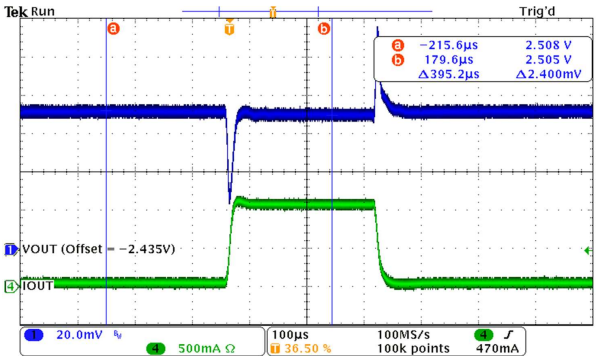
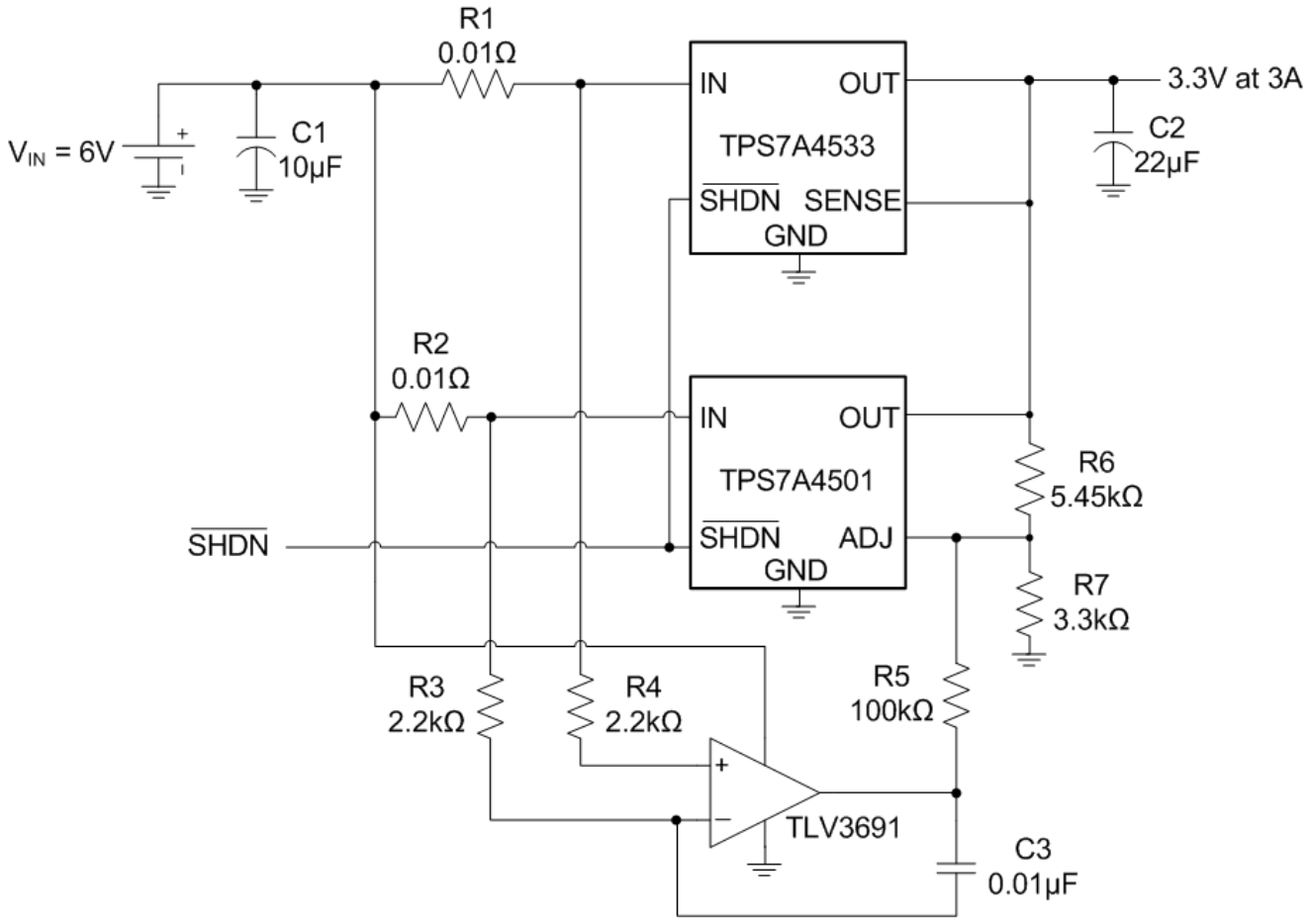


Figure 34. 1-A Load Transient Response

9.2.2 Paralleling Regulators for Higher Output Current



NOTE: All capacitors are ceramic.

Figure 35. Paralleling Regulators for Higher Output Current

9.2.2.1 Design Requirements

Table 3 shows the design requirements.

Table 3. Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage (V_{IN})	6.0 V
Output voltage (V_{OUT})	3.3 V
Output current (I_{OUT})	3.0 A

9.2.2.2 Detailed Design Procedure

In an application requiring higher output current, an adjustable output regular can be placed in parallel with a fixed output regulator to increase the current capacity. Two sense resistors and a comparator can be used to control the feedback loop of the adjustable regulator in order to balance the current between the two regulators.

In Figure 35 resistors R1 and R2 are used to sense the current flowing into each regulator and should have a very low resistance to avoid unnecessary power loss. R1 and R2 should have the same value and a tolerance of 1% or better so the current is shared equally between the regulators. For this example, a value of 0.01 Ω will be used.

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The TLV3691 rail-to-rail nanopower comparator output will alternate between VIN and GND depending on the currents flowing into each of the two regulators. To design this control circuit, begin by looking at the case where the two output currents are approximately equal and the comparator output is low. In this case, the output of the TPS7A4501 should be set the same as the fixed voltage regulator. The TPS7A4533 has a 3.3 V fixed output, so this will be the set point for the adjustable regulator. Begin by selecting a R7 value less than 4.17 kΩ. In this example, 3.3 kΩ will be used. R5 will need to have a high resistance to satisfy Equation 14, for this example 100 kΩ was chosen. Then find the parallel resistance of R5 and R7 since they are both connected from the ADJ pin to GND using Equation 10.

$$(R5 \,||\, R7) = \frac{R5 \times R7}{R5 + R7} = 3.19k\Omega \tag{10}$$

Once the R5 and R7 parallel resistance in calculated, the value for R6 can be found using Equation 11.

$$R6 = \frac{V_{OUT}}{1.22V}(R5 \,||\, R7) - (R5 \,||\, R7) \tag{11}$$

$$R6 = \frac{3.3V}{1.22V}\left(3.19k\Omega\right) - \left(3.19k\Omega\right) \tag{12}$$

$$R6 = 5.45\ k\Omega \tag{13}$$

In the case where the TPS7A4533 is sourcing more current than TPS7A4501, the comparator output will go high. This will lower the voltage at the ADJ pin causing the TPS7A4501 to try and raise the output voltage by sourcing more current. The TPS7A4533 will then react by sourcing less current to try and keep the output from rising. When the current through the TPS7A4533 becomes less than the TPS7A4501, the comparator output will return to GND. In order for this to happen, Equation 14 must be satisfied:

$$V_{IN}\left(\frac{R7}{R5 + R7}\right) + \left(V_{IN} - V_{OUT}\right)\left(\frac{R6}{R5 + R6}\right) < Vref \tag{14}$$

$$6V\left(\frac{3.3k\Omega}{100k\Omega + 3.3k\Omega}\right) + (2.7V)\left(\frac{5.45k\Omega}{100k\Omega + 5.45k\Omega}\right) < 1.21V \tag{15}$$

$$0.19\ V + 0.14\ V < 1.21\ V \tag{16}$$

$$0.33\ V < 1.21\ V \tag{17}$$

9.2.2.3 Application Curve

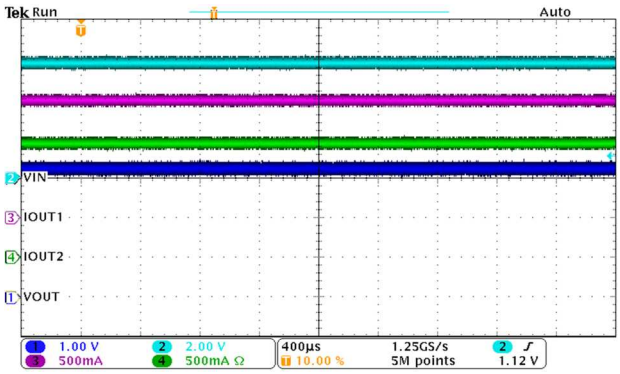

Figure 36. Parallel Regulators Sharing Load Current

10 Power Supply Recommendations

The device is designed to operate with an input voltage supply up to 20 V. The minimum input voltage should provide adequate headroom greater than the dropout voltage in order for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

11 Layout

11.1 Layout Guidelines

1. For best performance, all traces should be as short as possible.
2. Use wide traces for IN, OUT, and GND to minimize the parasitic electrical effects.
3. A minimum output capacitor of 10 µF with an ESR of 3 Ω or less is recommended to prevent oscillations. X5R and X7R dielectrics are preferred.
4. Place the Output Capacitor as close as possible to the OUT pin of the device.
5. The tab of the DCQ package should be connected to ground.
6. The exposed thermal pad of the KTT package should be connected to a wide ground plane for effective heat dissipation.

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11.2 Layout Example

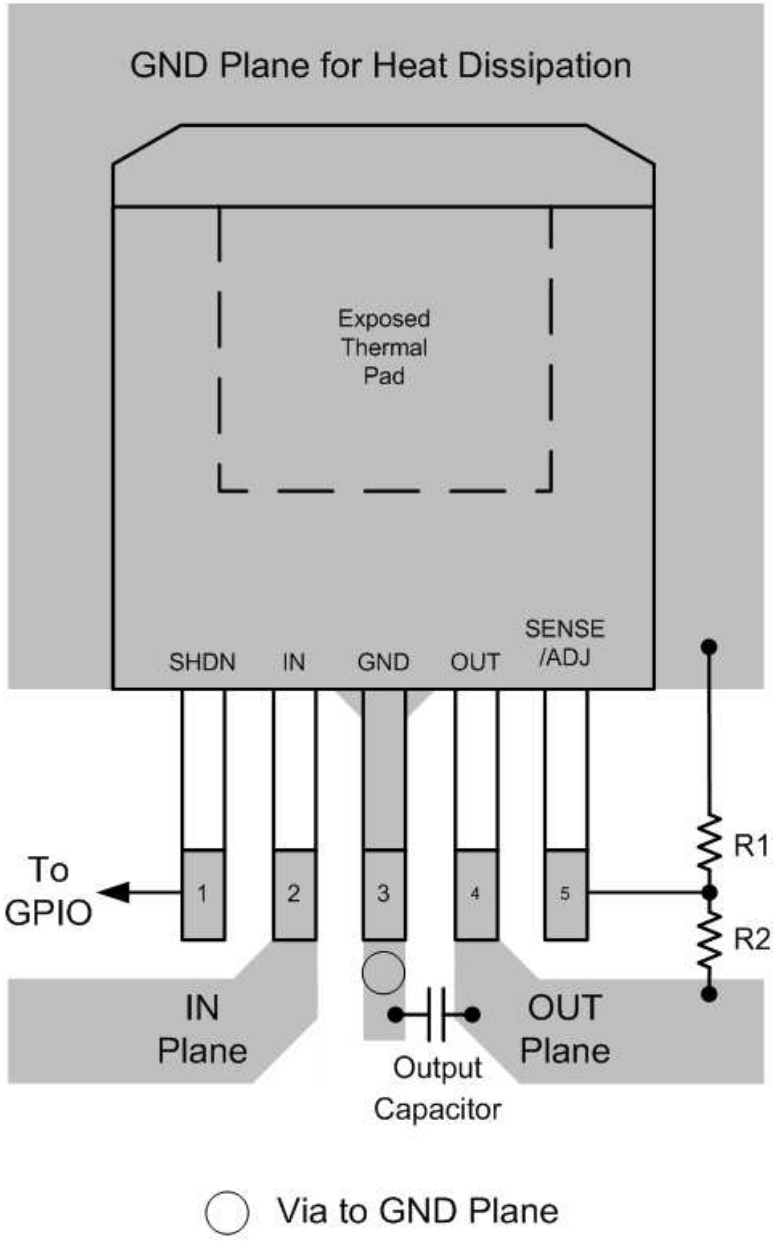

Figure 37. TO-263 Layout Example (KTT)

Layout Example (continued)

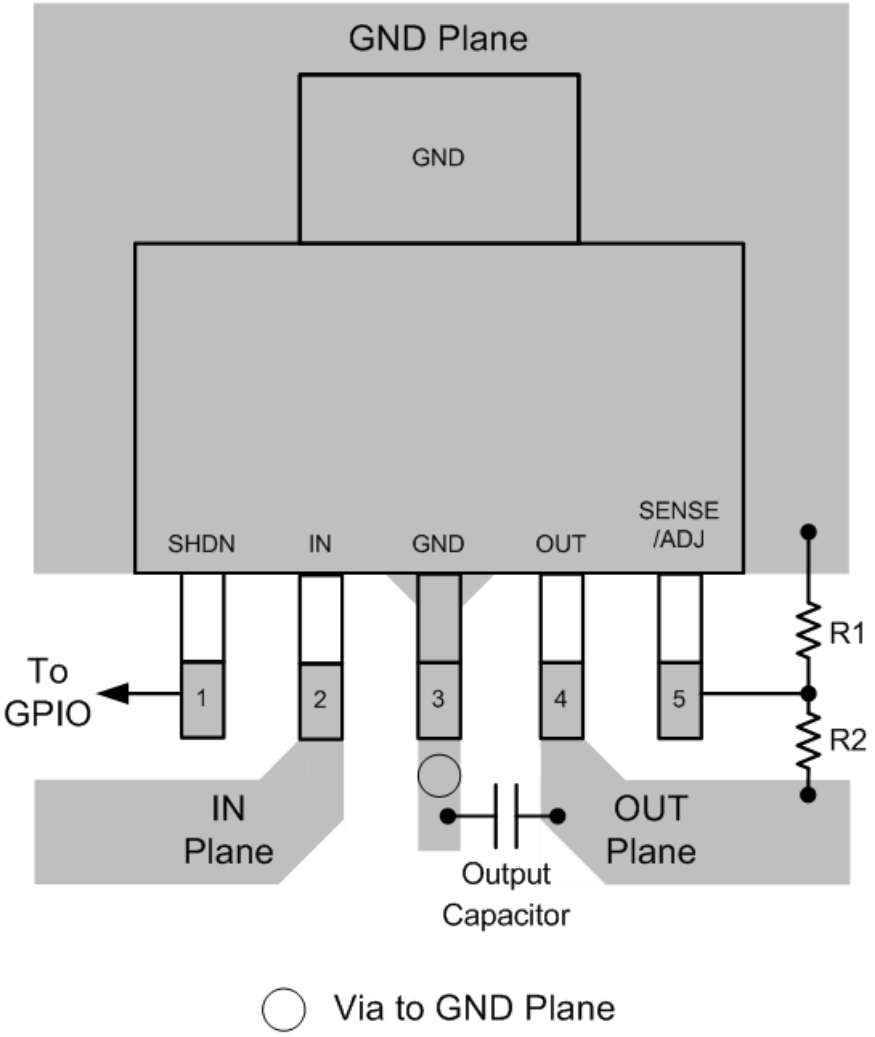

Figure 38. SOT-223 Layout Example (DCQ)

11.3 Thermal Considerations

The power handling capability of the device is limited by the recommended maximum operating junction temperature (125°C). The power dissipated by the device is made up of two components:

1. Output current multiplied by the input/output voltage differential: I_{OUT} (V_{IN} – V_{OUT})
2. GND pin current multiplied by the input voltage: $I_{GND}V_{IN}$

The GND pin current can be found using the GND pin current graphs in *Typical Characteristics*. Power dissipation is equal to the sum of the two components listed above.

The TPS7A45xx series regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions, the recommended maximum operating junction temperature is 125°C. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface-mount devices, heat sinking is accomplished by using the heat-spreading capabilities of the PCB and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

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Thermal Considerations (continued)

Table 4 lists thermal resistance for several different board sizes and copper areas. All measurements were taken in still air on 1/16-inch FR-4 board with 1-oz copper.

Table 4. Thermal Data (KTT Package, 5-Pin TO-263)

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION TO AMBIENT)
TOPSIDE (1)	BACKSIDE		
2500 mm^2	2500 mm^2	2500 mm^2	23°C/W
1000 mm^2	2500 mm^2	2500 mm^2	25°C/W
125 mm^2	2500 mm^2	2500 mm^2	33°C/W

(1) Device is mounted on topside.

11.3.1 Calculating Junction Temperature

Example: Given an output voltage of 3.3 V, an input voltage range of 4 to 6 V, an output current range of 0 to 500 mA, and a maximum ambient temperature of 50°C, what is the operating junction temperature?

The power dissipated by the device is equal to:

$$I_{OUT(MAX)}(V_{IN(MAX)} - V_{OUT}) + I_{GND}(V_{IN(MAX)})$$

where

- $I_{OUT(MAX)}$ = 500 mA
- $V_{IN(MAX)}$ = 6 V
- I_{GND} at (I_{OUT} = 500 mA, V_{IN} = 6 V) = 10 mA (18)

So,

$$P = 500\ mA \times (6\ V - 3.3\ V) + 10\ mA \times 6\ V = 1.41\ W \quad (19)$$

Using a KTT package, the thermal resistance is in the range of 23°C/W to 33°C/W, depending on the copper area. So the junction temperature rise above ambient is approximately equal to:

$$1.41\ W \times 28°C/W = 39.5\ °C \quad (20)$$

The junction temperature rise can then be added to the maximum ambient temperature to find the operating junction temperature (T_J):

$$T_J = 50°C + 39.5°C = 89.5°C \quad (21)$$

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS7A4501	Click here	Click here	Click here	Click here	Click here
TPS7A4515	Click here	Click here	Click here	Click here	Click here
TPS7A4518	Click here	Click here	Click here	Click here	Click here
TPS7A4525	Click here	Click here	Click here	Click here	Click here
TPS7A4533	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A4501DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS7A4501	Samples
TPS7A4501DCQT	ACTIVE	SOT-223	DCQ	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS7A4501	Samples
TPS7A4501KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	TPS7A4501	Samples
TPS7A4515DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS7A4515	Samples
TPS7A4515DCQT	ACTIVE	SOT-223	DCQ	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		PS7A4515	Samples
TPS7A4515KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	TPS7A4515	Samples
TPS7A4518DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS7A4518	Samples
TPS7A4518DCQT	ACTIVE	SOT-223	DCQ	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		PS7A4518	Samples
TPS7A4518KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	TPS7A4518	Samples
TPS7A4518KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	TPS7A4518	Samples
TPS7A4525DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS7A4525	Samples
TPS7A4525DCQT	ACTIVE	SOT-223	DCQ	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		PS7A4525	Samples
TPS7A4525KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	TPS7A4525	Samples
TPS7A4533DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS7A4533	Samples
TPS7A4533DCQT	ACTIVE	SOT-223	DCQ	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS7A4533	Samples
TPS7A4533KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	TPS7A4533	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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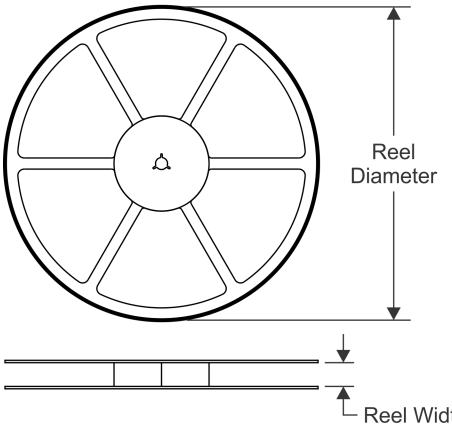
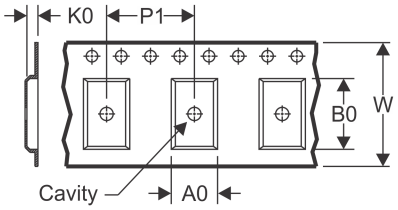
TAPE AND REEL INFORMATION

REEL DIMENSIONS

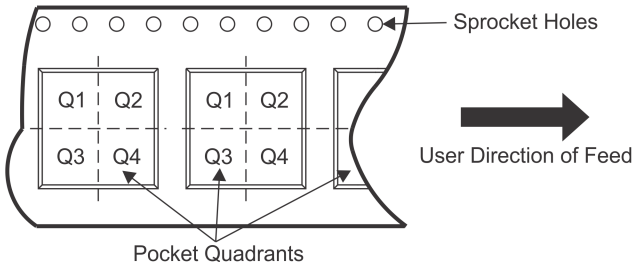


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

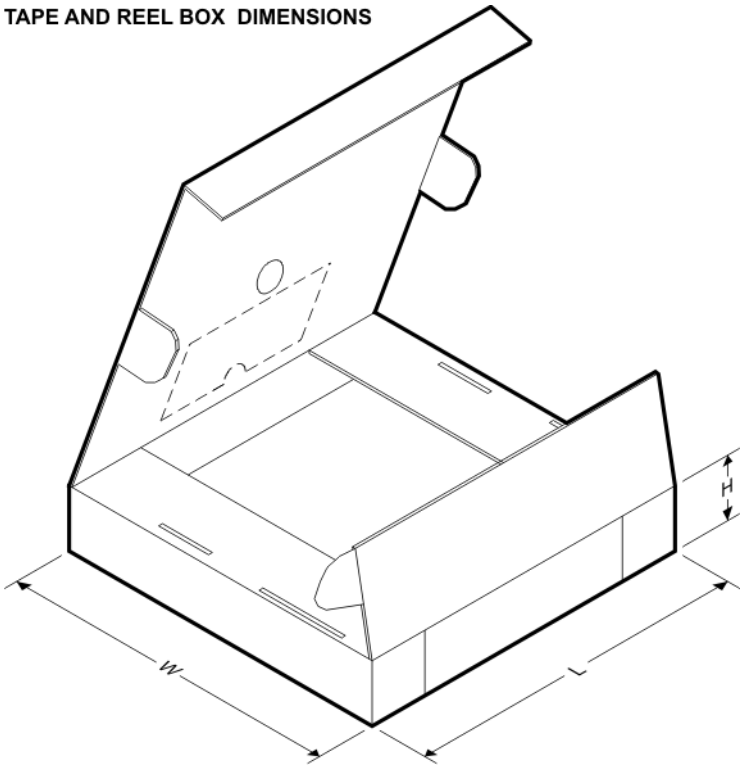


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A4501DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS7A4501DCQT	SOT-223	DCQ	6	250	177.8	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS7A4501KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TPS7A4515DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS7A4515DCQT	SOT-223	DCQ	6	250	177.8	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS7A4515KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TPS7A4518DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS7A4518DCQT	SOT-223	DCQ	6	250	177.8	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS7A4518KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TPS7A4525DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS7A4525DCQT	SOT-223	DCQ	6	250	177.8	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS7A4525KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
TPS7A4533DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS7A4533DCQT	SOT-223	DCQ	6	250	177.8	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS7A4533KTTR	DDPAK/	KTT	5	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	TO-263											

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

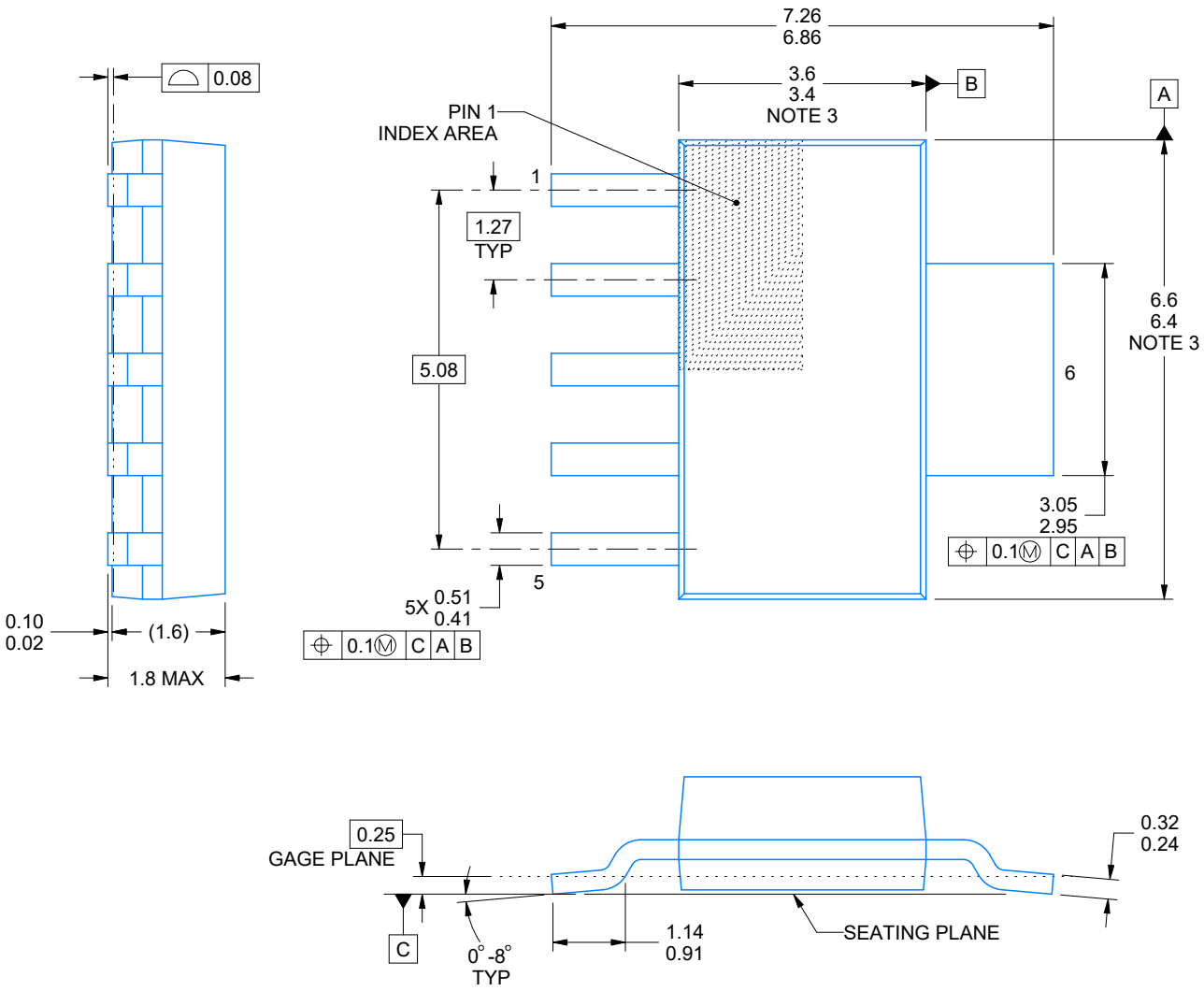
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A4501DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS7A4501DCQT	SOT-223	DCQ	6	250	223.0	270.0	35.0
TPS7A4501KTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TPS7A4515DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS7A4515DCQT	SOT-223	DCQ	6	250	180.0	180.0	85.0
TPS7A4515KTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TPS7A4518DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS7A4518DCQT	SOT-223	DCQ	6	250	223.0	270.0	35.0
TPS7A4518KTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TPS7A4525DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS7A4525DCQT	SOT-223	DCQ	6	250	180.0	180.0	85.0
TPS7A4525KTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TPS7A4533DCQR	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS7A4533DCQT	SOT-223	DCQ	6	250	180.0	180.0	85.0
TPS7A4533KTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0

PACKAGE OUTLINE

DCQ0006A

SOT - 1.8 mm max height

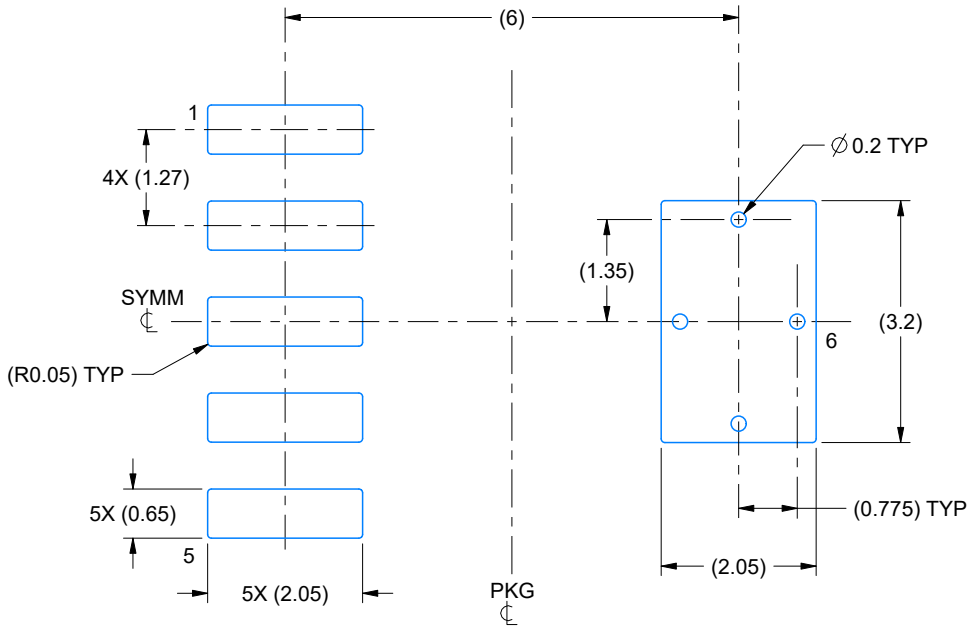
PLASTIC SMALL OUTLINE



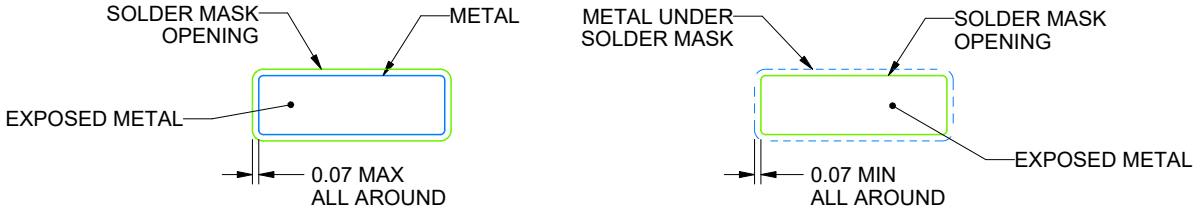
4214845/C 11/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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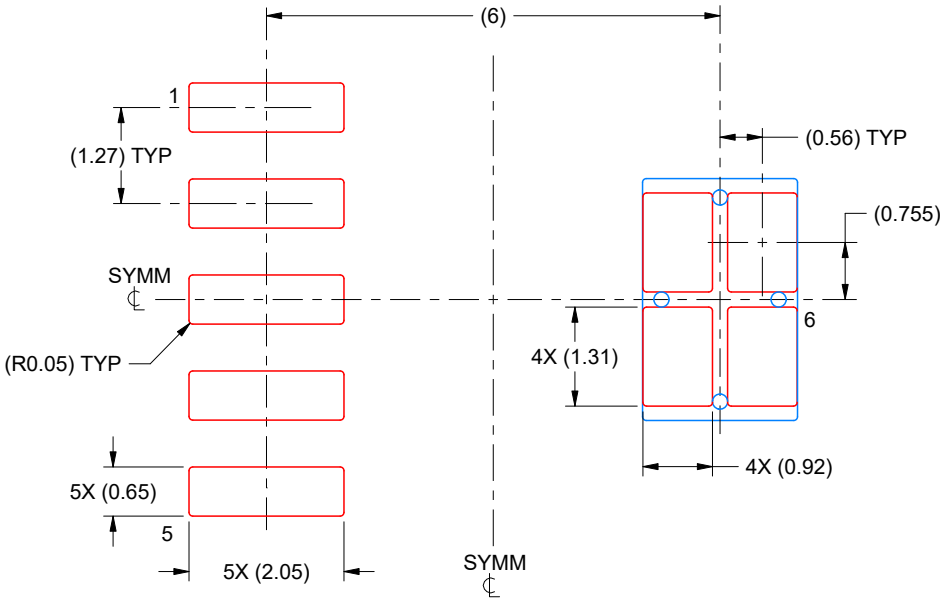
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



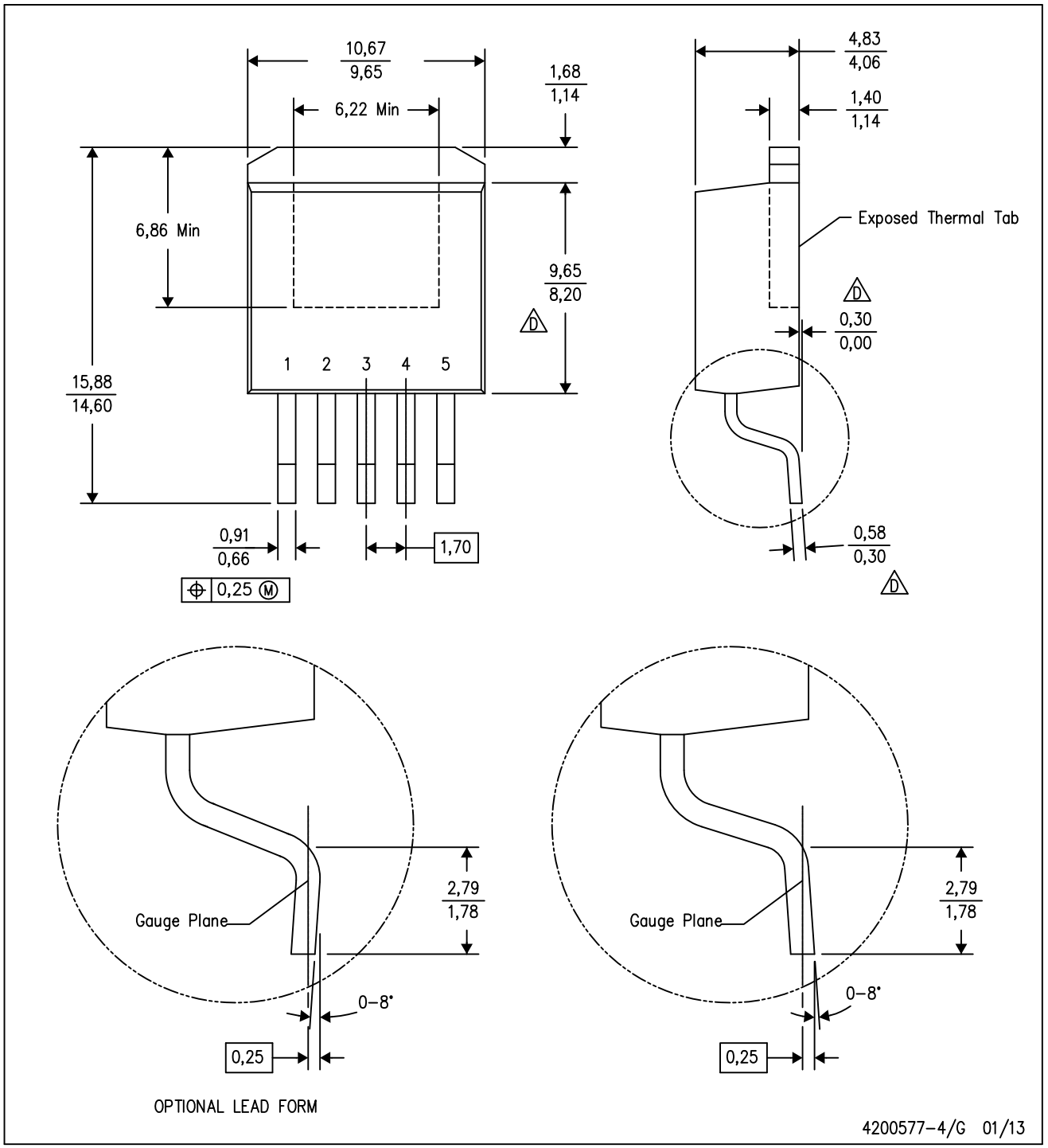
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

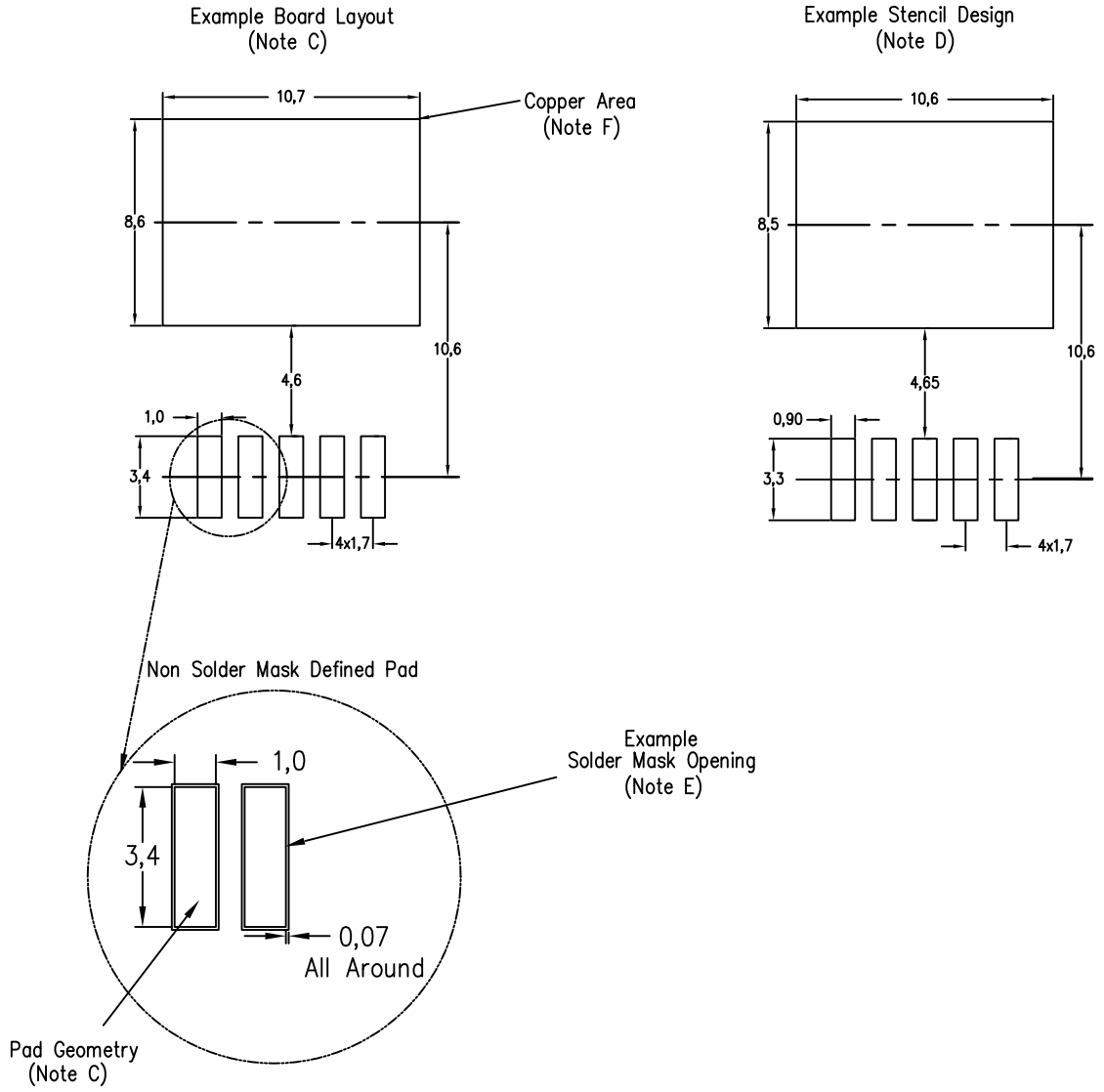
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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