TPS92511 500mA，65V 共阳极恒定电流降压发光二极管 (LED) 驱动器，无外部电流感测电阻器

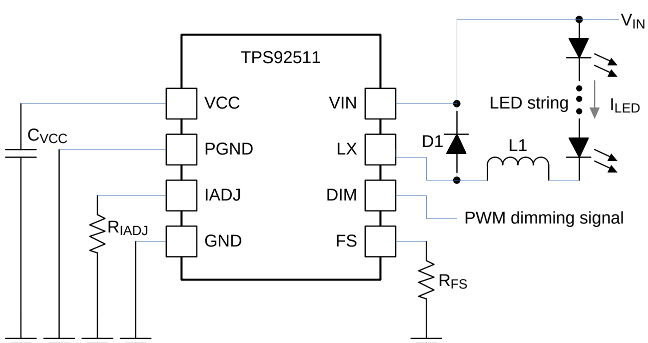
1 特性

- 宽输入电压范围：4.5V 至 65V
- 无需外部电流感测电阻器
- 无需外部环路补偿
- 易于使用，最少需要 5 个组件
- 1000:1 对比率可行
- 单层印刷电路板 (PCB) 可行
- 可作为高压降压稳压器运行
- 可作为线性电流并联稳压器运行
- 集成低端 N 通道金属氧化物半导体场效应晶体管 (MOSFET)
- LED 电流可设定为高达 0.5A
- 典型值为 ±3.6% 的 LED 电流精度
- 开关频率可在 50kHz 至 500kHz 之间进行编程
- 电流限制保护
- VCC 欠压闭锁
- 热关断保护
- 支持模拟调光和热折返
- 带有外露散热焊盘的功率增强型小外形尺寸集成电路 (SOIC)-8 封装（带散热片小外形尺寸封装 (HSOP)-8）

2 应用范围

- 高功率 LED 驱动器
- 建筑照明
- 办公室嵌入式照明
- 汽车照明
- MR-16 LED 灯

简化应用



3 说明

TPS92511 是一款易于使用的 65V 恒定电流降压转换器，用于驱动电流高达 0.5A 且效率高达 95% 的单个 LED 灯串。 对于基本运行，只需 5 个外部组件，而且由于集成了一个 N-MOSFET，无外部电流感测电阻器，没有外部补偿，以及适当的端子分配，可实现单层 PCB。 LED 电流由一个高值外部电阻器设定，这样的话，可实现 LED 电流的微调。 另外一个高值外部电阻器将恒定开关频率设定在 50kHz 至 500kHz 之间。 电磁干扰 (EMI) 的设计由于恒定开关频率的原因而变得更加简单。 TPS92511 提供 4.5V 至 65V 的宽输入电压范围。 通过添加简单的外部电路，此器件甚至能够处理具有更高输入电压的应用。

TPS92511 采用私有控制机制来调节 LED 电流，而无需直接感测 LED 电流。 它采用一个具有低端 N 通道功率 MOSFET 的浮动降压拓扑结构，此拓扑结构无需自举电容器。 对于多通道系统，浮动降压拓扑结构连同私有控制机制可在无需外部电流感测网络的前提下实现 LED 灯串的共阳极连接。 这极大地减少了接线数量，以及整体制造成本。

TPS92511 具有极快速的脉宽调制 (PWM) 调光响应时间。 例如，如果开关频率为 500kHz，最小 DIM 脉宽为 6μs，并且调光频率为 150Hz，那么可实现大于 1000:1 的对比率。

TPS92511 采用带有外露散热焊盘的功率增强型 SOIC-8 封装。

器件信息(1)

部件号	封装	封装尺寸（标称值）
TPS92511	HSOP (8)	4.89mm × 3.90mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

English Data Sheet: SNVS901

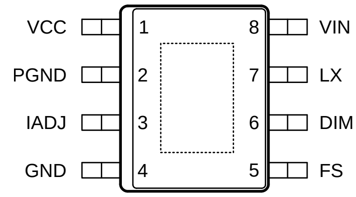
目录

4 修订历史记录

Changes from Original (March 2014) to Revision A	**Page**
• 已更正图形数字排序	1
• 已更新器件信息表	1
• Changed Terminal to Pin	3

5 Pin Configuration and Functions

DDA (SO THERMAL PAD) PACKAGE
8 PINS
(TOP VIEW)



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
DIM	6	PWM Dimming Control. Apply logic level PWM signal to this pin dims the LED string. This pin is internally pulled up.
FS	5	Switching Frequency Setting. An external resistor R_{FS} connecting the FS pin to ground programs the switching frequency from 50 kHz to 500 kHz.
GND	4	Analog Signal Ground.
IADJ	3	Average LED Current Setting. An external resistor R_{IADJ} connecting the IADJ pin to ground programs the average LED current.
LX	7	Integrated MOSFET Drain. Internally connected to the drain of the integrated MOSFET. Connect this pin to the output inductor and anode of the Schottky diode.
PGND	2	Power Ground. Must be connected to the GND pin for normal operation. The PGND and GND pins are not internally shorted.
VCC	1	Internal Regulator Output. Typically regulated to 5.4 V. Connect a capacitor of larger than 1 µF between the VCC and GND pins.
VIN	8	Input Voltage. Supply pin to the device. The input voltage range is from 4.5 V to 65 V.
Thermal pad		Thermal Connection Pad. Connect to a ground plane for heat dissipation.

6 Specifications

6.1 Absolute Maximum Ratings (1)

Unless otherwise specified, $T_J = T_A = 25°C$

		MIN	NOM	MAX	UNIT
Pin voltage range	VIN to GND	–0.3		65	V
	VIN to GND (Transient)	–0.3		67	V
	LX to PGND	–0.3		65	V
	LX to PGND (Transient)	–3(2ns)		67	V
	FS, IADJ to GND	–0.3		5	V
	DIM to GND	–0.3		6	V
	VCC to GND	–0.3		7	V
Temperature range	Operating junction temperature range, T_J	–40		Internally limited	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specified specifications and test conditions, see the Electrical Characteristics.

6.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	-65	150	°C
V_{ESD} (1)	Human Body Model (HBM) ESD stress voltage (2)		1.5	kV
	Charged Device Model (CDM) ESD stress voltage (3)		1.5	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage range	4.5		65	V
T_A	Operating free air temperature	–40		125	°C
T_J	Operating junction temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPS92511	UNIT
		DDA	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	59.9	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	59.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	30.6	
ψ_{JT}	Junction-to-top characterization parameter	11.0	
ψ_{JB}	Junction-to-board characterization parameter	30.5	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	4.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified, -40°C ≤ T_J = T_A ≤ 125°C, V_{IN} = 48 V

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM						
$I_{IN-DIM-HIGH}$	VIN Operating Current	4.5 V ≤ V_{IN} ≤ 65 V, R_{IADJ} = 3 kΩ, V_{DIM} = High		2.8	3.15	mA
$I_{IN-DIM-LOW}$	VIN Standby Current	4.5 V ≤ V_{IN} ≤ 65 V, R_{IADJ} = 3 kΩ, V_{DIM} = Low		2.3	2.7	mA
I_{LX-OFF}	LX Pin Current	Main switch turned OFF, V_{LX} = V_{IN} = 65 V		0.1	1.0	µA
I_{LED}	Average LED Current	V_{FS} = 4.6V, R_{IADJ} = 3 kΩ, T_A = 25°C	484	502	520	mA
		V_{FS} = 4.6V, R_{IADJ} = 3 kΩ	477	502	528	mA
		V_{FS} = 4.6V, R_{IADJ} = 6 kΩ, T_A = 25°C	236	249	262	mA
		V_{FS} = 4.6V, R_{IADJ} = 6 kΩ	233	249	268	mA
		V_{FS} = 4.6V, R_{IADJ} = 10 kΩ, T_A = 25°C	138	149	160	mA
		V_{FS} = 4.6V, R_{IADJ} = 10 kΩ	133	149	166	mA
V_{IADJ}	IADJ Pin voltage		1.224	1.25	1.278	V
V_{DIM-ON}	DIM Pin Upper Threshold	V_{DIM} Increasing	0.85	1.0	1.25	V
$V_{DIM-OFF}$	DIM Pin Lower Threshold	V_{DIM} Decreasing	0.44			V
$V_{DIM-HYS}$	DIM Pin Threshold Hysteresis			325		mV
f_{SW}	Switching frequency	R_{FS} = 20 kΩ	450	500	550	kHz
$t_{on(min)}$	Minimum On-time			250	400	ns
INTERNAL REGULATOR						
V_{CC}	VCC Regulated Output Voltage	C_{VCC} =1 µF, no load	4.7	5.4	6.0	V
		C_{VCC} =1 µF, V_{IN} = 4.5V, 2 mA load	3.7	4.1		V
$V_{CC-UVLO-ON}$	VCC UVLO Upper Threshold	V_{CC} rising	3.50	3.75	4.00	V
$V_{CC-UVLO-OFF}$	VCC UVLO Lower Threshold	V_{CC} falling	3.05			V
$V_{CC-UVLO-HYS}$	VCC UVLO Hysteresis			275		mV
INTEGRATED MOSFET						
R_{LX}	Resistance Across LX and GND	Main Switch Turned ON, T_A = 25°C		1.4	2.15	Ω
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature	T_J Rising		165		°C
T_{SD-HYS}	Thermal shutdown hysteresis	T_J Falling		10		

6.6 Typical Characteristics

Unless otherwise specified, all curves are taken at V_{IN} = 48V with configuration in the application circuit for driving 12 LEDs with I_{LED} = 0.5A and f_{SW} = 300 kHz as shown in this datasheet, and T_A = 25°C.

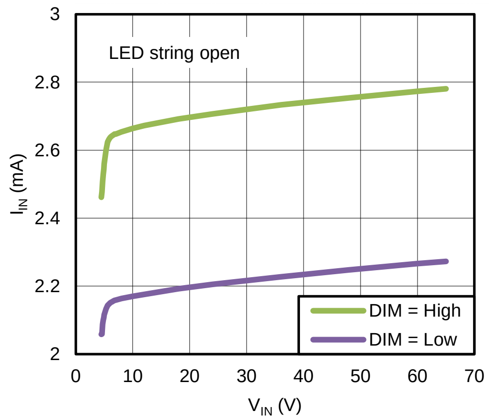


图 1. I_{IN} vs V_{IN}

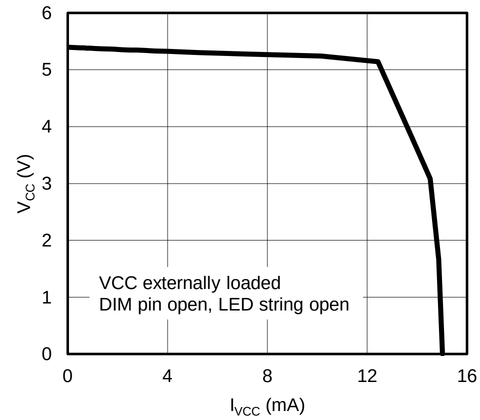


图 2. V_{CC} vs I_{VCC}

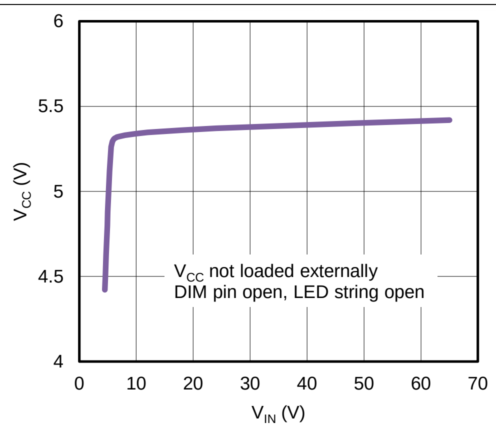


图 3. V_{CC} vs V_{IN}

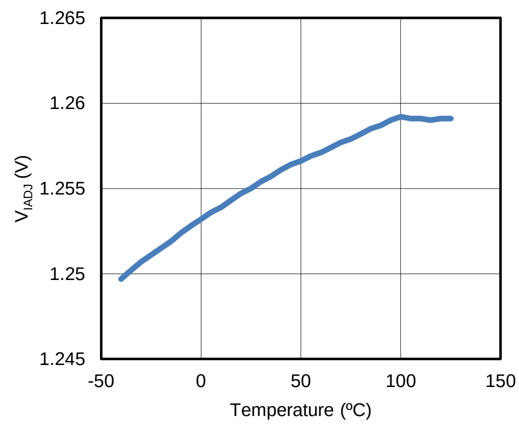


图 4. V_{IADJ} vs Temperature

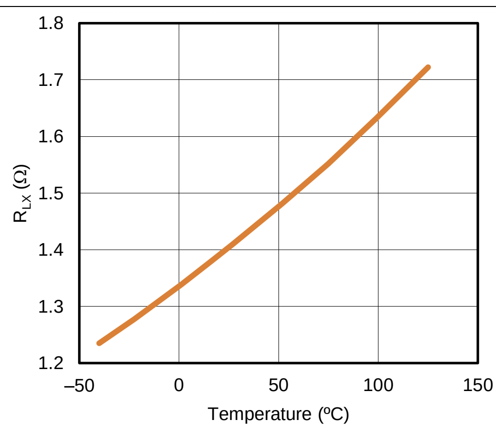


图 5. R_{LX} vs Temperature

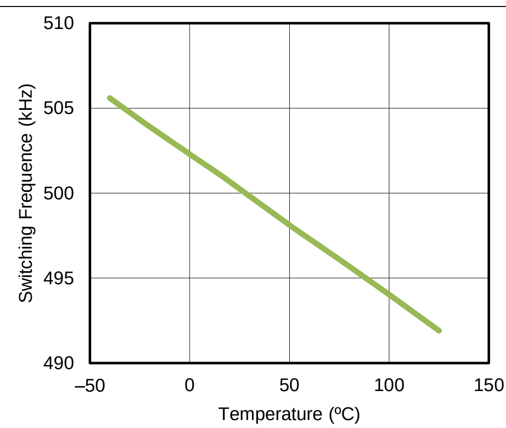


图 6. f_{SW} vs Temperature

Typical Characteristics (接下页)

Unless otherwise specified, all curves are taken at V_{IN} = 48V with configuration in the application circuit for driving 12 LEDs with I_{LED} = 0.5A and f_{SW} = 300 kHz as shown in this datasheet, and T_A = 25°C.

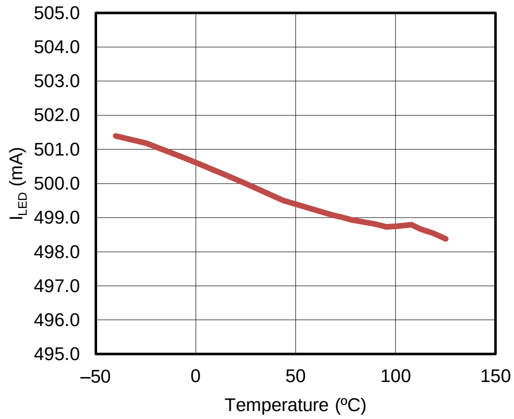


图 7. I_{LED} at 500 mA vs Temperature

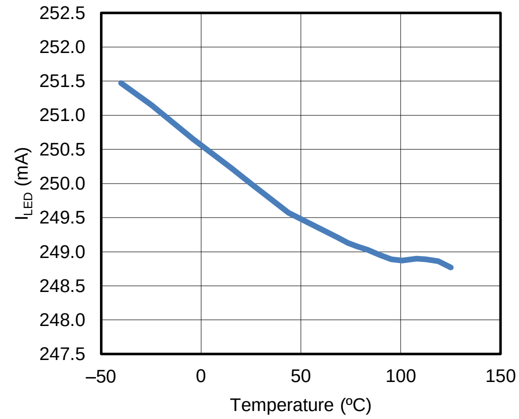


图 8. I_{LED} at 250 mA vs Temperature

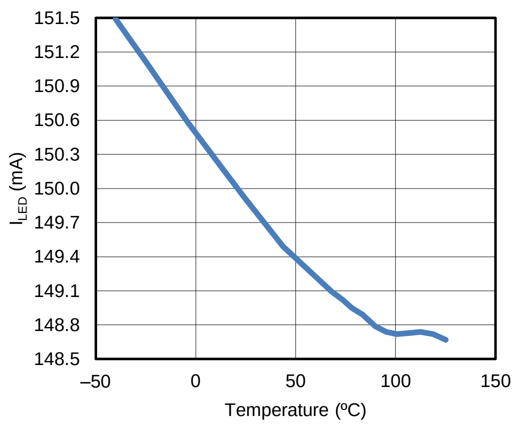


图 9. I_{LED} at 150 mA vs Temperature

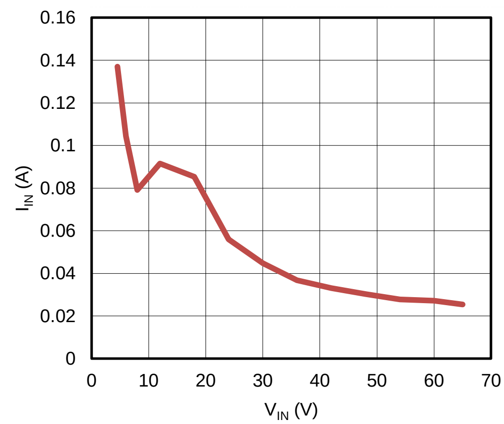


图 10. I_{IN} vs V_{IN} at LED Short

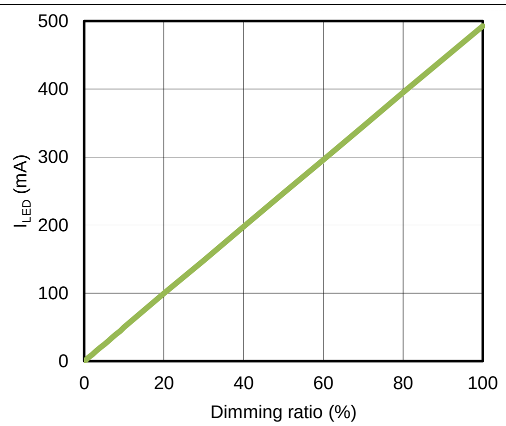


图 11. PWM Dimming Linearity (0-100%) (f_{SW} = 500kHz, L1 = 68 µH

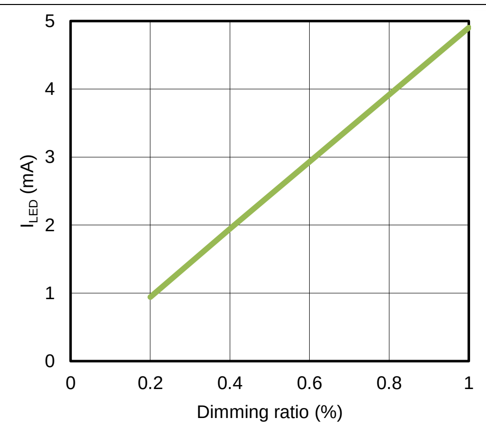


图 12. PWM Dimming Linearity (under 1%) (f_{SW} = 500kHz, L1 = 68 µH

7 Detailed Description

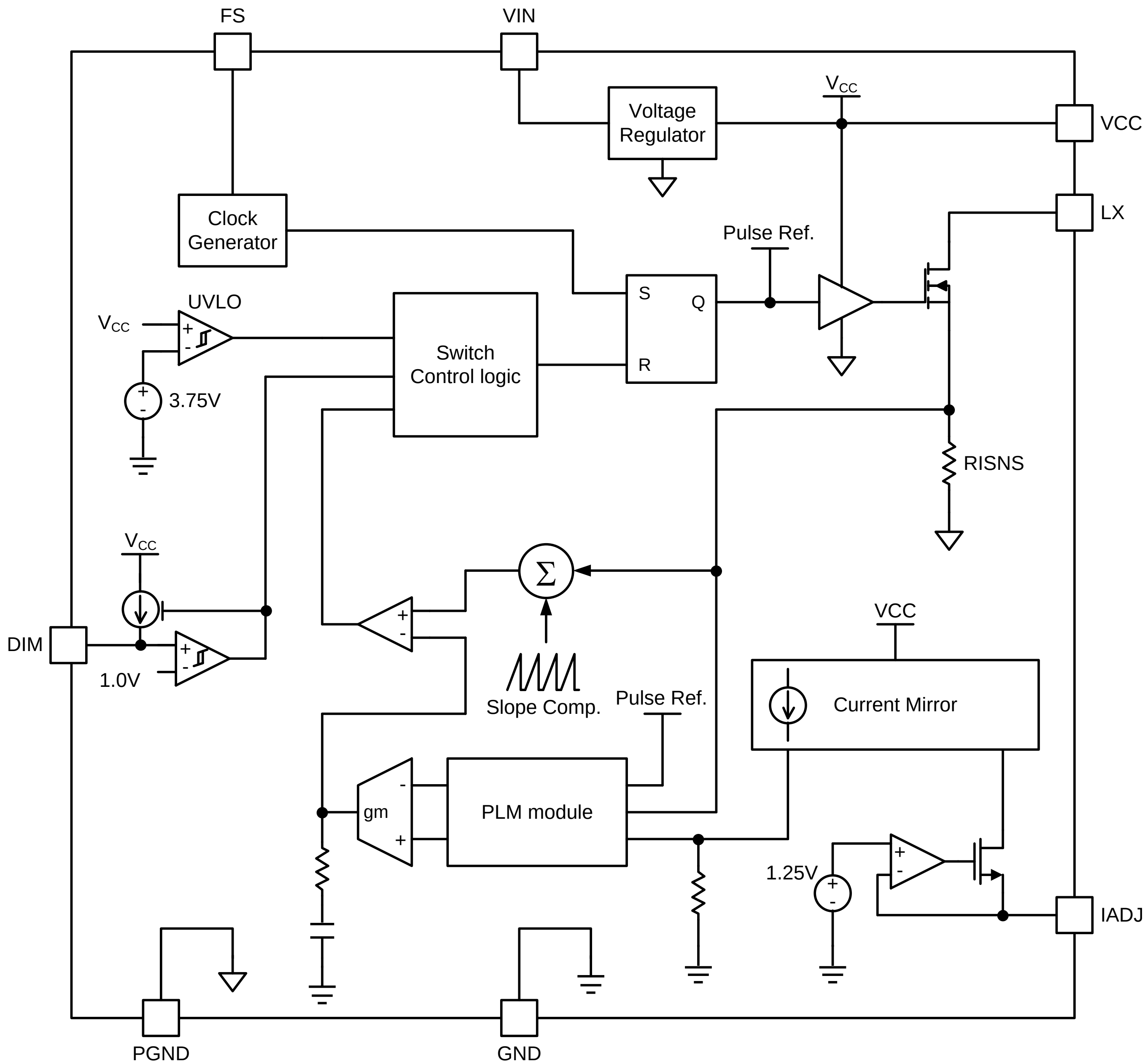
7.1 Overview

The TPS92511 is an easy to use constant current buck converter for driving a single LED string with current up to 0.5A and efficiency up to 95%. Only 5 external components are required for basic operation and single layer PCB layout is feasible because of the integration of a N-MOSFET, no external current sensing resistor, no external compensation and the proper pin assignment. A high-value external resistor programs the LED current so that fine tuning of the LED current can be achieved. Another high-value external resistor programs a constant switching frequency from 50kHz to 500kHz. As a result of constant switching frequency, EMI design becomes easy. The TPS92511 provides a wide input voltage range from 4.5V to 65V. By adding simple external circuits, it can handle applications with even higher input voltages.

The TPS92511 employs a proprietary Pulse-Level-Modulation (PLM) control scheme under continuous conduction mode (CCM) to regulate the LED current without the need of sensing the LED current directly. It applies a floating buck topology with a low-side N-channel power MOSFET, which does not need boot-strapping capacitor, so that driving LED string under drop-out conditions and very high input voltages are feasible. For multiple channel systems, the floating buck topology without external current sensing network together with the proprietary control scheme allows a common-anode connection of the LED strings without external current sensing network. This saves high-side current sensing wirings for separate driver boards and LED board systems and significantly reduces the number of wiring, which can lower overall manufacturing cost.

The TPS92511 has very fast PWM dimming response time. There is almost no delay between the DIM pin voltage rising edge and the start of the LED current conduction, so it can dim down to nearly zero current. In order to maintain good dimming linearity, the minimum LED current pulse width is suggested to be three switching cycles. For example, if the switching frequency is 500 kHz, the minimum DIM pulse width is 6µs and the dimming frequency is 150Hz, a contrast ratio of more than 1000:1 can be achieved.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Pulse Level Modulation (PLM) Control

A proprietary Pulse-Level-Modulation (PLM) control method is used in the TPS92511. It can regulate the average LED current by sensing only the inductor current at the on-period (图 13). The integrated MOSFET and the sensing and control circuits in the TPS92511 implement the whole PLM control internally so the control does not suffer from tolerance and noise issues that may be coming from external components. As compared with the conventional method which regulates average LED current by sensing the current over the entire switching cycle, the power dissipation on the sensing circuit in PLM is much lower. For example, consider a duty cycle of 0.5, the power dissipation on current sensing in PLM can be reduced by half. PLM requires no external loop compensation circuit. Besides, the accuracy of the regulated LED current is high (typically ±3.5% in the TPS92511).

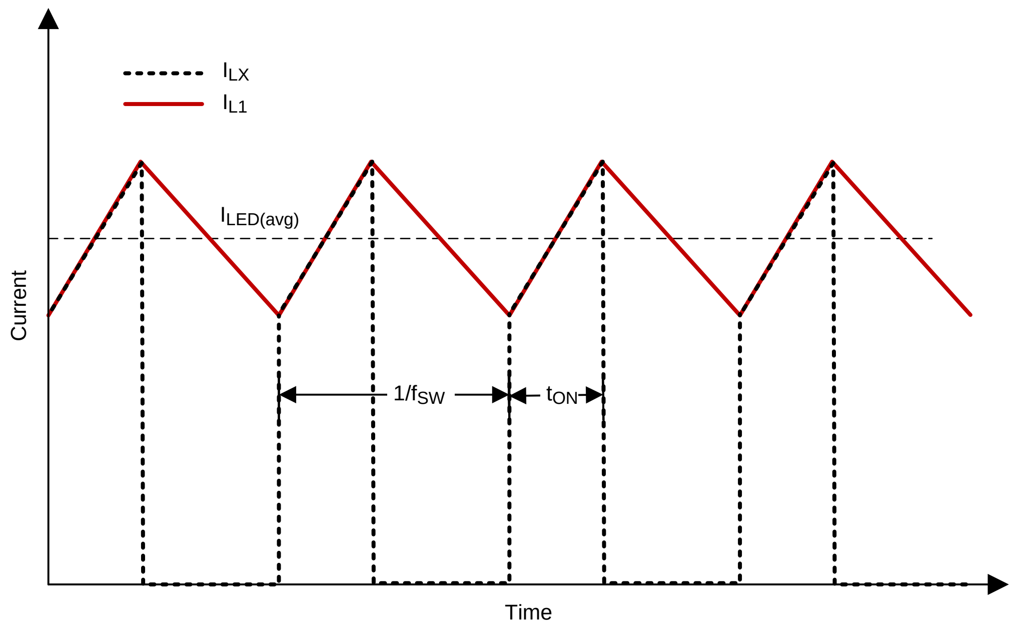


图 13. Waveforms of a Floating Buck LED Driver with PLM

7.3.2 Pulse Level Modulation (PLM) Operaion Principles

The Pulse-Level-Modulation is a patented method to ensure an accurate average output current regulation without the need of direct output current sensing. 图 13 shows the current waveforms of a typical buck converter under steady state, where, I_{L1} is the inductor current and I_{LX} is the current flowing into the LX pin. For a buck converter operating in steady state, the mid-point of the RAMP portion of I_{L1} equals to the average value of I_{L1} and hence the average LED current $I_{LED(avg)}$. In short, by regulating the mid-point with respect to a precise reference level, PLM achieves LED current regulation by sensing the main MOSFET current solely, instead of the entire cycle of I_{L1}.

7.3.3 PLM Control enable Common-Anode Low-Side Sensing (CALS)Technique to Save Wiring

For multi-channel systems with separated driver boards and LED array boards, the Pulse-Level-Modulation (PLM) control scheme enable Common-Anode Low-Side Current Sensing to save inter-board wirings. 图 14 shows a conventional configuration with a Low-side switching and High-Side Current Sensing. For an n channel system with separated driver and an LED array boards, 2n inter-board wirings are required. For example, an 128-channel system needs 256 inter-board wirings, which implies a high material and manufacturing cost. 图 15 shows the PLM configuration with Low-side switching and Low-Side Current Sensing. A Common-Anode configuration is used for the LED array board. As shown in the figure, an n channel system with separated driver and LED array boards requires only n+1 inter-board wirings. For an 128-channel system, only 129 inter-board wirings are required. The wiring cost is cut by half, and the cost of the end product can be reduced.

Feature Description (接下页)

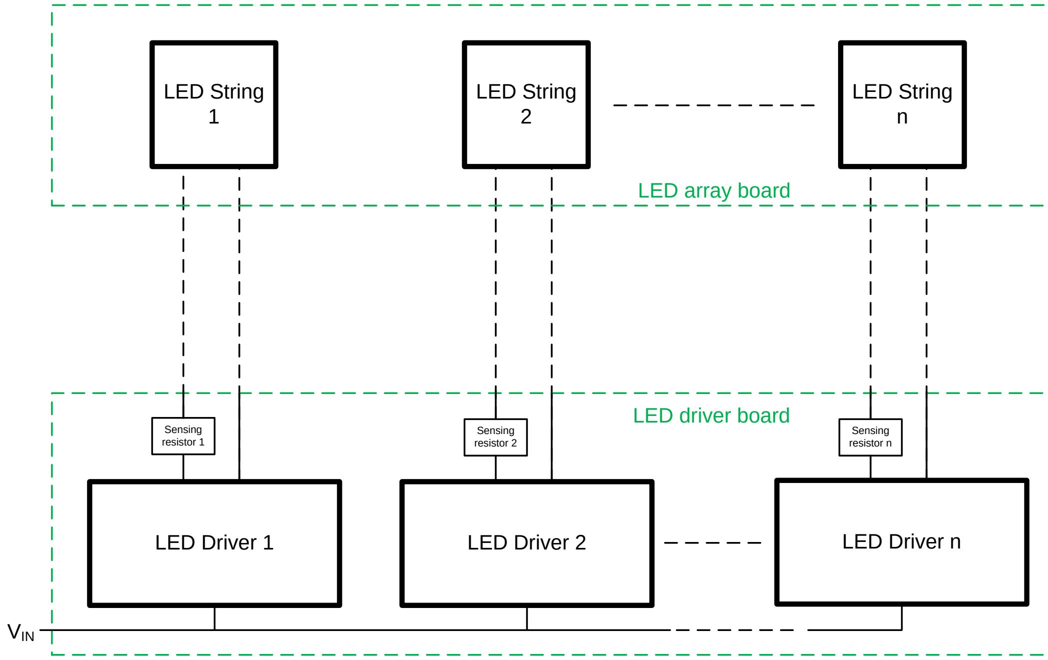


图 14. Conventional Configuration with Low-Side Switching and High-Side Current Sensing Requires 2×n Inter-Board Wirings

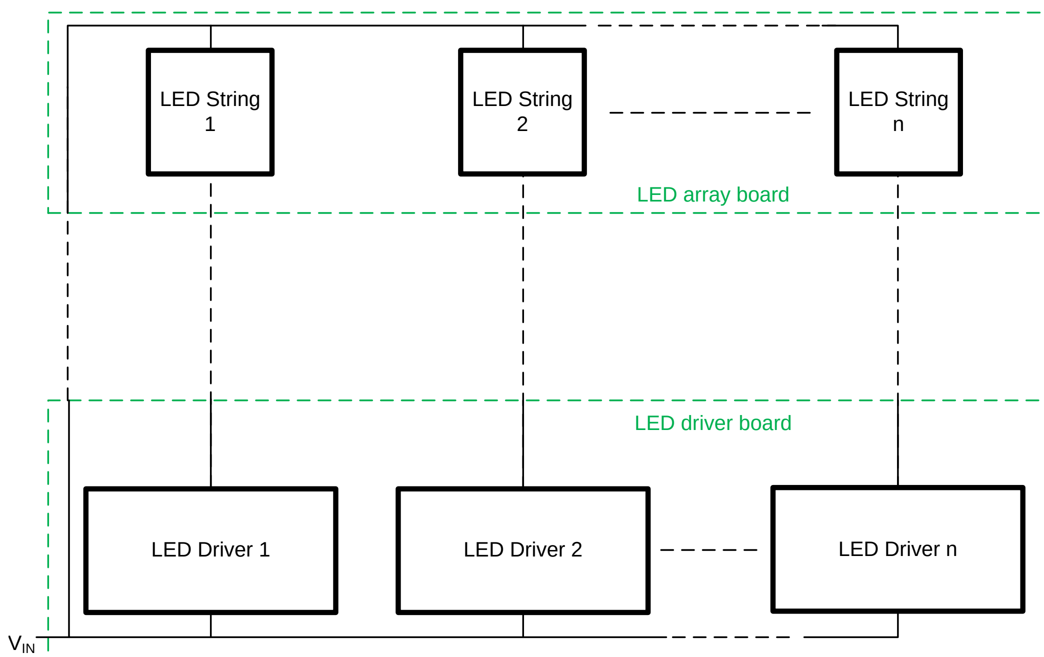


图 15. PLM Configuration with Common-Anode Low-Side Switching Requires n+1 Inter-Board Wirings

Feature Description (接下页)

7.3.4 Internal Regulator

The TPS92511 integrates an internal voltage regulator for powering internal circuitry. For stability, an external capacitor C_{VCC} of at least 1 µF should be connected between the VCC and PGND pins The output of the internal regulator V_{CC} is 5.4V when V_{IN} is larger than 6V. If V_{IN} is lower than 6V, V_{CC} decreases. The TPS92511 will trigger the VCC under-voltage lock-out if V_{CC} falls below typically 3.5V. V_{CC} can be used to bias external circuits subject to a loading of maximum 2 mA, while it has a short circuit current limit at typically 16 mA.

7.3.5 Setting The Switching Frequency

The switching frequency f_{SW} of the TPS92511 is programmable in the range of 50 kHz to 500 kHz by a single resistor R_{FS} connecting the FS pin and ground. The following equation shows the relationship between f_{SW} and R_{FS}:

$$f_{SW} = \frac{10 \times 10^6}{R_{FS}} \text{kHz} \quad (1)$$

图 16 plots f_{sw} against R_{FS}. 表 1 shows values of R_{FS} for commonly used switching frequencies.

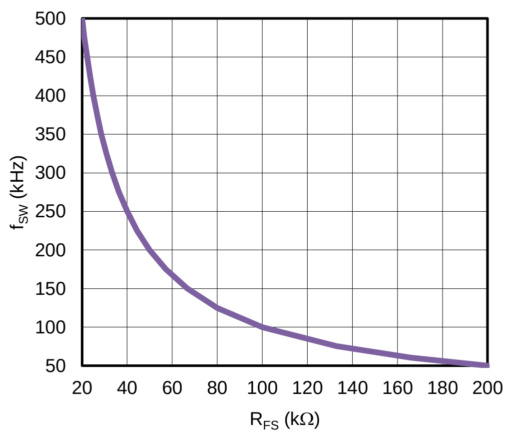


图 16. Switching Frequency vs R_{FS}

表 1. Commonly Used f_{SW} And R_{FS}

f_{SW} (kHz)	R_{FS} (kΩ)
50	200
100	100
300	33.2
500	20

7.3.6 Setting The LED Current

The LED current I_{LED} of the TPS92511 is programmable by a single resistor R_{IADJ} connecting the IADJ pin and ground. The IADJ pin is internally biased to 1.25 V. 公式 2 shows the relationship between I_{LED} and R_{IADJ}:

$$I_{LED} = \frac{1500}{R_{IADJ}} \text{A} \quad (2)$$

To ensure stability, R_{IADJ} must be less that 30 kΩ, implying a minimum I_{LED} of 50 mA can be programmed. The tolerance of I_{LED} of 150 mA is shown in the ELECTRICAL CHARACTERISTICS. Larger tolerance should be expected for lower I_{LED}. 图 17 plots I_{LED} against R_{IADJ}. 表 2 shows values of R_{IADJ} for commonly used I_{LED}.

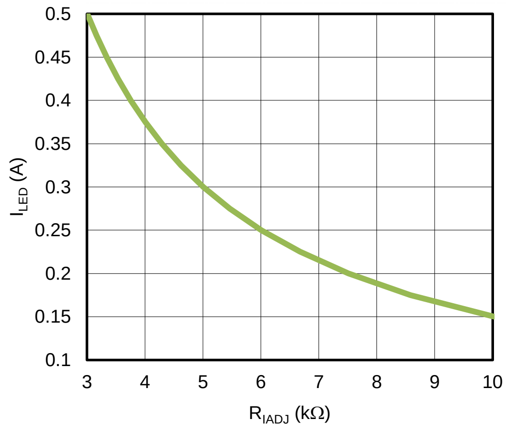


图 17. LED Current vs $_{RIADJ}$

表 2. Commonly Used I_{LED} And R_{IADJ}

I_{LED} (mA)	R_{IADJ} (kΩ)
150	10
350	4.32
500	3.01

7.3.7 Integrated MOSFET

The TPS92511 integrates a N-channel power MOSFET, the drain of which is connected to the LX pin. When the integrated MOSFET is turned on, the resistance across the LX and GND pins is typically 1.4Ω. The integrated MOSFET has a fixed current limit of 1.2A to protect the application circuit during critical operation conditions like short circuit of the LED string. Once the limit is hit, the integrated MOSFET turns off immediately for 34 µs to let the inductor discharge.

The minimum on-time of the integrated MOSFET is 400 ns. It may be hit at a high switching frequency and a high V_{IN}/V_{LED} ratio. Once hit, the I_{LED} regulation may be affected. In the worst case, I_{LED} may be boost up to a level higher than the programmed value, and the LED string and/or the inductor may be damaged as a result. Hence, it is recommened that the ratio between V_{IN} and V_{LED} should be designed under the following constraint:

$$\frac{V_{LED}}{V_{IN}} \geq 400ns \times f_{SW} \tag{3}$$

7.3.8 Inductor Selection

Operating in the continuous conduction mode (CCM) is required in the TPS92511 application circuit. In the CCM, considering the on-period, the peak-to-peak inductor current ripple ($2\Delta I_{L1}$) is shown in 公式 4.

$$2\Delta I_{L1} = \frac{t_{on}\left(V_{IN} - V_{LED}\right)}{L_1} \tag{4}$$

Because

$$\frac{V_{LED}}{V_{IN}} = t_{on} f_{SW} \tag{5}$$

L_1 can be a function of V_{IN}, V_{LED}, f_{SW} and ΔI_{L1} as shown in 公式 6 .

$$L_1 = \frac{\left(V_{IN} - V_{LED}\right)V_{LED}}{2\Delta I_{L1} V_{IN} f_{SW}} \tag{6}$$

The value of L_1 is selected by designers with the consideration of all above parameters. The minimum L_1 calculated by the following equation is a good starting point for designing L_1:

$$L_1 > 1\mu H\Omega^{-1} \times \frac{R_{FS}R_{IADJ}}{10^6} \tag{7}$$

The following table shows some typical examples of using R_{FS} and R_{IADJ} to estimate the minimum L_1:

表 3. Estimation Of Minimum L_1 Using R_{FS} And R_{IADJ}

R_{FS} (kΩ)	R_{IADJ} (kΩ)	Estimated Minimum L_1 (µH)	Recommended L_1 (µH)
100	10	1000	1000
33.2	3.01	100	100
20	4.32	86	100
20	3.01	60	68

To maintain the CCM, ΔI_{L1} must be smaller than the average LED current $I_{LED(avg)}$. Hence, the minimum inductance used is:

$$L_{1(min)} = \frac{(V_{IN} - V_{LED})V_{LED}}{2I_{LED(avg)}V_{IN}f_{SW}} \tag{8}$$

In the absence of output capacitors, the TPS92511 can maintain a continuous I_{LED} throughout the entire switching cycle because in such case the inductor current is the same as I_{LED} (floating buck topology operating in the CCM). However, the LED peak current must not exceed the rated current of the LED. The peak LED current can be found by the following equation:

$$I_{LED(peak)} = I_{LED(avg)} + \frac{(V_{IN} - V_{LED})V_{LED}}{2L_1V_{IN}f_{SW}} \tag{9}$$

7.3.9 Integrated MOSFET Current Limit

The current limit of the integrated MOSFET is internally fixed at 1.2A to protect the LED string, the inductor and the integrated MOSFET from overdriven. Once triggered, the integrated MOSFET turns off immediately for 34 µs to let the inductor to discharge. The triggering of the current limit cycles repetitively until all overdriven conditions disappear.

7.3.10 PWM Dimming Control

The TPS92511 implements PWM dimming by applying a PWM dimming signal to the DIM pin. A low input applying to the DIM pin disables the switching of the integrated MOSFET, and as a result discharges the inductor and then turns off the LED string. To turn on the LED string, the DIM pin should be connected to high or left open (since it is internally pulled high by a current of typically 40 µA and 90 µA when the DIM pin is low and high respectively). The PWM dimming frequency is recommended to be lower than $0.1f_{SW}$ to ensure normal operation.

7.3.11 Analog Dimming

Analog dimming can be implemented by injecting a current to R_{IADJ} (图 18) and as a result reduces the current of the IADJ pin, I_{ADJ}, which is controlled internally by the TPS92511 to bias the voltage on the IADJ pin to be 1.25V. If the CCM can be maintained, the minimum I_{ADJ} can achieve 15 µA, which refers to an I_{LED} of 18 mA. If I_{ADJ} is further decreased, I_{LED} may not follow due to the presence of the minimum on-time of the integrated MOSFET. If the CCM cannot be maintained, I_{LED} can still decrease monotonically with I_{ADJ}. However, if good line and load regulations are required, the CCM should be maintained by using a large inductance.

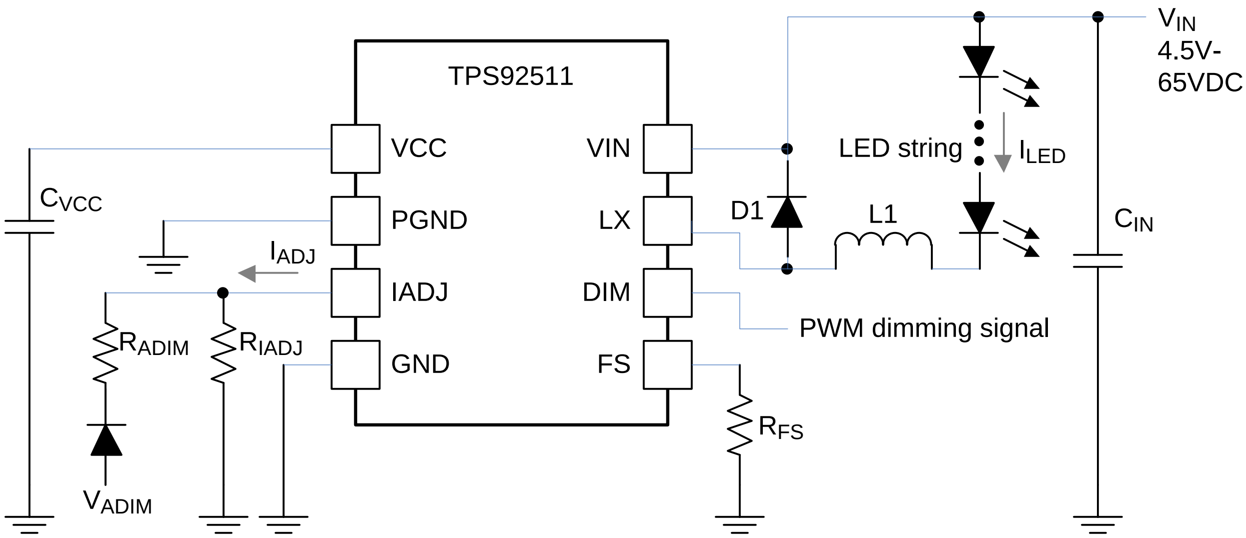


图 18. Circuit Configuration for Analog Dimming

7.3.12 High Voltage Buck Configuration

The TPS92511 can handle applications with an input voltage higher than 65V, which is the maximum V_{IN} of the recommended operating condition of the TPS92511, by adding an external high voltage N-channel MOSFET to the application circuit as shown in 图 19. PWM dimming can be implemented in this circuit without additional efforts, and analog dimming is also feasible by referencing to additional circuits shown in 图 18.

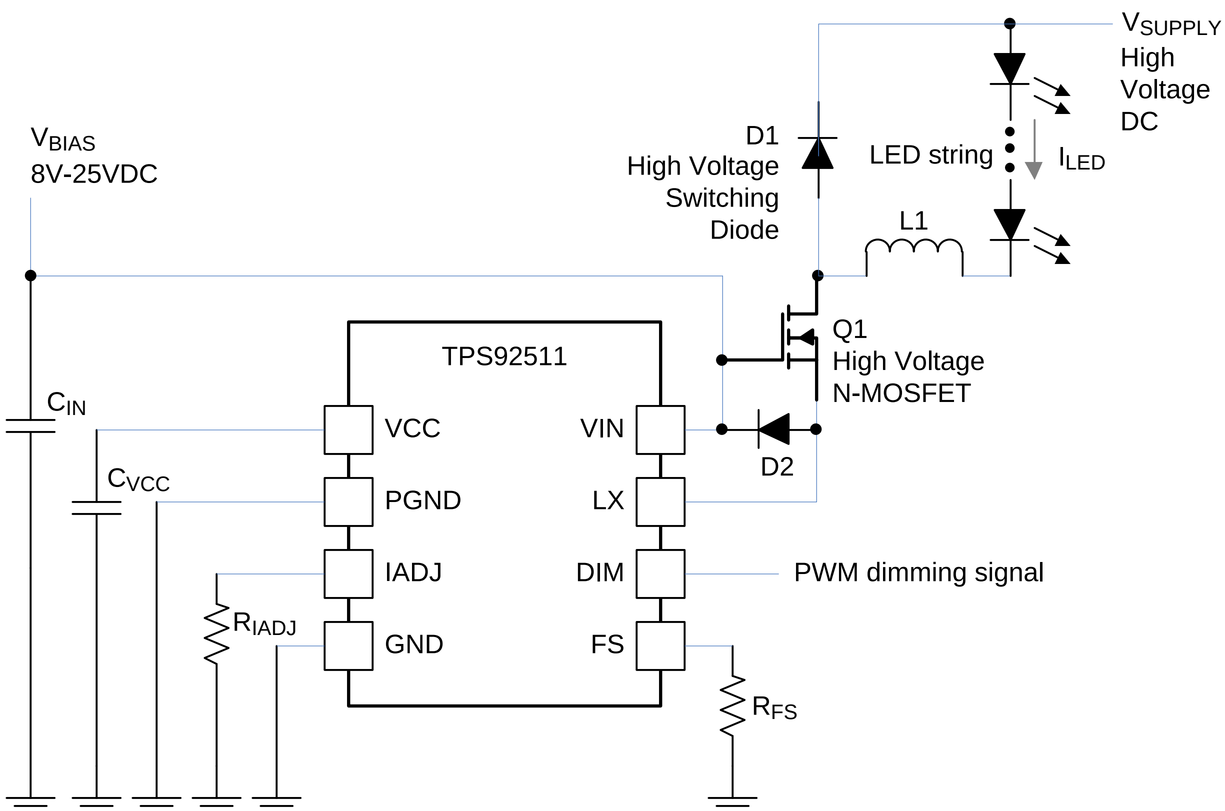


图 19. Circuit Configuration for Very High Voltage Buck

7.3.13 Thermal Foldback

Thermal foldback is useful to prevent over-temperature of LEDs during operation by sensing the temperature of LEDs and, if the sensed temperature is high, reducing I_{LED} to decrease the power and as well as the temperature of LEDs. Thanks to the feature of analog dimming, thermal foldback can be implemented by embedding a negative temperature coefficient (NTC) resistor, R_{NTC}, into a circuit as shown in 图 20. When the sensed temperature increases, R_{NTC} decreases and thus the emitter current of Q_{T1} increases to reduce I_{LED} by means of analog dimming. The resistor R_{TF} can adjust the loop gain of the thermal foldback control loop, which should be high enough to avoid oscillation and maintain stability.

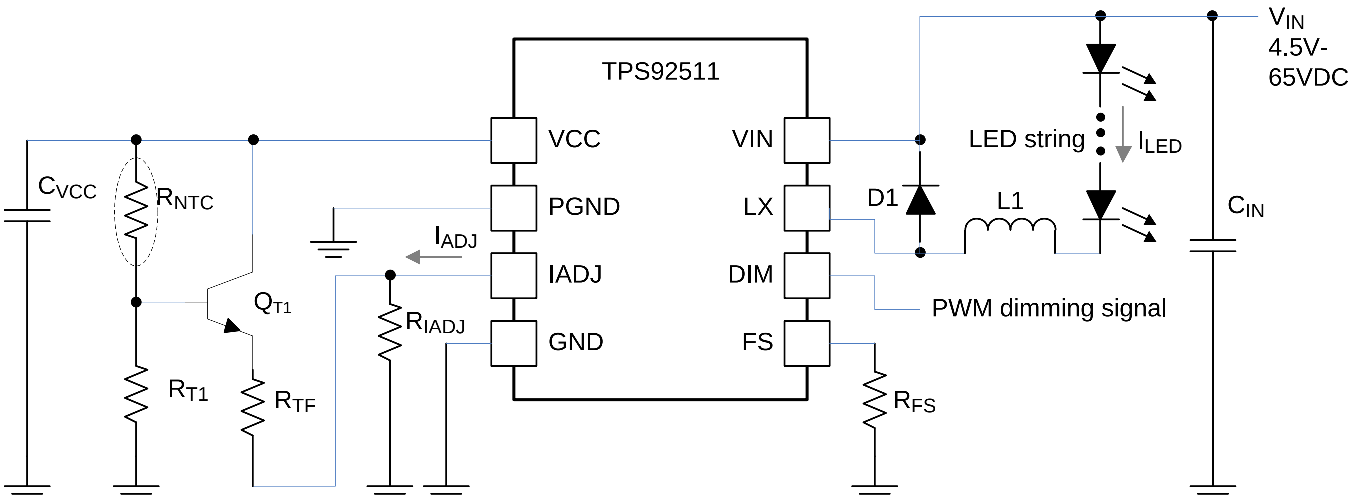


图 20. Circuit Configuration for Thermal Foldback

7.3.14 EMI Consideration

Conductive and radiative EMI can be major concerns for lighting applications. The TPS92511 application circuit can be designed for the EN 55022 class B standard by adding a few external components, as shown in 图 21. The input filter which consists of an inductor L_2 and two capacitors C_{IN2} and C_{IN3} takes care of the conductive EMI, while the output capacitor C_{LED} and the ferrite bead FB_1 which inserts between the LX pin and D_1 take care of the radiative EMI.

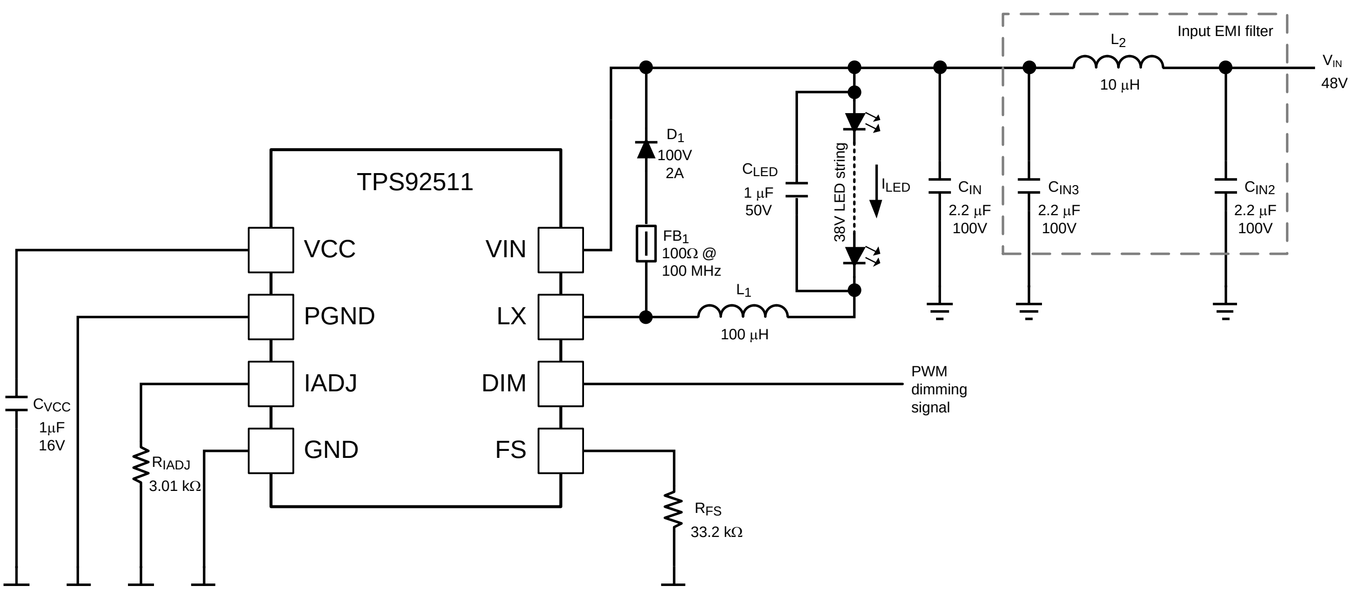


图 21. Circuit Configuration with EMI Design Consideration

7.4 Device Functional Modes

7.4.1 Operation with V_{IN} < 4.5 V (minimum V_{IN})

For the typical application circuit, when the input voltage drops so that the VCC voltage regulator is under drop-out mode, and the VCC voltage drops below the “VCC UVLO Lower Threshold” (typically 3.48V), the switching of the main MOSFET is stopped, and the LED current will become zero. At the same time, the voltages of both the FS and IADJ pins will become zero .

When the input voltage increases from zero and the VCC voltage is increased to cross over the “VCC UVLO Upper Threshold” (typically 3.75V), the voltages on the FS and IADJ pins will rise to their regulation voltage (typically 1.25V), the switching of the main MOSFET is started upon the DIM pin voltage is HIGH, and the LED current will ramp up to its preset value set by R_{IADJ}.

7.4.2 Operation with DIM control

For the typical application circuit, when the VCC voltage is not under UVLO condition, the switching of the main MOSFET is enabled and the LED current is conducted if the DIM pin voltage is higher than the “DIM Pin Upper Threshold” (typically 1V).

Alternaltively, the switching is disabled and the LED current is cut off if the voltage of the DIM pin is lower than the “DIM Pin Lower Threshold” (typically 0.675V).

7.4.3 Linear Mode

When the VCC voltage is not under UVLO condition and the voltage on the FS pin is forced to be higher than 4.2V but lower than 5V, the switching of the main MOSFET is disabled, and the TPS92511 is working in the Linear Mode. In the Linear Mode, if the voltage on the DIM pin is higher than the “DIM Pin Upper Threshold” (typically 1V), the TPS92511 will regulate the LX pin in-going current according to the preset value set by R_{IADJ}. Alternatively, if the voltage on the DIM pin is lower than the “DIM Pin Lower Threshold” (typically 0.675V), the LX pin will open and its in-going current will become zero.

Below is the simple configuration to have the TPS92511 working as a linear current shunt regulator.

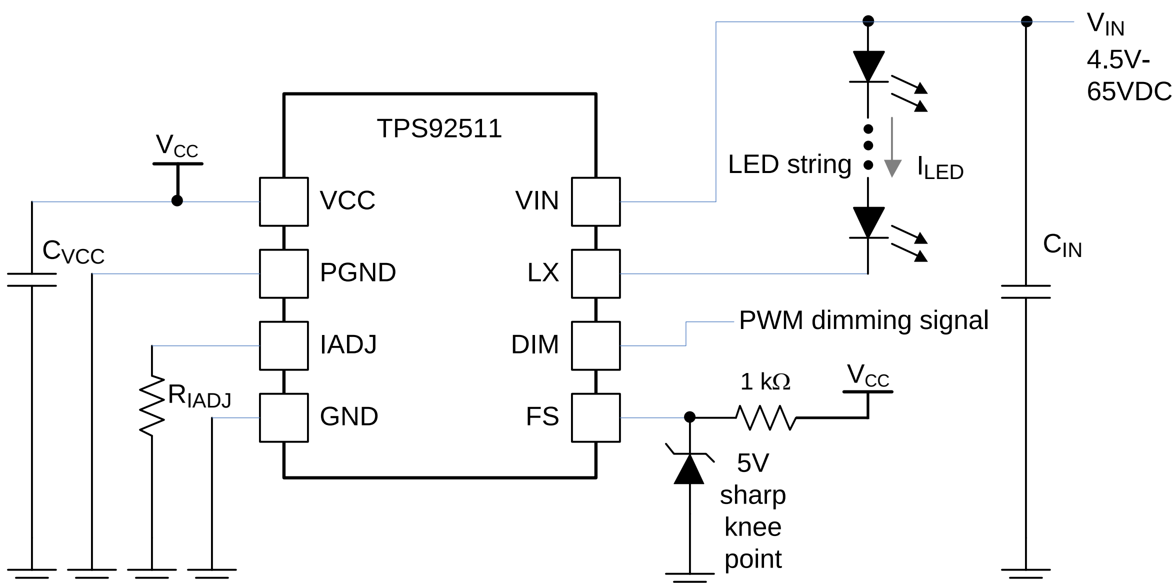


图 22. Circuit Configuration for Working as a Linear Current Shunt Regulator

8 Application and Implementation

8.1 Application Information

The TPS92511 is an LED driver which provides a regulated output current to drive a single string of LED with the forward voltage lower than the input voltage. The following procedures design a TPS92511 application circuit with an input voltage of 48V, driving an LED string of 38V at an LED current of 0.5A. The switching frequency is 300 kHz.

8.2 Typical Application

8.2.1 TPS92511 LED driver for 12 LEDs at 0.5A

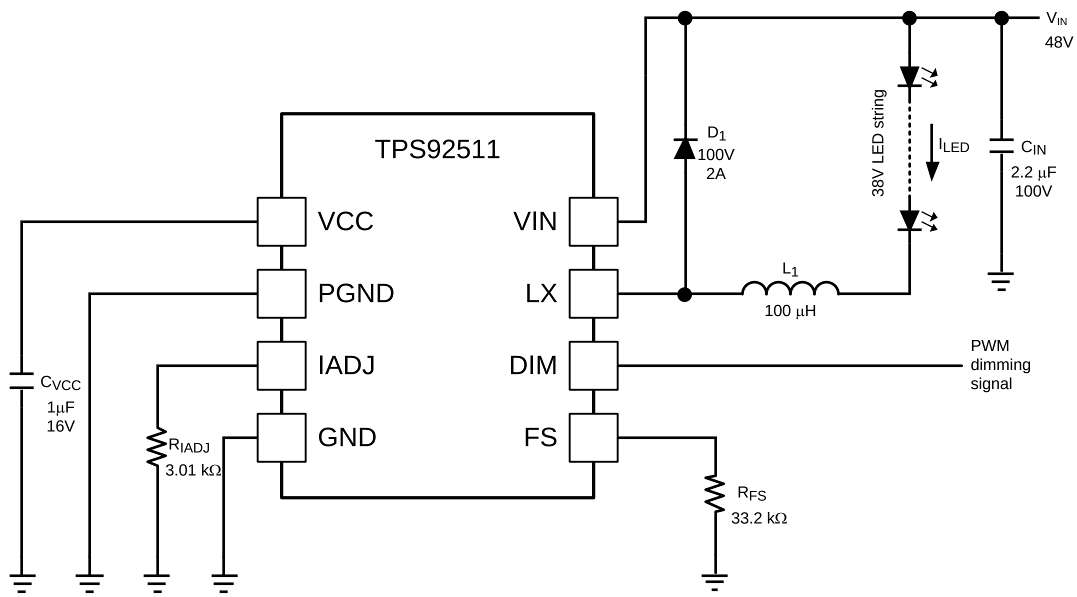


图 23. Application Circuit of TPS92511 (f_{SW} = 300 kHz and I_{LED} = 0.5A)

Typical Application (接下页)

8.2.1.1 Design Requirements

表 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	43V to 53V
LED current	0.5A
LED string forward voltage	38V
Operating frequency	300 kHz

8.2.1.2 Detailed Design Procedure

C_{IN} : The function of the input capacitor C_{IN} is to reduce the input voltage ripple. Ceramic capacitors are recommended owing to the concern of product lifetime. A 100V 2.2 µF ceramic capacitor is selected in this circuit.

C_{VCC} : The capacitor on the VCC pin provides noise filtering and stabilizes the internal regulator. It also prevents false triggering of the VCC UVLO. C_{VCC} is recommended to be a 1 µF good quality and low ESR ceramic capacitor.

D_1 : The diode D_1 should have a reverse voltage larger than V_{IN} in the floating buck topology. In this circuit, a 100V diode is selected.

R_{FS} and R_{IADJ} : In this circuit, the switching frequency and LED current are designed to be 300 kHz and 0.5A. From 表 1 and 表 2, R_{FS} is 33.2 kΩ and R_{IADJ} is 3.01 kΩ.

L_1 : The selection of inductor mainly affects the inductor current ripple. In this circuit, we design the peak to peak inductor current ripple to be 50% of I_{LED}, i.e. 0.25A. From (6), L_1 is calculated to be 106 µH, and a 100 µH inductor is selected.

8.2.1.3 Application Curves

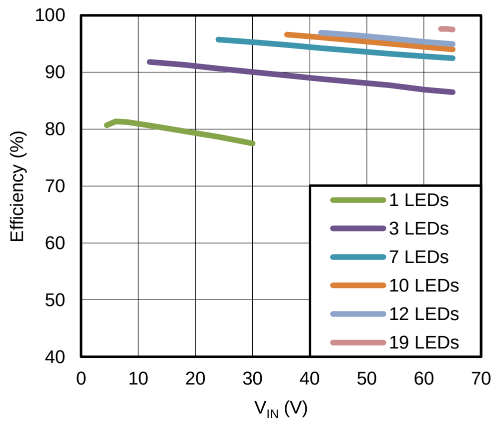


图 24. Efficiency vs V_{IN}

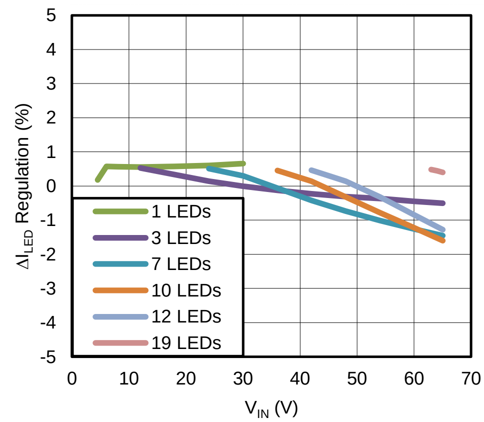


图 25. LED Current Regulation vs V_{IN}

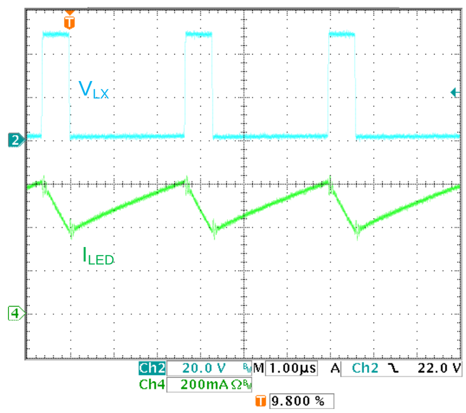


图 26. Steady State Operation

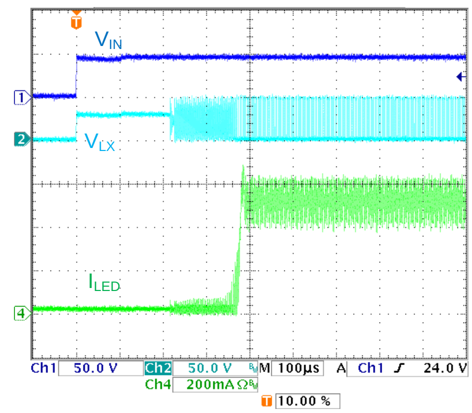


图 27. Power Up

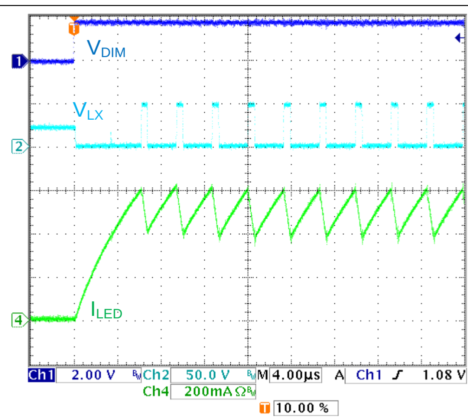


图 28. PWM Dimming (V_{DIM} Rising)

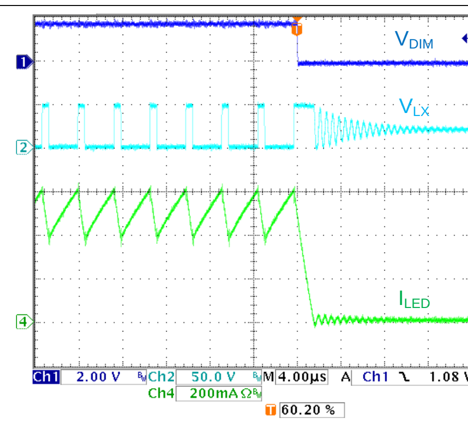


图 29. PWM Dimming (V_{DIM} Falling)

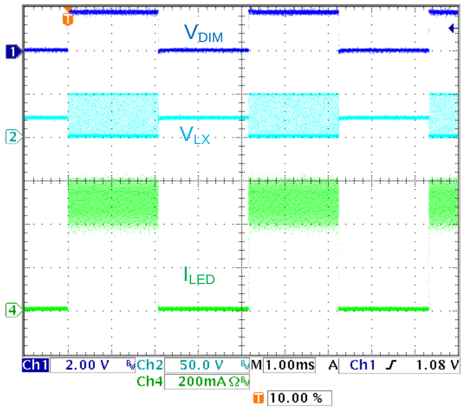


图 30. PWM Dimming (f_{DIM} = 1 kHz, 50% Duty Cycle)

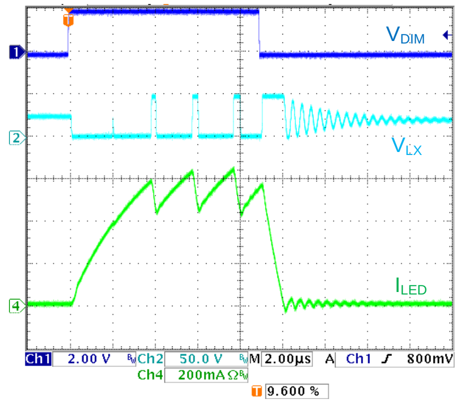


图 31. PWM Dimming (9 µs dimming pulse) (f_{SW} = 500kHz, L_1 = 68 µH)

9 Power Supply Recommendation

This device is designed to operate from an input voltage supply range between 4.5 V and 65 V. The input supply should be well regulated. If the input supply is located more than a few inches from the TPS92511 application board, additional bulk capacitance may be required in addition to the input capacitor. A ceramic capacitor with a value of 2.2 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

- The PCB layout of the TPS92511 application circuit plays an important role in optimizing the performance.
- The external components should be placed as close to the TPS92511 as possible to minimize resistance and parasitic inductance of copper traces.
- For example, D_1 and L_1 should be near the LX pin, and C_{VCC} should be near the VCC pin, and the connecting copper traces are short and thick.
- The exposed pad of the TPS92511, which is internally connected to the die substrate, should be connect to a ground plane, and the plane should be extended as much as possible on the same copper layer around the TPS92511.
- Using numerous vias beneath the exposed pad to dissipate heat to another copper layer is also a good practice.

10.2 Layout Example

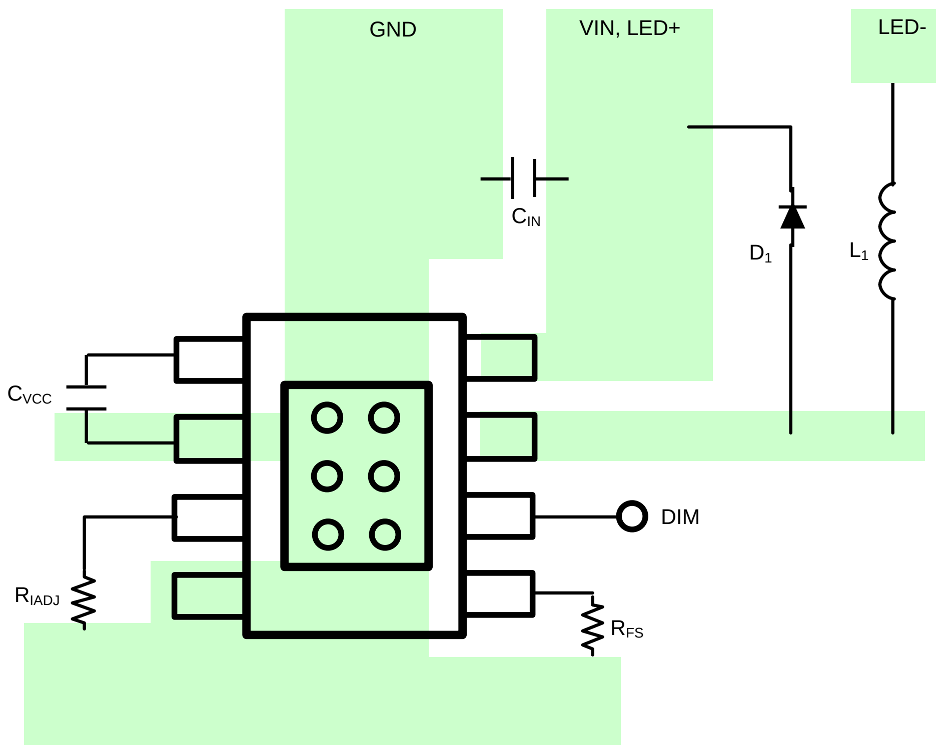


图 32. TPS92511 Board Layout

10.2.1 Thermal Consideration

Ψ_{JT} (shown in session 6.4 Thermal Information) is a relatively small value for package with exposed pad since most of the heat is dissipated through the exposed pad to the copper plate of the PCB (assuming optimized PCB layout), relatively little heat goes to the top of the device. The top of the device mold compound temperature is physically close to the device junction temperature.

For example, a 30W output TPS92511 end system at 95% power efficiency (can be estimated from the efficiency curves of Figure 13), power loss is 1.6W. Assuming all the heat is generated from the TPS92511 (which is true for high V_{LED}), and assuming half of the heat generated is dissipated through the top of the device. Now Ψ_{JT} is 11 °C/W, the device junction temperature is estimated to be higher than the package's top-surface temperature by 11 x 1.6 x 0.5 = 8.8 (°C). If the package top-surface temperature is measured to be 90 °C (for example by an IR camera), the device junction temperature is around 99 °C, which is within the 125°C maximum junction temperature requirement with margin.

11 器件和文档支持

11.1 商标

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11.2 静电放电警告

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11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92511DDA	ACTIVE	SO PowerPAD	DDA	8	95	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	92511	Samples
TPS92511DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	92511	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
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PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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