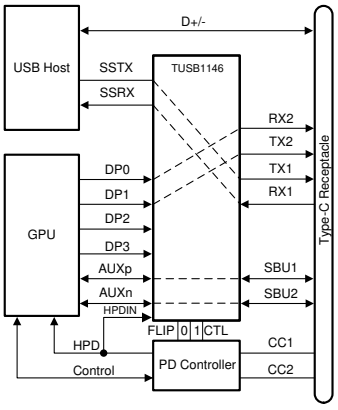
TUSB1146 USB Type-C™ DisplayPort™ Alt Mode 10-Gbps Linear Redriver Crosspoint Switch

1 Features

- USB Type-C crosspoint switch supporting
  - USB 3.2 SSP + 2 DisplayPort Lanes
  - 4 DisplayPort Lanes
- USB 3.2 x1 Gen 1/Gen 2 up to 10 Gbps
- VESA®DisplayPort 2.0 up to 10 Gbps (UHBR10)
- Supports D_DFP pin assignments C, D, and E
- Choice between adaptive or fixed equalization for USB DFP receivers.
- Linear and limited redriver supported on UFP transmitter
- Limited redriver option offers both TX voltage swing and TX equalization control
  - 4 Levels of TX voltage swing from 800 mVpp up to 1100 mVpp
  - TX pre-shoot and de-emphasis
- Ultra-low-power architecture
- Up to 12 dB equalization at 5 GHz
- Transparent to DisplayPort link training
- Configuration through GPIO or I^2C
- Intel proprietary DCI capability on USB Type-C for closed chassis debugging
- Hot-Plug capable
- Industrial temperature range: –40 ºC to 85 ºC (TUSB1146I)
- Commercial temperature range: 0 ºC to 70 ºC (TUSB1146)
- 4 mm x 6 mm, 0.4 mm Pitch WQFN package

Simplified Schematics



2 Applications

- Notebooks and desktops
- Tablets
- Docking Stations

3 Description

The TUSB1146 is a VESA USB Type-C™ Alt Mode redriving switch supporting USB 3.2 data rates up to 10 Gbps and DisplayPort 2.0 up to 10 Gbps for downstream facing port (Host). The device is used for configurations C, D, and E from the VESA DisplayPort Alt Mode on USB Type-C standard. This protocol-agnostic linear redriver is also capable of supporting other USB Type-C Alt Mode interfaces such as HDMI Alt Mode.

The TUSB1146 incorporates an innovative, adaptive receiver equalization (AEQ) feature. The AEQ feature will automatically find the best ISI compensation setting between the USB device and the TUSB1146. Because the AEQ finds the best setting, interoperability between a USB Host and USB Device is vastly improved. The TUSB1146 operates on a single 3.3-V supply and comes in a commercial temperature range and industrial temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB1146	WQFN (40)	4.00 mm x 6.00 mm
TUSB1146I		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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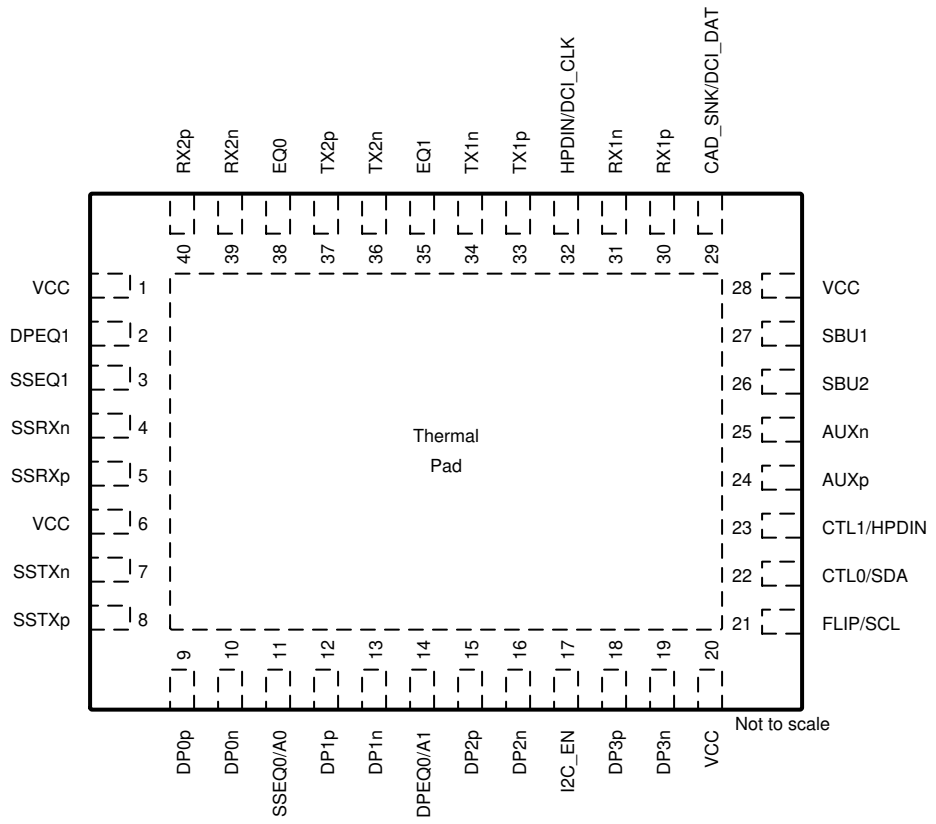
4 Revision History

DATE	REVISION	NOTES
April 2020	*	Initial release.

5 TUSB1146 Pin Configuration and Functions

RNQ Package
40-Pin (WQFN)
Top View



TUSB1146 Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DP0p	9	Diff I	DP Differential positive input for DisplayPort Lane 0.
DP0n	10	Diff I	DP Differential negative input for DisplayPort Lane 0.
DP1p	12	Diff I	DP Differential positive input for DisplayPort Lane 1.
DP1n	13	Diff I	DP Differential negative input for DisplayPort Lane 1.
DP2p	15	Diff I	DP Differential positive input for DisplayPort Lane 2.
DP2n	16	Diff I	DP Differential negative input for DisplayPort Lane 2.
DP3p	18	Diff I	DP Differential positive input for DisplayPort Lane 3.
DP3n	19	Diff I	DP Differential negative input for DisplayPort Lane 3.
RX1n	31	Diff I/O	Differential negative output for DisplayPort or differential negative input for USB3.1 Downstream Facing port.
RX1p	30	Diff I/O	Differential positive output for DisplayPort or differential positive input for USB3.1 Downstream Facing port.
TX1n	34	Diff O	Differential negative output for DisplayPort or USB3.1 downstream facing port.
TX1p	33	Diff O	Differential positive output for DisplayPort or USB 3.1 downstream facing port.
TX2p	37	Diff O	Differential positive output for DisplayPort or USB 3.1 downstream facing port.
TX2n	36	Diff O	Differential negative output for DisplayPort or USB 3.1 downstream facing port.

TUSB1146 Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
RX2p	40	Diff I/O	Differential positive output for DisplayPort or differential positive input for USB3.1 Downstream Facing port.
RX2n	39	Diff I/O	Differential negative output for DisplayPort or differential negative input for USB3.1 Downstream Facing port.
SSTXp	8	Diff I	Differential positive input for USB3.1 upstream facing port.
SSTXn	7	Diff I	Differential negative input for USB3.1 upstream facing port.
SSRXp	5	Diff O	Differential positive output for USB3.1 upstream facing port.
SSRXn	4	Diff O	Differential negative output for USB3.1 upstream facing port.
EQ1	35	4 Level I	This pin along with EQ0 sets the USB receiver equalizer gain for downstream facing RX1 and RX2 when USB used. Refer to Table 7 for details on the equalization setting.
EQ0	38	4 Level I	This pin along with EQ1 sets the USB receiver equalizer gain for downstream facing RX1 and RX2 when USB used. Refer to Table 7 for details on the equalization setting.
CAD_SNK/DCI_DAT(1)	29	I/O (PD)	When I2C_EN ! = 0, this pin functions as DCI data output Leave open if not used. When I2C_EN = 0 , this pin is CAD_SNK (L = AUX snoop enabled and H = AUX snoop disabled with all lanes active).
HPDIN/DCI_CLK(1)	32	I/O (PD)	When I2C_EN ! = 0, this pin functions as DCI clock output Leave open if not used. When I2C_EN = 0, this pin is an input for Hot Plug Detect received from DisplayPort sink. When HPDIN is Low for greater than 2ms, all DisplayPort lanes are disabled while the AUX to SBU switch will remain closed.
I2C_EN	17	4 Level I	I^2C Programming Mode or GPIO Programming Select. 0 = GPIO mode (I^2C disabled) with adaptive EQ disabled. R = TI Test Mode (I^2C enabled at 3.3 V) F = I^2C enabled at 1.8 V when EQ0 = "0" and EQ1 = "0". All other combinations of EQ0 and EQ1 are reserved. 1 = I^2C enabled at 3.3 V.
SBU1	27	I/O, CMOS	SBU1. This pin should be DC coupled to the SBU1 pin on the Type-C receptacle. A 2-M ohm resistor to GND is also recommended.
SBU2	26	I/O, CMOS	SBU2. This pin should be DC coupled to the SBU2 pin on the Type-C receptacle. A 2-M ohm resistor to GND is also recommended.
AUXp	24	I/O, CMOS	AUXp. DisplayPort AUX positive I/O connected to the DisplayPort source through a AC coupling capacitor. In addition to AC coupling capacitor, this pin also requires a 100K resistor to GND. This pin along with AUXN is used by the TUSB1146 for AUX snooping and is routed to SBU1/2 based on the orientation of the Type-C.
AUXn	25	I/O, CMOS	AUXn. DisplayPort AUX negative I/O connected to the DisplayPort source through a AC coupling capacitor. In addition to AC coupling capacitor, this pin also requires a 100K resistor to VCC (3.3V). This pin along with AUXP is used by the TUSB1146 for AUX snooping and is routed to SBU1/2 based on the orientation of the Type-C.
DPEQ1	2	4 Level I	DisplayPort Receiver EQ. Along with DPEQ0, this pin selects the DisplayPort receiver equalization gain. Refer to Table 9 for details on the equalization settings.
DPEQ0/A1	14	4 Level I	DisplayPort Receiver EQ. Along with DPEQ1, this pin selects the DisplayPort receiver equalization gain. When I2C_EN is not '0', this pin will also set the TUSB1146 I^2C address. Refer to Table 9 for details on the equalization settings.
SSEQ1	3	4 Level I	Along with SSEQ0, sets the USB receiver equalizer gain for upstream facing SSTXP/N. Refer to Table 8 for details on the equalization settings.
SSEQ0/A0	11	4 Level I	Along with SSEQ1, sets the USB receiver equalizer gain for upstream facing SSTXP/N. When I2C_EN is not '0', this pin will also set the TUSB1146 I^2C address. Refer to Table 8 for details on the equalization settings.
FLIP/SCL	21	2 Level I	When I2C_EN='0' this is Flip control pin, otherwise this pin is I^2C clock. . When used for I^2C clock pull-up to I^2C master's VCC I2C supply.
CTL0/SDA	22	2 Level I	When I2C_EN='0' this is a USB3.1 Switch control pin, otherwise this pin is I^2C data. When used for I^2C data pullup to I^2C master's VCC I2C supply.
CTL1/HPDIN	23	2 Level I (Failsafe) (PD)	DP Alt mode Switch Control Pin. When I2C_EN = '0', this pin will enable or disable DisplayPort functionality. Otherwise, when I2C_EN is not "0", DisplayPort functionality is enabled and disabled through I^2C registers. L = DisplayPort Disabled. H = DisplayPort Enabled. When I2C_EN is not "0" this pin is an input for Hot Plug Detect received from DisplayPort sink. When this HPDIN is Low for greater than 2 ms, all DisplayPort lanes are disabled and AUX to SBU switch will remain closed.
VCC	1, 6, 20, 28	P	3.3-V Power Supply
Thermal Pad		G	Ground

(1) Not a fail-safe I/O. Actively driving pin high while VCC is removed results in leakage voltage on VCC pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage Range	V_{CC}	–0.3	4	V
Voltage Range at any input or output pin	Differential voltage between positive and negative inputs	-2.5	2.5	V
	Voltage at differential inputs	–0.5	4	V
	CMOS Inputs	–0.5	4	V
Maximum junction temperature, T_J	TUSB1146		105	°C
	TUSB1146I		125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Main power supply	3.0	3.3	3.6	V
	Main supply ramp requirement	0.1		50	ms
$V_{(I2C)}$	Supply that external resistors are pulled up to on SDA and SCL	1.7		3.6	V
$V_{(PSN)}$	Supply Noise on V_{CC} pins (less than 4MHz)			100	mV
T_A	TUSB1146 Operating free-air temperature	0		70	°C
	TUSB1146I Operating free-air temperature	-40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TUSB1146 RNQ (WQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	°C/W

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and ICPackage Thermal Metrics* application report.

6.5 Power Supply Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{CC(ACTIVE-USB)}$	Average active power USB Only	Link in U0 with GEN2 data transmission; EQ control pins = NC; PRBS7 pattern at 10 Gbps, V_{ID} = 1000 mV_{PP} ; LINR_L3; CTL1 = L; CTL0 = H		270		mW

Power Supply Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{CC(ACTIVE-USB-DP1)}$	Average active power USB + 2 Lane DP	Link in U0 with GEN2 data transmission; EQ control pins = NC; PRBS7 pattern at 10 Gbps, V_{ID} = 1000 mV_{PP}; LINR_L3; CTL1 = H; CTL0 = H		520		mW
$P_{CC(ACTIVE--4DP)}$	Average active power 4 Lane DP Only	Four active DP lanes operating at 8.1Gbps; PRBS7 pattern; CTL1 = H; CTL0 = L; LINR_L3;		500		mW
$P_{CC(NC-USB)}$	Average power with no connection	No GEN2 device is connected to TXP/TXN; CTL1 = L; CTL0 = H;		3.5		mW
$P_{CC(U2U3)}$	Average power in U2/U3	Link in U2 or U3; USB Mode Only; CTL1 = L; CTL0 = H;		2.0		mW
$P_{CC(HPDLOW--4DP)}$	Power 4 Lane DP Only when HPDIN = L	CTL1 = H; CTL0 = L; HPDIN = L;		0.475		mW
$P_{CC(DISABLED-I2C)}$	Device Diabled power in I2C Mode	I2C_EN != 0; HPDIN = L;		0.122		mW
$P_{CC(DISABLED)}$	Device Diabled power	CTL1 = L; CTL0 = L; I2C_EN = 0; HPDIN = L;		0.110		mW

6.6 Control I/O DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4-level Inputs						
4-Level V_{TH}	Threshold 0 / R	V_{CC} = 3.3 V		0.55		V
4-Level V_{TH}	Threshold R/ Float	V_{CC} = 3.3 V		1.65		V
4-Level V_{TH}	Threshold Float / 1	V_{CC33} = 3.3 V		2.7		V
I_{IH}	High level input current	V_{CC} = 3.6 V; V_{IN} = 3.6 V	20		60	µA
I_{IL}	Low level input current	V_{CC} = 3.6 V; V_{IN} = 0 V	–100		-40	µA
R_{PU}	Internal pull-up resistance			48		kΩ
R_{PD}	Internal pull-down resistance			98		kΩ
2-State CMOS Input (CTL0, CTL1, FLIP). CTL0 and FLIP are Failsafe.						
V_{IH}	High-level input voltage	V_{CC} = 3.0V	2		3.6	V
V_{IL}	Low-level input voltage	V_{CC} = 3.6V	0		0.8	V
R_{PD}	Internal pull-down resistance for HPDIN, CADSNK		400	500	600	kΩ
R_{PD}	Internal pull-down resistance for CTL1		300	400	500	kΩ
I_{IH_CTL1}	High-level input current for CTL1	V_{IN} = 3.6 V	–11		11	µA
I_{IL_CTL1}	Low-level input current for CTL1	V_{IN} = GND, V_{CC} = 3.6 V	–1		1	µA
$I_{IH\_HPD\_CAD}$	High-level input current for HPDIN, CADSNK	V_{IN} = 3.6 V	–11		11	µA
$I_{IL\_HPD\_CAD}$	Low-level input current for HPDIN, CADSNK	V_{IN} = GND, V_{CC} = 3.6 V	–1		1	µA
$I_{IH\_CTL0\_FLIP}$	High-level input current for CTL0 and FLIP	V_{IN} = 3.6 V; I2C_EN = 0	–1		1	µA
$I_{IL\_CTL0\_FLIP}$	Low-level input current for CTL0 and FLIP	V_{IN} = GND, V_{CC} = 3.6 V; I2C_EN = 0;	–1		1	µA
I^2C Control Pins (SCL, SDA)						
V_{IH_3p3V}	High-level input voltage when configured for 3.3V I2C level	I2C_EN = 1	2.0		3.6	V
V_{IL_3p3V}	Low-level input voltage when configured for 3.3V I2C level	I2C_EN = 1	0		0.8	V
V_{IH_1p8V}	High-level input voltage when configured for 1.8V I2C level	I2C_EN = F	1.2			V
V_{IL_1p8V}	Low-level input voltage when configured for 1.8V I2C level	I2C_EN = F	0		0.6	V
V_{OL}	Low-level output voltage	I2C_EN = 0; I_{OL} = 6 mA	0		0.4	V

Control I/O DC Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OL}	Low-level output current	I2C_EN = 0; V_{OL} = 0.4 V	20			mA
$I_{I(I2C)}$	Input current	0.1 x $V_{(I2C)}$ < Input voltage < 3.3 V	–1		1	µA
$C_{I(I2C)}$	Input capacitance				10	pF
$C_{(I2C\_FM+\_BUS)}$	I2C bus capacitance for FM+ (1MHz)				150	pF
$C_{(I2C\_FM\_BUS)}$	I2C bus capacitance for FM (400kHz)				150	pF
$R_{(EXT\_I2C\_FM+)}$	External resistors on both SDA and SCL when operating at FM+ (1MHz)	$C_{(I2C\_FM+\_BUS)}$ = 150 pF	620	820	910	Ω
$R_{(EXT\_I2C\_FM)}$	External resistors on both SDA and SCL when operating at FM (400kHz)	$C_{(I2C\_FM\_BUS)}$ = 150 pF	620	1500	2200	Ω

6.7 USB and DP Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB Gen 2 Differential Receiver (RX1p/n, RX2p/n, SSTXp/n)						
$V_{(RX-DIFF-PP)}$	Input differential peak-peak voltage swing linear dynamic range	AC-coupled differential peak-to-peak signal measured post CTLE through a reference channel		1200		mVpp
$V_{(RX-DC-CM)}$	Common-mode voltage bias in the receiver (DC)			0		V
$V_{RX\_CM-INST}$	Max Instantaneous RX DC common mode voltage change under all operating conditions (OFF to ON, Disabled to USB, etc…)	Measured at non-TUSB1146 side of AC coupling capacitor with 200-kΩ load.	-200		500	mV
$R_{(RX-DIFF-DC)}$	Differential input impedance (DC)	Present after a GEN2 device is detected on TXP/TXN	72	90	120	Ω
$R_{(RX-CM-DC)}$	Receiver DC common mode impedance	Present after a GEN2 device is detected on TXP/TXN	18		30	Ω
$Z_{(RX-HIGH-IMP-DC-POS)}$	Common-mode input impedance with termination disabled (DC)	Present when no GEN2 device is detected on TXP/TXN. Measured over the range of 0-500mV with respect to GND.	25			kΩ
$V_{(SIGNAL-DET-DIFF-PP)}$	Input differential peak-to-peak signal detect assert level	At 10 Gbps, no input loss, PRBS7 pattern		80		mV
$V_{(RX-IDLE-DET-DIFF-PP)}$	Input differential peak-to-peak signal detect de-assert Level	At 10 Gbps, no input loss, PRBS7 pattern		60		mV
$V_{(RX-LFPS-DET-DIFF-PP)}$	Low frequency periodic signaling (LFPS) detect threshold	Below the minimum is squelched	100		300	mV
$V_{(RX-CM-AC-P)}$	Peak RX AC common-mode voltage	Measured at package pin			150	mV
$C_{(RX)}$	RX input capacitance to GND	At 5 GHz;		0.88	1	pF
$R_{L(RX-DIFF)}$	Differential return Loss	50 MHz – 1.25 GHz at 90 Ω;		–19		dB
		5 GHz at 90 Ω;		–10		dB
$R_{L(RX-CM)}$	Common-mode return loss	50 MHz – 5 GHz at 90 Ω;		–10		dB
E_{Q_SSTX15}	SSTX Receiver equalization at 5 GHz	FLIPSEL = 0; SSEQ_SEL = 15;		11.5		dB
E_{Q_RX15}	RX1 Receiver equalization at 5 GHz	FLIPSEL = 0; EQ1_SEL = 15;		11.0		dB
$C_{AC-USB1}$	Required external AC capacitor on SSTX		75		265	nF
$C_{AC-USB2}$	Optional external AC capacitor on RX1 and RX2.		297		363	nF
USB Gen 2 Differential Transmitter (TX1p/n, TX2p/n, SSRXp/n)						
$V_{TX(DIFF-PP)}$	Transmitter dynamic differential voltage swing range.			1200		mVpp
$V_{TX(RCV-DETECT)}$	Amount of voltage change allowed during receiver detection				600	mV
$V_{TX-CM-INST-ONOFF}$	Max Instantaneous TX DC common mode voltage change under operating condition: OFF to ON, ON to OFF, during Rx.Detect; Disconnect to U0, U2/U3 to U0.	Measured single-ended at non-TUSB1146 side of AC coupling capacitor with 200-kΩ load.	-500		800	mV
$V_{TX(CM-IDLE-DELTA)}$	Transmitter idle common-mode voltage change while in U2/U3 and not actively transmitting LFPS		–300		600	mV
$V_{TX(DC-CM)}$	Common-mode voltage bias in the transmitter (DC)		0		1	V
$V_{TX(CM-AC-PP-ACTIVE)}$	Tx AC common-mode voltage active	Max mismatch from Txp + Txn for both time and amplitude			100	mVpp
$V_{TX(IDLE-DIFF-AC-PP)}$	AC electrical idle differential peak-to-peak output voltage	At package pins	0		10	mV
$V_{TX(CM-DC-ACTIVE-IDLE-DELTA)}$	Absolute DC common-mode voltage between U1 and U0	At package pin			200	mV
$R_{TX(DIFF)}$	Differential impedance of the driver		80	90	120	Ω
$R_{TX(CM)}$	Common-mode impedance of the driver	Measured with respect to AC ground over 0–500 mV	18		30	Ω

USB and DP Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{SSRX-LIMITED-VODL0}$	SSRX differential peak-to-peak voltage when configured for limited redriver and LINR_L0	TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 0;		800		mVpp
$V_{SSRX-LIMITED-VODL1}$	SSRX differential peak-to-peak voltage when configured for limited redriver and LINR_L1	TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 0;		900		mVpp
$V_{SSRX-LIMITED-VODL2}$	SSRX differential peak-to-peak voltage when configured for limited redriver and LINR_L2	TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 0;		1000		mVpp
$V_{SSRX-LIMITED-VODL3}$	SSRX differential peak-to-peak voltage when configured for limited redriver and LINR_L3	TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 0;		1100		mVpp
$V_{SSRX-DE-RATIO0}$	SSRX de-emphasis when configured for limited redriver and de-emphasis enabled.	TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 1; TX_DEEPHASIS = 2'b00; USB_SSRX_VOD = 2'b00 (LINR_L3); Refer to Figure 25		-1.5		dB
$V_{SSRX-DE-RATIO1}$	SSRX de-emphasis when configured for limited redriver and de-emphasis enabled.	TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 1; TX_DEEPHASIS = 2'b01; USB_SSRX_VOD = 2'b00 (LINR_L3); Refer to Figure 25		-2.1		dB
$V_{SSRX-DE-RATIO2}$	SSRX de-emphasis when configured for limited redriver and de-emphasis enabled.	TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 1; TX_DEEPHASIS = 2'b10; USB_SSRX_VOD = 2'b00 (LINR_L3); Refer to Figure 25		-3.2		dB
$V_{SSRX-DE-RATIO3}$	SSRX de-emphasis when configured for limited redriver and de-emphasis enabled.	TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 1; TX_DEEPHASIS = 2'b11; USB_SSRX_VOD = 2'b00 (LINR_L3); Refer to Figure 25		-3.8		dB
$V_{SSRX-PRESH-RATIO0}$	SSRX pre-shoot level when configured for limited redriver and pre-shoot enabled.	TX_PRESHOOT_EN = 1; TX_DEEMPHASIS_EN = 0; TX_PRESHOOT = 2'b00; USB_SSRX_VOD = 2'b00 (LINR_L3); Refer to Figure 26		1.5		dB
$V_{SSRX-PRESH-RATIO1}$	SSRX pre-shoot level when configured for limited redriver and pre-shoot enabled.	TX_PRESHOOT_EN = 1; TX_DEEMPHASIS_EN = 0; TX_PRESHOOT = 2'b01; USB_SSRX_VOD = 2'b00 (LINR_L3); Refer to Figure 26		2.0		dB
$V_{SSRX-PRESH-RATIO2}$	SSRX pre-shoot level when configured for limited redriver and pre-shoot enabled.	TX_PRESHOOT_EN = 1; TX_DEEMPHASIS_EN = 0; TX_PRESHOOT = 2'b10; USB_SSRX_VOD = 2'b00 (LINR_L3); Refer to Figure 26		2.3		dB
$V_{SSRX-PRESH-RATIO3}$	SSRX pre-shoot level when configured for limited redriver and pre-shoot enabled.	TX_PRESHOOT_EN = 1; TX_DEEMPHASIS_EN = 0; TX_PRESHOOT = 2'b11; USB_SSRX_VOD = 2'b00 (LINR_L3); Refer to Figure 26		2.8		dB
$I_{TX(SHORT)}$	TX short circuit current	TX± shorted to GND			40	mA
$C_{TX(PARASITIC)}$	TX input capacitance for return loss	At package pins, at 5 GHz		0.9	1.25	pF
$R_{LTX(DIFF)}$	Differential return loss	50 MHz – 1.25 GHz at 90 Ω		-30		dB
		5 GHz at 90 Ω		-21		dB
$R_{LTX(CM)}$	Common-mode return loss	50 MHz – 5 GHz at 90 Ω		-10		dB
$C_{TX-AC(COUPLING)}$	External required AC coupling capacitor		75		265	nF
AC Characteristics						
Crosstalk	Differential crosstalk between TX and RX signal pairs	at 5 GHz; EQ = 0;		–30		dB
$CP_{LF-LINRL0}$	Low-frequency 1-dB compression point at LINR_L0 setting.	At 100 MHz, 200 mVpp < V_{ID} < 1200 mVpp		600		mVpp

USB and DP Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$CP_{HF-LINRL0}$	High-frequency 1-dB compression point at LINR_L0 setting.	At 5 GHz, 200 mVpp < V_{ID} < 1200 mVpp		550		mVpp
$CP_{LF-LINRL1}$	Low-frequency 1-dB compression point at LINR_L1 setting.	At 100 MHz, 200 mVpp < V_{ID} < 1200 mVpp		700		mVpp
$CP_{HF-LINRL1}$	High-frequency 1-dB compression point at LINR_L1 setting.	At 5 GHz, 200 mVpp < V_{ID} < 1200 mVpp		650		mVpp
$CP_{LF-LINRL2}$	Low-frequency 1-dB compression point at LINR_L2 setting.	At 100 MHz, 200 mVpp < V_{ID} < 1200 mVpp		800		mVpp
$CP_{HF-LINRL2}$	High-frequency 1-dB compression point at LINR_L2 setting.	At 5 GHz, 200 mVpp < V_{ID} < 1200 mVpp		750		mVpp
$CP_{LF-LINRL3}$	Low-frequency 1-dB compression point at LINR_L3 setting.	At 100 MHz, 200 mVpp < V_{ID} < 1200 mVpp		900		mVpp
$CP_{HF-LINRL3}$	High-frequency 1-dB compression point at LINR_L3 setting.	At 5 GHz, 200 mVpp < V_{ID} < 1200 mVpp		830		mVpp
f_{LF}	Low frequency cutoff	200 mV_{PP}< V_{ID} < 1200 mV_{PP}		20	50	kHz
$t_{TX\_DJ\_USB}$	TX output deterministic residual jitter when operating in USB mode.	Optimual EQ setting; 12-in prechannel (SDD21 = -11.2dB); 1.6-in post channel (SDD21 = -1.8dB); PRBS7; 10 Gbps		.07		UI
$t_{TX\_DJ\_DP}$	TX output deterministic residual jitter when operating in DP mode.	Optimual EQ setting;12-in prechannel (SDD21 = -11.2dB); 1.6-in post channel (SDD21 = -1.8dB); PRBS7; 8.1 Gbps		.04		UI
DisplayPort Receiver (DP[3:0]p/n)						
$V_{ID(PP)}$	Peak-to-peak input differential dynamic voltage range			1400		V
V_{IC}	Input common mode voltage		0	1.75	2	V
$V_{RX\_CM-INST}$	Max Instantaneous RX DC common mode voltage change under all operating conditions (OFF to ON, Disabled to 4DP, etc…)	Measured single-ended at non-TUSB1146 side of AC coupling capacitor with 50-Ω load.	-300		500	mV
d_R	Data rate				10	Gbps
$R_{(ti)}$	Input termination resistance		75	90	110	Ω
$C_{(AC)}$	External required AC coupling capacitance		75		265	nF
E_{Q_DP15}	DP0 Receiver equalization at 4.05 GHz	FLIPSEL = 0; DP0EQ_SEL = 15;		12		dB
E_{Q_DP15}	DP0 Receiver equalization at 5 GHz	FLIPSEL = 0; DP0EQ_SEL = 15;		12.3		dB
DisplayPort Transmitter (TX1p/n, TX2p/n, RX1p/n, RX2p/n)						
$V_{TX-CM-INST}$	Max Instantaneous TX DC common mode voltage change under all operating conditions (Disabled to 4DP, etc…)	Measured at non-TUSB1146 side of AC coupling capacitor with 50-Ω load.	-500		1000	mV
$V_{TX(DC-CM)}$	Common-mode voltage bias in the transmitter (DC)		0		1	V
AUXp or AUXn and SBU1 or SBU2						
R_{ON}	Output ON resistance	V_{CC} = 3.3 V; V_I = 0 to 0.4 V for AUXp; V_I = 2.7 V to 3.6 V for AUXn	2	5.5	10	Ω
ΔR_{ON}	ON resistance mismatch within pair	V_{CC} = 3.3 V; V_I = 0 to 0.4 V for AUXP; V_I = 2.7 V to 3.6 V for AUXN			2.5	Ω
$R_{ON(FLAT)}$	ON resistance flatness (RON max – RON min) measured at identical VCC and temperature	V_{CC} = 3.3 V; V_I = 0 to 0.4 V for AUXp; V_I = 2.7 V to 3.6 V for AUXn			2	Ω
$V_{(AUXP\_DC\_CM)}$	AUX Channel DC common mode voltage for AUXp and SBU1.	V_{CC} = 3.3 V;	0		0.4	V
$V_{(AUXN\_DC\_CM)}$	AUX Channel DC common mode voltage for AUXn and SBU2	V_{CC} = 3.3 V;	2.7		3.6	V
$C_{(AUX\_ON)}$	ON-state capacitance	V_{CC} = 3.3 V; CTL1 = 1; V_I = 0 V or 3.3 V		4	7	pF
$C_{(AUX\_OFF)}$	OFF-state capacitance	V_{CC} = 3.3 V; CTL1 = 0; V_I = 0 V or 3.3 V		3	6	pF

6.8 DCI Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DCI_CLK and DCI_DAT LVCMOS Outputs						
V_{OL}	Low-Level output voltage	V_{CC} = 3 V; I_{OL} = 2 mA; C_L = 10 pF			0.45	V
V_{OH}	High-Level output voltage	V_{CC} = 3 V; I_{OL} = –2 mA;	2.4			V
R_{DCI}	Output characteristic impedance		21	25	33	Ω
t_{PERIOD}	DCI Clock period	Measured at 50%	7.52			ns
t_{VALID}	Rising edge of DCI clock to DCI data valid				1	ns
t_{DCI_RISE}	DCI output rise time	Measured at 20% to 80%.	350			ps
t_{DCI_FALL}	DCI output fall time	Measured at 80% to 20%	350			ps

6.9 Timing Requirements

			MIN	NOM	MAX	UNIT
USB3.1						
$t_{IDLEEntry}$	Delay from U0 to electrical idle	Refer to Figure 20.		10		ns
$t_{IDELExit\_U1}$	U1 exist time: break in electrical idle to the transmission of LFPS	Refer to Figure 20.		6		ns
$t_{IDLEExit\_U2U3}$	U2/U3 exit time: break in electrical idle to transmission of LFPS	Refer to Figure 20.		10		µs
t_{RXDET_INTVL}	RX detect interval while in Disconnect				12	ms
$t_{IDLEExit\_DISC}$	Disconnect Exit Time			10		µs
t_{Exit_SHTDN}	Shutdown Exit Time			1		ms
$t_{AEQ\_FULL\_DONE}$	Maximum time to obtain optimum EQ setting when operating in Full AEQ mode.				300	µs
$t_{AEQ\_FAST\_DONE}$	Maximum time to determine appropriate EQ setting when operating in Fast AEQ mode.				60	µs
t_{DIFF_DLY}	Differential Propagation Delay	Refer to Figure 19.			300	ps
t_R, t_F	Output Rise/Fall time	20%-80% of differential voltage measured 1.7 inch from the output pin; Refer to Figure 21.		40		ps
t_{RF_MM}	Output Rise/Fall time mismatch	20%-80% of differential voltage measured 1.7 inch from the output pin			2.6	ps
Power-up						
t_{D_PG}	$V_{CC(min)}$ to internal Power Good asserted high	Refer to Figure 27			25	ms
t_{CFG_SU}	CFG(1) pins setup(2)	Refer to Figure 27	250			µs
t_{CFG_HD}	CFG(1) pins hold	Refer to Figure 27	10			µs
t_{CTL_DB}	CTL[1:0] and FLIP pin debounce	Refer to Figure 27			16	ms

(1) Following pins comprise CFG pins: I2C_EN, EQ[1:0], SSEQ[1:0], and DPEQ[1:0].
(2) Recommend CFG pins are stable when V_{CC} is at min.

6.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUXp or AUXn and SBU1 or SBU2						
t_{AUX_PD}	Switch propagation delay				400	ps
$t_{AUX\_SW\_OFF}$	Switching time CTL1 to switch OFF. Not including TCTL1_DEBOUNCE.	Refer to Figure 23.			500	ns
$t_{AUX\_SW\_ON}$	Switching time CTL1 to switch ON	Refer to Figure 22.			500	ns
t_{AUX_INTRA}	Intra-pair output skew				100	ps
USB3.1 and DisplayPort Mode Transition Requirement GPIO Mode						
$t_{GP\_USB\_4DP}$	Min overlap of CTL0 and CTL1 when transitioning from USB 3.1 only mode to 4-Lane DisplayPort mode or vice versa.	I2C_EN = 0; Refer to Figure 18.	4			µs

Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CTL1 and HPDIN						
$t_{CTL1\_DEBOUNCE}$	CTL1 and HPDIN debounce time when transitioning from H to L.		2		10	ms
I^2C						
f_{SCL}	I^2C clock frequency				1	MHz
t_{BUF}	Bus free time between START and STOP conditions	Refer to Figure 17	0.5			µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated	Refer to Figure 17	0.26			µs
t_{LOW}	Low period of the I^2C clock	Refer to Figure 17	0.5			µs
t_{HIGH}	High period of the I^2C clock	Refer to Figure 17	0.26			µs
t_{SUSTA}	Setup time for a repeated START condition	Refer to Figure 17	0.26			µs
t_{HDDAT}	Data hold time	Refer to Figure 17	0			µs
t_{SUDAT}	Data setup time	Refer to Figure 17	50			ns
t_R	Rise time of both SDA and SCL signals	Refer to Figure 17			120	ns
t_F	Fall time of both SDA and SCL signals	Refer to Figure 17	20 × ($V_{(I2C)}$/5.5 V)		120	ns
t_{SUSTO}	Setup time for STOP condition	Refer to Figure 17	0.26			µs
C_b	Capacitive load for each bus line				150	pF

6.11 Typical Characteristics

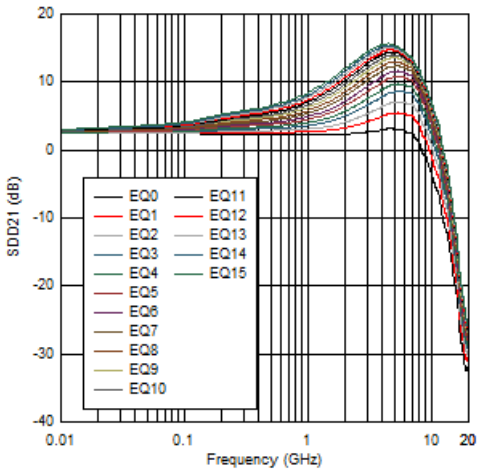


Figure 1. DisplayPort EQ Settings Curves

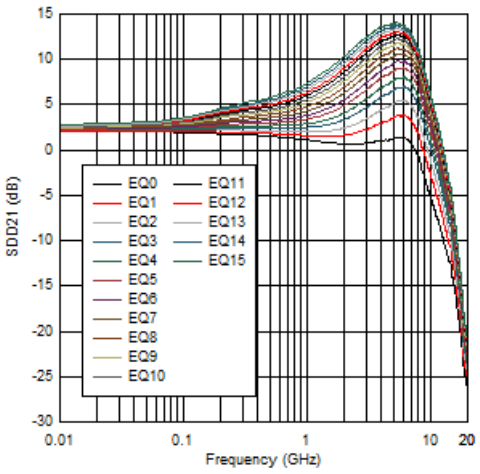


Figure 2. USB RX1 EQ Settings Curves

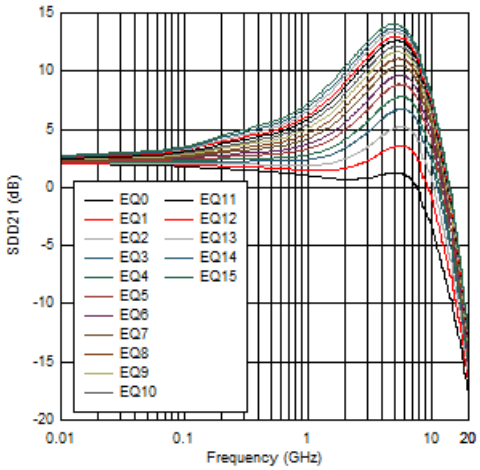


Figure 3. USB SSTX EQ Settings Curves

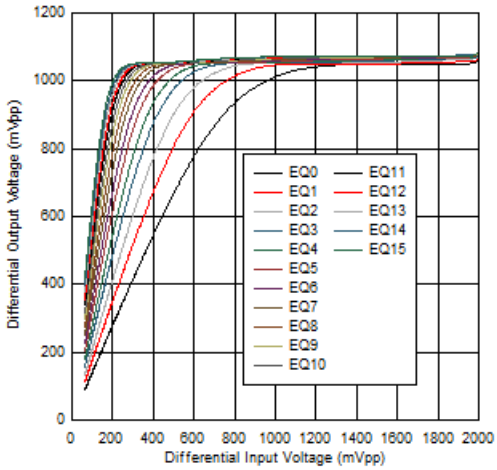


Figure 4. DisplayPort Linearity Curves at 4.05 GHz

Typical Characteristics (continued)

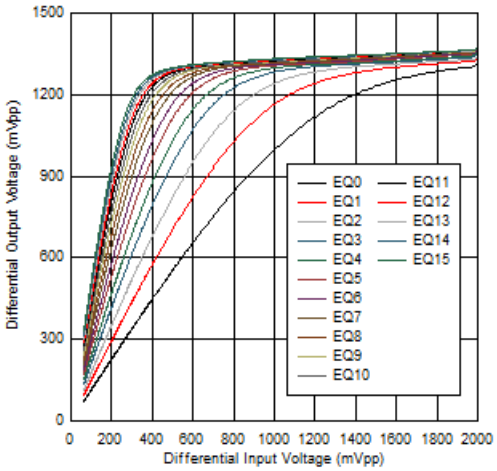


Figure 5. USB TX Linearity Curves at 5 GHz

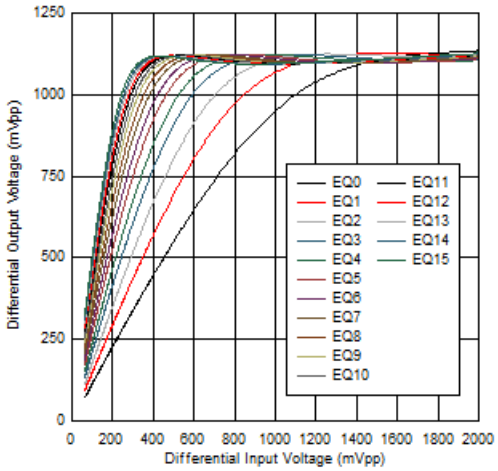


Figure 6. USB RX Linearity Curves at 5 GHz

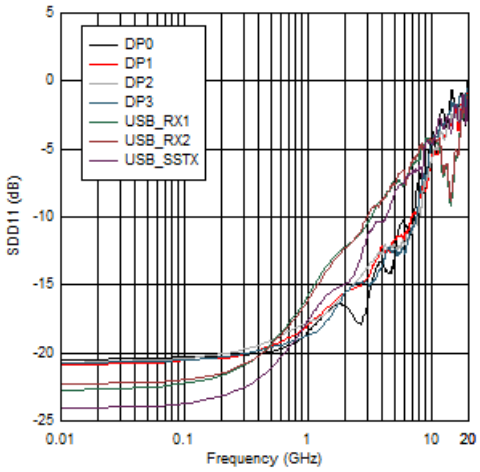


Figure 7. Input Return Loss Performance

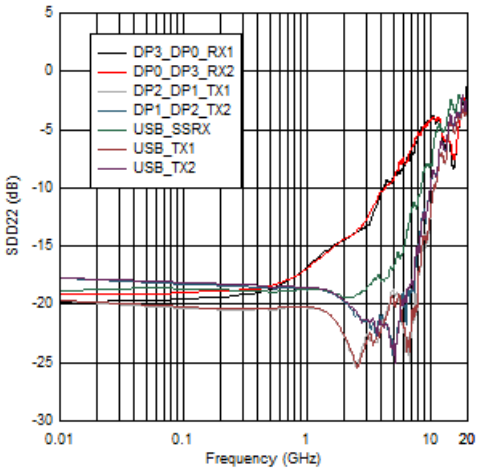


Figure 8. Output Return Loss Performance

Typical Characteristics (continued)

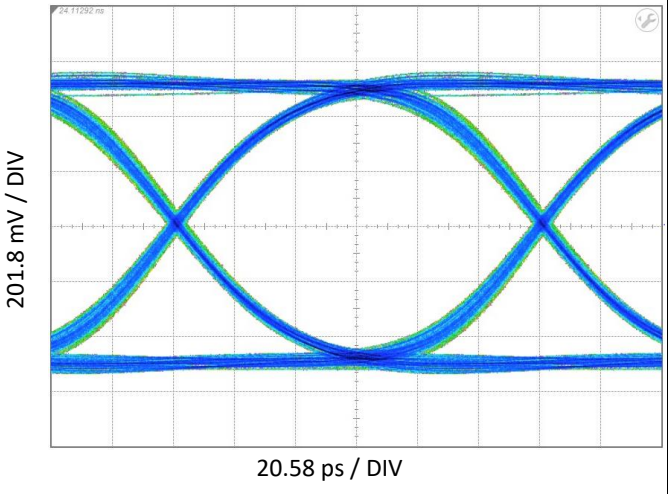


Figure 9. DisplayPort HBR3 Eye-Pattern Performance with 12-inch Input PCB Trace at 8.1 Gbps

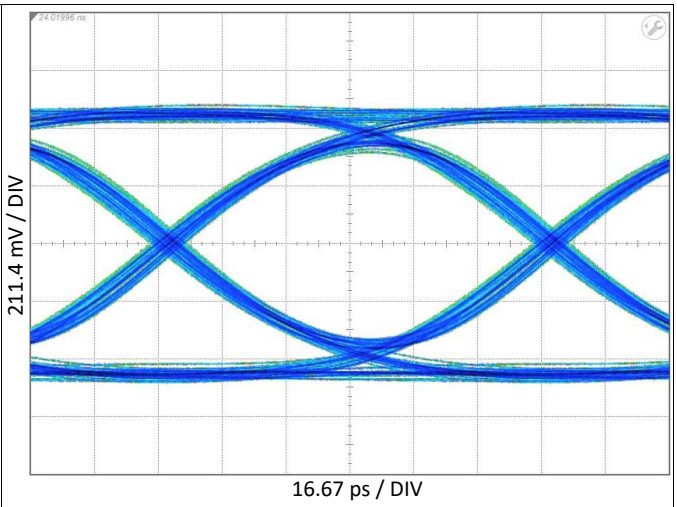


Figure 10. USB 3.1 Gen2 Eye-Pattern Performance with 12-inch Input PCB Trace at 10 Gbps

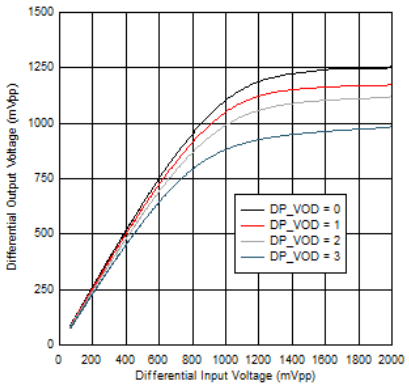


Figure 11. DP VOD Linearity settings at 100MHz

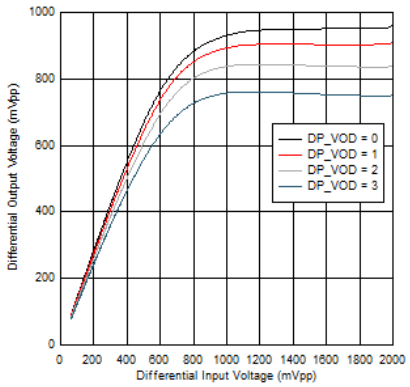


Figure 12. DP VOD Linearity Settings at 5GHz

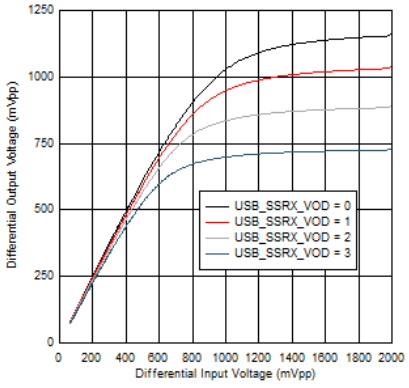


Figure 13. USB SSRX VOD Linearity Settings at 100MHz

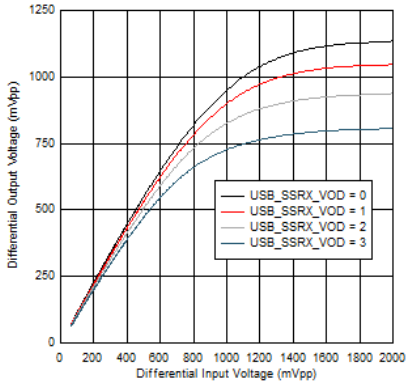


Figure 14. USB SSRX VOD Linearity Settings at 5GHz

Typical Characteristics (continued)

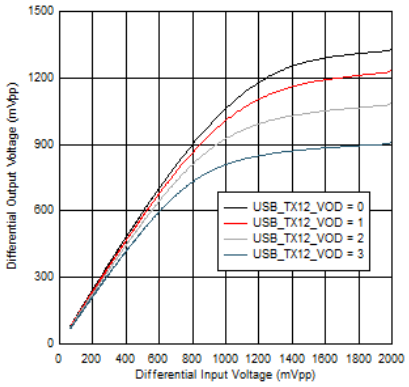


Figure 15. USB TX1 VOD Linearity Settings at 100MHz

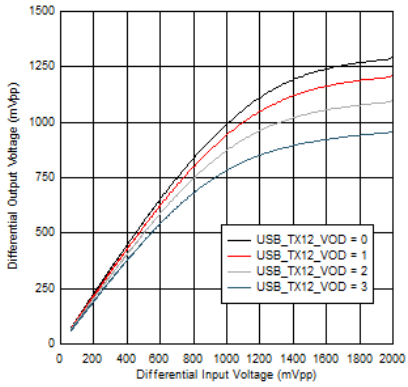


Figure 16. USB TX1 VOD Linearity Settings at 5GHz

7 Parameter Measurement Information

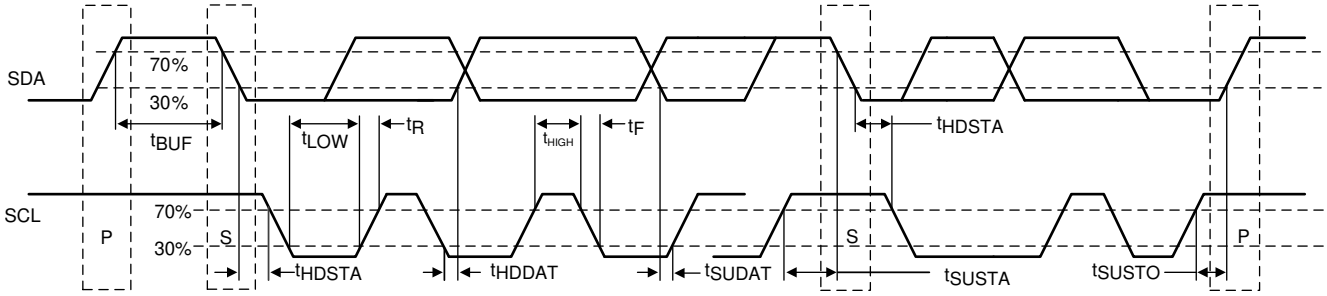


Figure 17. I²C Timing Diagram Definitions

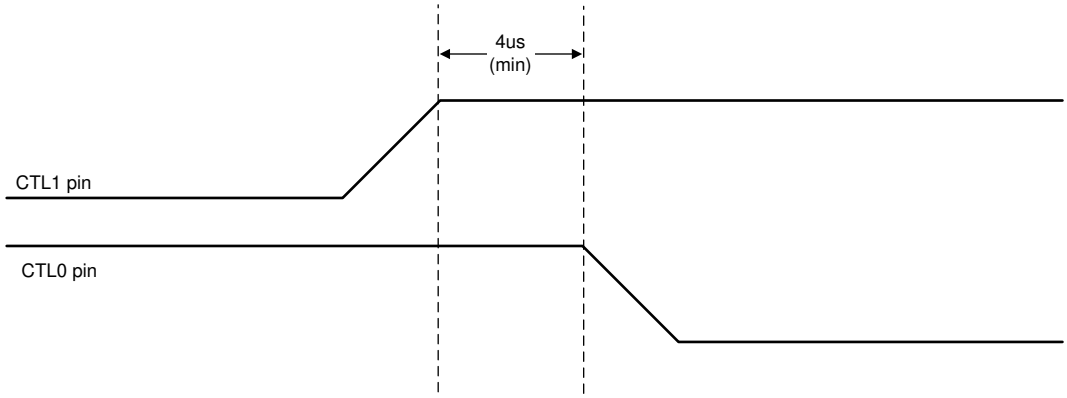


Figure 18. USB3.1 to 4-Lane DisplayPort in GPIO Mode

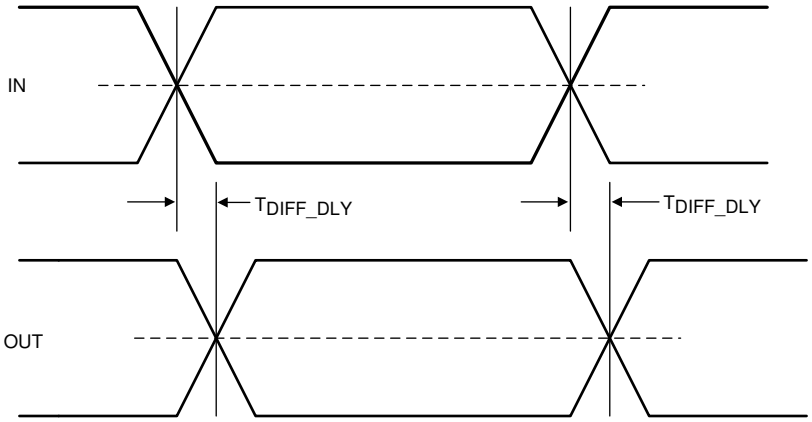


Figure 19. Propagation Delay

Parameter Measurement Information (continued)

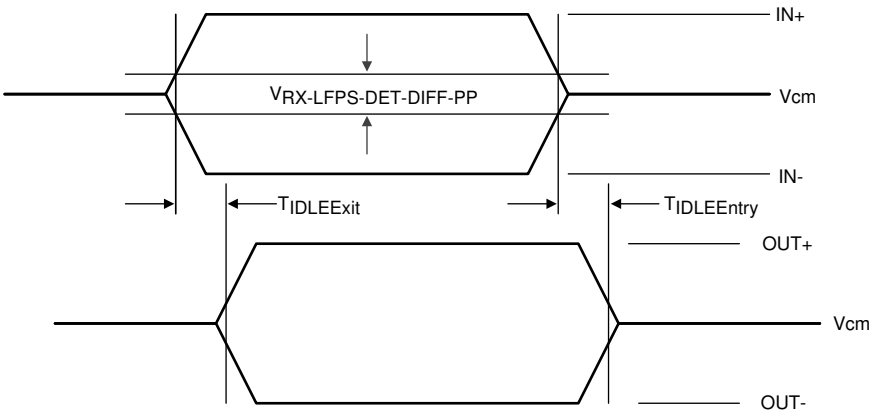


Figure 20. Electrical Idle Mode Exit and Entry Delay

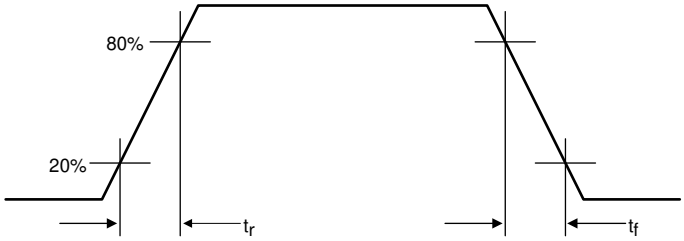


Figure 21. Output Rise and Fall Times

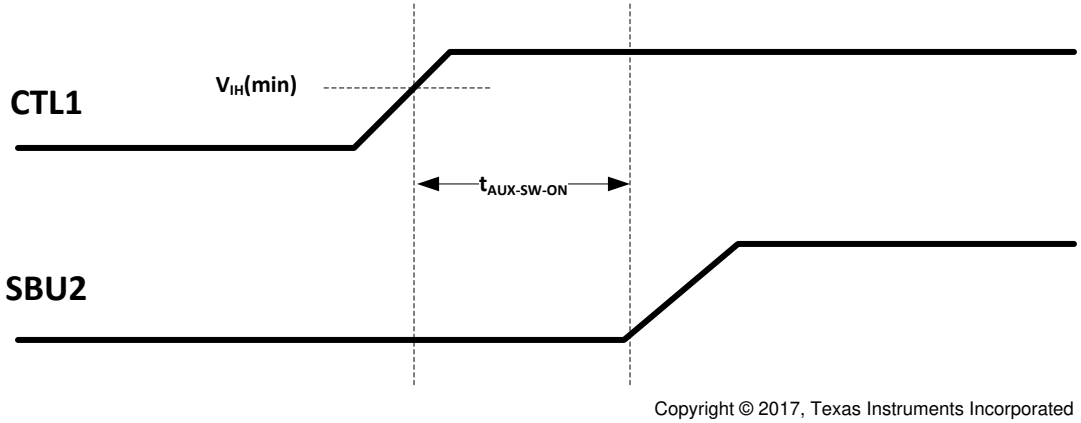


Figure 22. AUX to SBU Switch ON Timing Diagram

Parameter Measurement Information (continued)

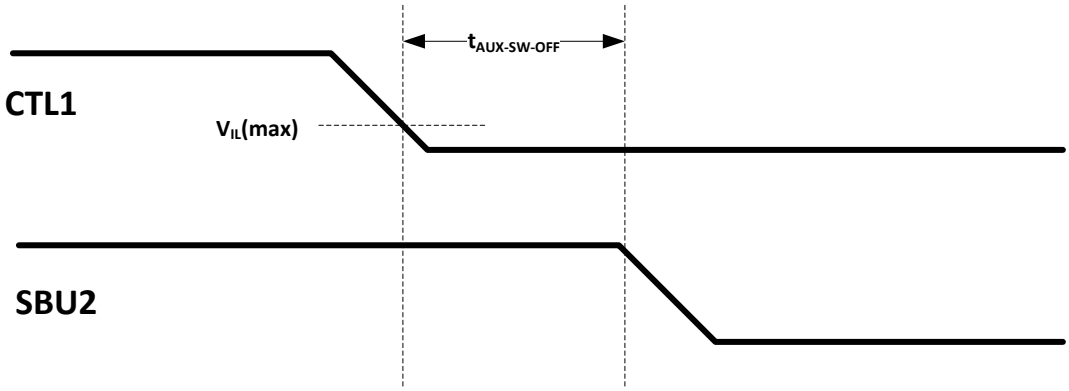


Figure 23. AUX to SBU Switch OFF Timing Diagram

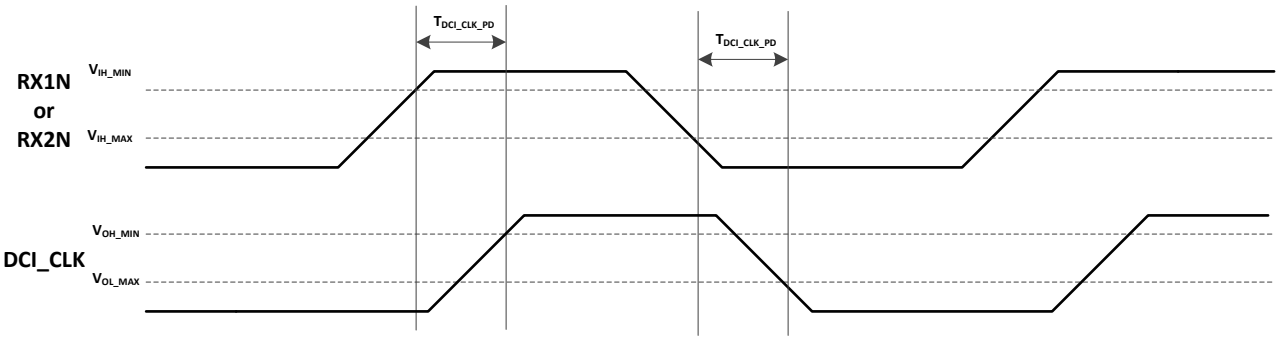


Figure 24. DCI Clock Propagation Delay

TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 0;
TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 1; TX_DEEMPHASIS = 0;
TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 1; TX_DEEMPHASIS = 1;
TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 1; TX_DEEMPHASIS = 2;
TX_PRESHOOT_EN = 0; TX_DEEMPHASIS_EN = 1; TX_DEEMPHASIS = 3;

Figure 25. SSRX Limited De-emphasis Only

Parameter Measurement Information (continued)

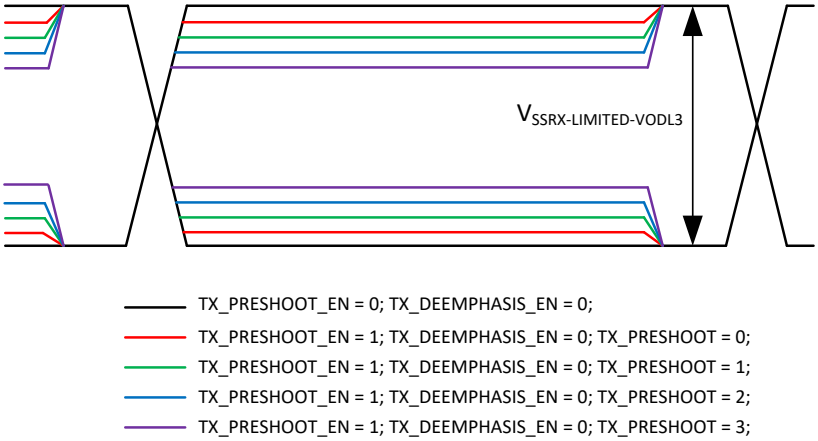


Figure 26. SSRX Limited Pre-Shoot Only

Parameter Measurement Information (continued)

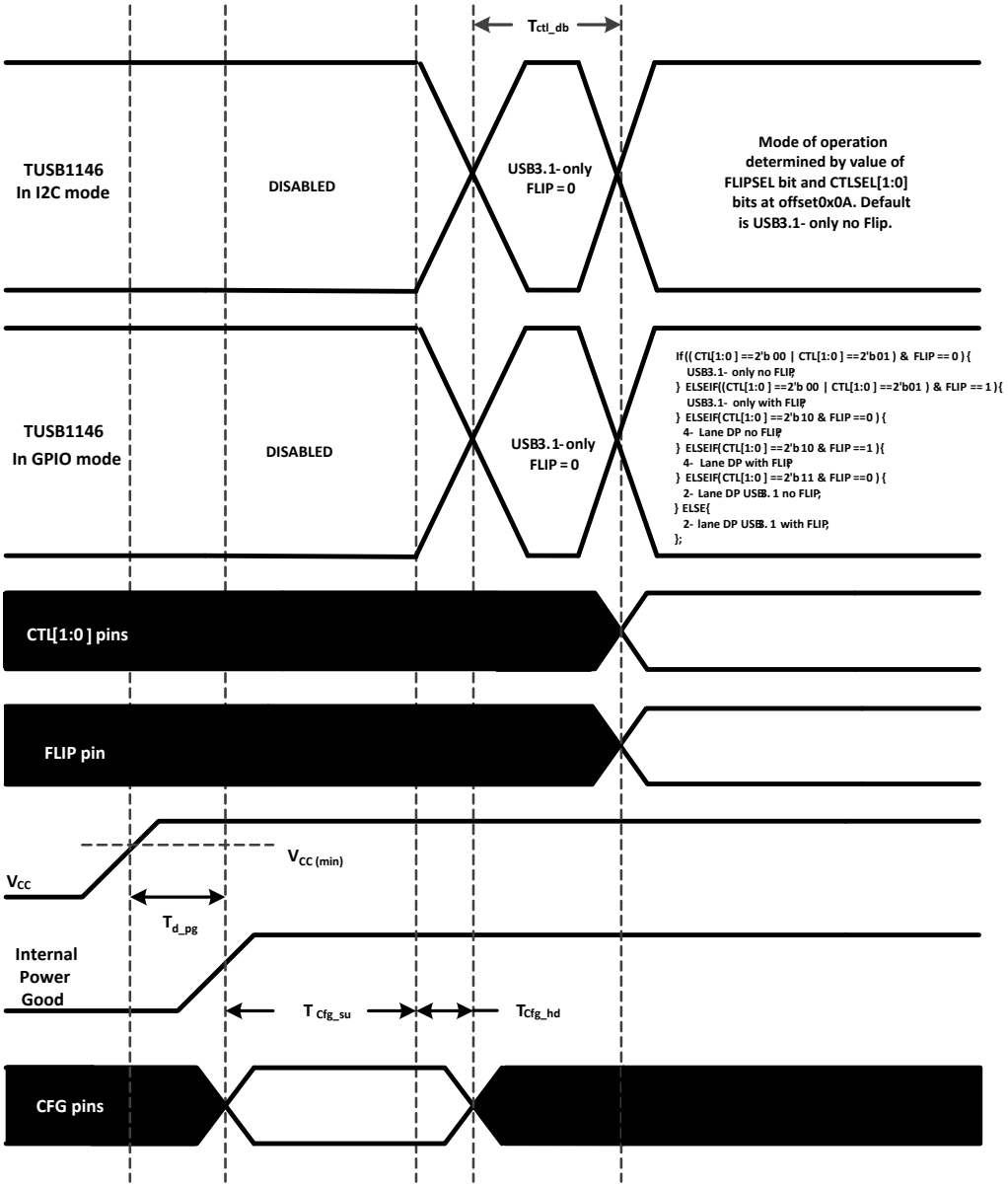


Figure 27. Power-On Timing

8 Detailed Description

8.1 Overview

The TUSB1146 is a VESA USB Type-C Alt Mode redriving switch supporting data rates up to 10 Gbps for downstream facing port. The device utilize 5th generation USB redriver technology as well as new innovative adaptive equalization feature on its DFP receivers. The device is utilized for DFP configurations C, D, and E from the VESA DisplayPort Alt Mode on USB Type-C.

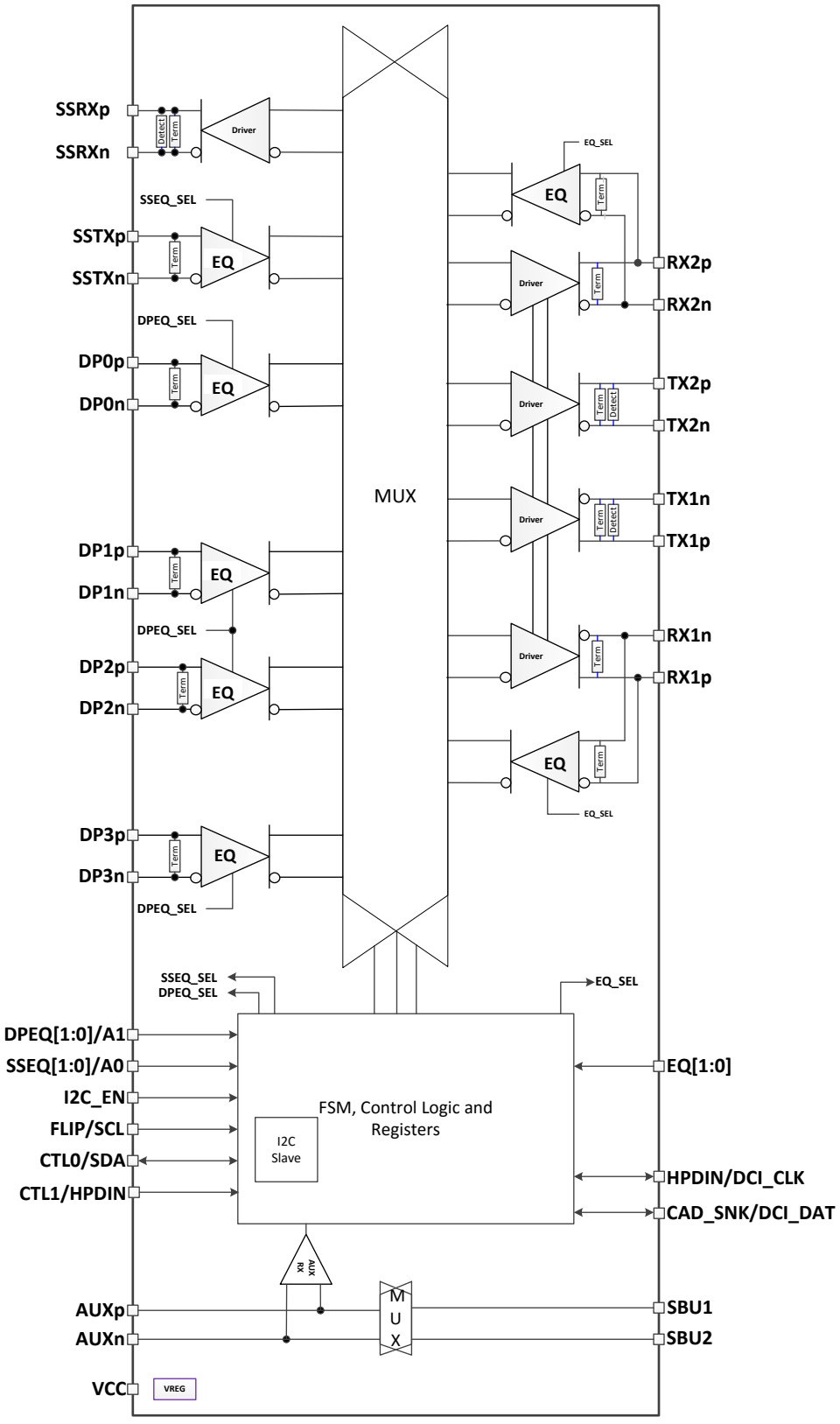
The TUSB1146 provides several levels of receive equalization to compensate for cable and board trace loss due to inter-symbol interference (ISI) when USB 3.1 Gen1/Gen2 or DisplayPort 2.0 signals travel across a PCB or cable. This device requires a 3.3-V power supply. It comes in a commercial temperature range and industrial temperature range.

For a host application the TUSB1146 enables the system to pass both transmitter compliance and receiver jitter tolerance tests for USB 3.1 Gen1/Gen2 and DisplayPort version 2.0 (up to UHBR10). The re-driver recovers incoming data by applying equalization that compensates for channel loss, and drives out signals with a high differential voltage. Each channel has a receiver equalizer with selectable gain settings. The equalization should be set based on the amount of insertion loss before the TUSB1146 receivers. Independent equalization control for each channel can be set using EQ[1:0], SSEQ[1:0], and DPEQ[1:0] pins.

The TUSB1146 advanced state machine makes it transparent to hosts and devices. After power up, the TUSB1146. periodically performs receiver detection on the TX pairs. If it detects a USB 3.1 Gen1/Gen2 receiver, the RX termination is enabled, and the TUSB1146 is ready to re-drive.

The device ultra-low-power architecture operates at a 3.3-V power supply and achieves enhanced performance. The automatic LFPS de-emphasis control further enables the system to be USB3.1 compliant.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 USB 3.1

The TUSB1146 supports USB 3.1 Gen1/Gen2 datarates up to 10 Gbps. The TUSB1146 supports all the USB defined power states (U0, U1, U2, and U3). Because the TUSB1146 is a linear redriver, it can't decode USB3.1 physical layer traffic. The TUSB1146 monitors the actual physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the USB power state of the USB 3.1 interface.

The TUSB1146 features an intelligent low frequency periodic signaling (LFPS) detector. The LFPS detector automatically senses the low frequency signals and disables receiver equalization functionality. When not receiving LFPS, the TUSB1146 will enable receiver equalization based on the EQ[1:0] and SSEQ[1:0] pins or values programmed into EQ1_SEL, EQ2_SEL, and SSEQ_SEL registers.

8.3.2 DisplayPort

The TUSB1146 supports up to 4 DisplayPort lanes at datarates up to 10 Gbps (UHBR10). The TUSB1146, when configured in DisplayPort mode, monitors the native AUX traffic as it traverses between DisplayPort source and DisplayPort sink. For the purposes of reducing power, the TUSB1146 manages the number of active DisplayPort lanes based on the content of the AUX transactions. The TUSB1146 snoops native AUX writes to DisplayPort sink's DPCD registers 0x00101 (LANE_COUNT_SET) and 0x00600 (SET_POWER_STATE). TUSB1146 disables/enables lanes based on value written to LANE_COUNT_SET. The TUSB1146 disables all lanes when SET_POWER_STATE is in the D3. Otherwise active lanes will be based on value of LANE_COUNT_SET.

DisplayPort AUX snooping is enabled by default but can be disabled by changing the AUX_SNOOP_DISABLE register. Once AUX snoop is disabled, management of TUSB1146 DisplayPort lanes are controlled through various configuration registers. When TUSB1146 is enabled for GPIO mode (I2C_EN = "0"), the CAD_SNK pin can be used to disable AUX snooping. When CAD_SNK pin is high, the AUX snooping functionality is disabled and all four DisplayPort lanes will be active.

8.3.3 4-level Inputs

The TUSB1146 has (I2C_EN, EQ[1:0], DPEQ[1:0], and SSEQ[1:0]) 4-level inputs pins that are used to control the equalization gain and place TUSB1146 into different modes of operation. These 4-level inputs utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings. There is an internal pull-up and pull-down resistors. These resistors, together with the external resistor connection combine to achieve the desired voltage level.

Table 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 KΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 KΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 KΩ 5%to V_{CC}. Option 2: Tie directly to V_{CC}.

NOTE

All four-level inputs are latched after rising edge of the internal reset. After t_{cfg_hd}, the internal pull-up and pull-down resistors will be isolated in order to save power.

8.3.4 Receiver Linear Equalization

The purpose of receiver equalization is to compensate for channel insertion loss and inter-symbol interference in the system before the input of the TUSB1146. The receiver overcomes these losses by attenuating the low frequency components of the signals with respect to the high frequency components. The proper gain setting should be selected to match the channel insertion loss before the input of the TUSB1146 receivers. Two 4-level inputs pins enable up to 16 possible equalization settings. USB3.1 upstream path, USB3.1 downstream path, and DisplayPort each have their own two 4-level inputs. The TUSB1146 also provides the flexibility of adjusting settings through I^2C registers.

The TUSB1146 implements three different equalizer features for the USB-C downstream facing port receivers (RX1 and RX2): Fixed EQ, Fast Adaptive EQ (Fast AEQ), and Full Adaptive EQ (Full AEQ). The default operation is Fixed EQ. In Fixed EQ operation, a single setting is used for all possible devices (with and without cable) inserted into the USB-C receptacle. The Fast AEQ feature will distinguish between a short channel and a long channel. A short channel represents a low loss use case of a USB 3.1 device plugged directly into USB-C receptacle without a cable. A long channel represents the high loss use case of the USB 3.1 device plugged into the receptacle through a USB cable. In Fast AEQ mode, TUSB1146 will select between two pre-determined settings based on whether or not channel is short or long. When TUSB1146 is configured for Full AEQ, the TUSB1146 will automatically determine the best equalization setting each time a USB device is inserted into the USB-C receptacle. In Full AEQ mode, the TUSB1146 will always determine the best settings regardless if the channel is short, long or somewhere in between. The Full AEQ feature is disabled by default but can be enabled through a register.

8.4 Device Functional Modes

8.4.1 Device Configuration in GPIO Mode

The TUSB1146 is in GPIO configuration when I2C_EN = “0” or when I2C_EN = "F" and !(EQ0 = "0" and EQ1 = "0"). The TUSB1146 supports the following configurations: USB 3.1 only, 2 DisplayPort lanes + USB 3.1, or 4 DisplayPort lanes (no USB 3.1). The CTL1 pin controls whether DisplayPort is enabled. The combination of CTL1 and CTL0 selects between USB 3.1 only, 2 lanes of DisplayPort, or 4-lanes of DisplayPort as detailed in Table 2. The AUXp or AUXn to SBU1 or SBU2 mapping is controlled based on Table 3.

After power-up (V_{CC} from 0 V to 3.3 V), the TUSB1146 defaults to USB3.1 mode. The USB PD controller upon detecting no device attached to Type-C port or USB3.1 operation not required by attached device must take TUSB1146 out of USB3.1 mode by transitioning the CTL0 pin from L to H and back to L.

Table 2. GPIO Configuration Control

CTL1 PIN	CTL0 PIN	FLIP PIN	TUSB1146 CONFIGURATION	VESA DisplayPort ALT MODE DFP_D CONFIGURATION
L	L	L	Power Down	—
L	L	H	Power Down	—
L	H	L	One Port USB 3.1 - No Flip	—
L	H	H	One Port USB 3.1 – With Flip	—
H	L	L	4 Lane DP - No Flip	C and E
H	L	H	4 Lane DP – With Flip	C and E
H	H	L	One Port USB 3.1 + 2 Lane DP- No Flip	D
H	H	H	One Port USB 3.1 + 2 Lane DP– With Flip	D

Table 3. GPIO AUXp or AUXn to SBU1 or SBU2 Mapping

CTL1 PIN	FLIP PIN	MAPPING
H	L	AUXp → SBU1 AUXn → SBU2
H	H	AUXp → SBU2 AUXn → SBU1
L > 2 ms	X	Open

Table 4 Details the TUSB1146’s mux routing. This table is valid for both I^2C and GPIO configuration modes.

Table 4. INPUT to OUTPUT Mapping

CTL1 PIN	CTL0 PIN	FLIP PIN	FROM	TO
			INPUT PIN	OUTPUT PIN
L	L	L	NA	NA
L	L	H	NA	NA
L	H	L	RX1P	SSRXP
			RX1N	SSRXN
			SSTXP	TX1P
			SSTXN	TX1N
L	H	H	RX2P	SSRXP
			RX2N	SSRXN
			SSTXP	TX2P
			SSTXN	TX2P
H	L	L	DP0P	RX2P
			DP0N	RX2N
			DP1P	TX2P
			DP1N	TX2N
			DP2P	TX1P
			DP2N	TX1N
			DP3P	RX1P
			DP3N	RX1N
H	L	H	DP0P	RX1P
			DP0N	RX1N
			DP1P	TX1P
			DP1N	TX1N
			DP2P	TX2P
			DP2N	TX2N
			DP3P	RX2P
			DP3N	RX2N
H	H	L	RX1P	SSRXP
			RX1N	SSRXN
			SSTXP	TX1P
			SSTXN	TX1N
			DP0P	RX2P
			DP0N	RX2N
			DP1P	TX2P
			DP1N	TX2N
H	H	H	RX2P	SSRXP
			RX2N	SSRXN
			SSTXP	TX2P
			SSTXN	TX2N
			DP0P	RX1P
			DP0N	RX1N
			DP1P	TX1P
			DP1N	TX1N

8.4.2 Device Configuration In I²C Mode

The TUSB1146 is in I²C mode when I2C_EN is not equal to “0” or when I2C_EN = "F" and EQ0 = "0" and EQ1 = "0". The same configurations defined in GPIO mode are also available in I²C mode. The TUSB1146 USB3.1 and DisplayPort configuration is controlled based on Table 5. The AUXp or AUXn to SBU1 or SBU2 mapping control is based on Table 6.

Table 5. I²C Configuration Control

REGISTERS			TUSB1146 CONFIGURATION	VESA DisplayPort ALT MODE DFP_D CONFIGURATION
CTLSEL1	CTLSEL0	FLIPSEL		
0	0	0	Power Down	—
0	0	1	Power Down	—
0	1	0	One Port USB 3.1 - No Flip	—
0	1	1	One Port USB 3.1 – With Flip	—
1	0	0	4 Lane DP - No Flip	C and E
1	0	1	4 Lane DP – With Flip	C and E
1	1	0	One Port USB 3.1 + 2 Lane DP- No Flip	D
1	1	1	One Port USB 3.1 + 2 Lane DP– With Flip	D

Table 6. I²C AUXp or AUXn to SBU1 or SBU2 Mapping

REGISTERS				MAPPING
AUX_SBU_OVR1	AUX_SBU_OVR0	CTLSEL1	FLIPSEL	
0	0	1	0	AUXp → SBU1 AUXn → SBU2
0	0	1	1	AUXp → SBU2 AUXn → SBU1
0	0	0	X	Open
0	1	X	X	AUXp → SBU1 AUXn → SBU2
1	0	X	X	AUXp → SBU2 AUXn → SBU1
1	1	X	X	Open

8.4.3 DisplayPort Mode

The TUSB1146 supports up to four DisplayPort lanes at datarates up to 10 Gbps (UHBR10). TUSB1146 can be enabled for DisplayPort through GPIO control or through I²C register control. When I2C_EN is ‘0’, DisplayPort is controlled based on Table 2. When not in GPIO mode, enable of DisplayPort functionality is controlled through I²C registers.

8.4.4 Linear EQ Configuration

Each of the TUSB1146 receiver lanes has individual controls for receiver equalization. The receiver equalization gain value can be controlled either through I^2C registers or through GPIOs. details the gain value for each available combination when TUSB1146 is in GPIO mode. These same options are also available in I^2C mode by updating registers DP0EQ_SEL, DP1EQ_SEL, DP2EQ_SEL, DP3EQ_SEL, EQ1_SEL, EQ2_SEL, and SSEQ_SEL.

Table 7. USB Downstream Facing Port Receiver (RX1 and RX2 pins) Equalization Control

Register(s): EQ1_SEL or EQ2_SEL Equalization Setting #	EQ1 PIN Level	EQ0 PIN Level	EQ Gain at 5 GHz minus Gain at 100MHz (dB)
0	0	0	-0.7
1	0	R	1.1
2	0	F	2.7
3	0	1	4.5
4	R	0	5.5
5	R	R	6
6	R	F	7.5
7	R	1	8.0
8	F	0	8.5
9	F	R	9.0
10	F	F	9.3
11	F	1	9.8
12	1	0	10.0
13	1	R	10.3
14	1	F	10.7
15	1	1	11

Table 8. USB Upstream Facing Port Receiver (SSTX pins) Equalization Control

Register(s): SSEQ_SEL Equalization Setting #	SSEQ1 PIN LEVEL	SSEQ0 PIN LEVEL	EQ Gain at 5 GHz minus Gain at 100MHz (dB)
0	0	0	-0.5
1	0	R	1.5
2	0	F	3.1
3	0	1	4.5
4	R	0	5.5
5	R	R	6.5
6	R	F	7.5
7	R	1	8.7
8	F	0	9.0
9	F	R	9.4
10	F	F	9.8
11	F	1	10.2
12	1	0	10.5
13	1	R	10.7
14	1	F	11.0
15	1	1	11.5

Table 9. DisplayPort Receiver (DP[3:0] pins) Equalization Control

Register(s): DP0EQ_SEL, DP1EQ_SEL, DP2EQ_SEL, or DP3EQ_SEL Equalization Setting #	DPEQ1 PIN LEVEL	DPEQ0 PIN LEVEL	EQ Gain at 4.05 GHz minus Gain at 100MHz (dB)
0	0	0	0.8
1	0	R	1.3
2	0	F	2.8
3	0	1	4.1
4	R	0	5.8
5	R	R	6.2
6	R	F	7.1
7	R	1	7.9
8	F	0	8.6
9	F	R	9.2
10	F	F	9.8
11	F	1	10.3
12	1	0	10.7
13	1	R	11.2
14	1	F	11.5
15	1	1	12

8.4.5 VOD modes

The TUSB1146 provides two modes for VOD (voltage output differential) control: Linearity VOD and Limited VOD. The TUSB1146 defaults linearity VOD mode but can be changed to limited VOD mode thru I2C register.

8.4.5.1 Linearity VOD

Linearity VOD defines the linearity range of the TUSB1146. When TUSB1146 is in linear VOD mode, the output VOD is a linear function of the input VID. For example, if the signal at TUSB1146's input (VID) is at 600mVpp then the TUSB1146's output VOD will be around 600mVpp. The linear VOD mode is the only mode available for the downstream paths (DisplayPort and USB). The upstream path (USB only) supports both linear and limited VOD. Linearity VOD mode is the default operation of the TUSB1146. The TUSB1146 provides four different linearity VOD settings. All four settings are available in I^2C mode thru register control.

8.4.5.2 Limited VOD

Limited VOD mode is used to set the actual VOD level and is used when TUSB1146 is configured in limited redriver mode. In this mode the VOD is no longer a linear function of the input VID. For example, if the signal at TUSB1146's input (VID) is at 600mVpp then the TUSB1146's output VOD will be around 1000mVpp (assuming LINR_L3 is selected). The limited redriver mode is only supported in the upstream direction (RX1 -> SSRX and RX2 -> SSRX). The downstream paths will always operate in linear redriver mode. Limited redriver mode can be enabled by I^2C register. This mode is not supported in GPIO mode. The TUSB1146 provides four different limited VOD settings. All four settings are available through register control.

8.4.6 Transmit Equalization

The TUSB1146 in limited redriver mode offers both SSRX transmitter pre-shoot and de-emphasis controls. The TUSB1146 offers four pre-shoot levels and four de-emphasis levels. These levels can be changed by modifying I2C registers. Pre-shoot is enabled when SSRX_LIMIT_ENABLE bit = 1 and TX_PRESHOOT_EN bit= 1. De-emphasis is enabled when SSRX_LIMIT_ENABLE bit = 1 and TX_DEEPHASIS_EN = 1.

8.4.7 USB3.1 Modes

The TUSB1146 monitors the physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the state of the USB3.1 interface. Depending on the state of the USB 3.1 interface, the TUSB1146 can be in one of four primary modes of operation when USB 3.1 is enabled (CTL0 = H or CTLSEL0 = 1b1): Disconnect, U2/U3, U1, and U0.

The Disconnect mode is the state in which TUSB1146 has not detected far-end termination on both upstream facing port (UFP) or downstream facing port (DFP). The disconnect mode is the lowest power mode of each of the four modes. The TUSB1146 remains in this mode until far-end receiver termination has been detected on both UFP and DFP. The TUSB1146 immediately exits this mode and enter U0 once far-end termination is detected.

Once in U0 mode, the TUSB1146 will redrive all traffic received on UFP and DFP. U0 is the highest power mode of all USB3.1 modes. The TUSB1146 remains in U0 mode until electrical idle occurs on both UFP and DFP. Upon detecting electrical idle, the TUSB1146 immediately transitions to U1.

The U1 mode is the intermediate mode between U0 mode and U2/U3 mode. In U1 mode, the TUSB1146 UFP and DFP receiver termination remains enabled. The UFP and DFP transmitter DC common mode is maintained. The power consumption in U1 is similar to power consumption of U0.

Next to the disconnect mode, the U2/U3 mode is next lowest power state. While in this mode, the TUSB1146 periodically performs far-end receiver detection. Anytime the far-end receiver termination is not detected on either UFP or DFP, the TUSB1146 leaves the U2/U3 mode and transitions to the Disconnect mode. It also monitors for a valid LFPS. Upon detection of a valid LFPS, the TUSB1146 immediately transitions to the U0 mode. In U2/U3 mode, the TUSB1146 receiver terminations remain enabled but the TX DC common mode voltage is not maintained.

8.4.8 Downstream Facing Port Adaptive Equalization

The TUSB1146 implements an adaptive equalizer (AEQ) function for the USB-C downstream facing port receivers (RX1 and RX2). The purpose of the adaptive equalizer function is determine the best EQ value such that output jitter is minimized. The TUSB1146 provides two modes of adaptive equalization: Fast AEQ and Full AEQ. The selection between Fast and Full AEQ is determined by a register. The AEQ feature is disabled by default but can enabled through a register. The Fast adaptive equalization feature is supported in GPIO mode when I2C_EN pin = "F" and !(EQ0 pin = "0" and EQ1 = "0").

NOTE

The AEQ feature is NOT supported on SSTX receiver and the DP[3:0] receivers. These receivers only support fixed EQ.

Fast AEQ is not supported in the GPIO defined by I2C_EN = "0". It is recommended to configure TUSB1146 for I2C mode when using adaptive EQ features as this provides the most flexibility.

8.4.8.1 Fast Adaptive Equalization in I2C Mode

The Fast AEQ mode is used to distinguish two channels (short channel and a long channel) and choose the appropriate receiver equalization setting for that channel. Because Fast AEQ only distinguishes between two choices, the AEQ time is a lot shorter than Full AEQ mode which minimizes impact to USB link training.

When Fast AEQ is enabled and channel is determined to be short, the TUSB1146 will use the value programmed into the EQx_SEL, where x = 1 or 2. If the TUSB1146 determines channel is not short, the TUSB1146 will switch to EQ value programmed into LONG_EQx register, where x = 1 or 2. During initial system evaluation, it is recommended to perform both short and long channel USB3.1 RX JTOL Gen2 testing and program EQx_SEL and LONG_EQx to the value which produced the best results for each channel configuration.

The TUSB1146 will determine short and long based on the estimate eye height. The value programmed into FASTAEQ_LIMITS register will determine the eye height limits. Software can change the defaults of this register to lower or raise the limits.

NOTE

EQ_OVERRIDE field must be set for values programmed into EQx_SEL and LONG_EQx to be used.

It is recommended to change the FASTAEQ_LIMITS register from the default value to 0x2 (80mV).

8.4.8.2 Full Adaptive Equalization

The Full AEQ mode attempts to find the best equalization value for RX1 and RX2 receivers by starting at the lowest EQ value and sweeping through all EQ combinations up to the value programmed into FULLAEQ_UPPER_EQ field. The default is to sweep through all sixteen EQ values (zero to fifteen). The number of EQ combinations can be reduced by programming FULLAEQ_UPPER_EQ register. The TUSB1146 also provides the ability to add or subtract some over/under equalization to compensate for channel in front of TUSB1146 by programming OVER_EQ_CTRL field to a non-zero value. If OVER_EQ_SIGN = 0, the TUSB1146 will add the value programmed into OVER_EQ_CTRL to the EQ value determined by the full adaptation. If OVER_EQ_SIGN = 1, the TUSB1146 will subtract the value programmed into OVER_EQ_CTRL from the EQ value determined by the full adaptation. For example, if full adaptation determines the best equalization value to be 4 and OVER_EQ_CTRL is 2 and OVER_EQ_SIGN = 0, the EQ setting used by TUSB1146 will be 6. The TUSB1146 hardware will always limit the sum of OVER_EQ_CTRL and the determined optimal EQ from full adaptation to be less than or equal to 15.

NOTE

Full AEQ is only supported in I2C mode.

8.5 Programming

8.5.1 Transition between Modes

The TUSB1146 allows for transitioning between any mode (USB-only to 4DP, 4DP to USB+2DP, and so forth). The USB-C standard requires transitioning to the USB Safe State before entering to or exiting from an Alternate Mode. The USB Safe State defines an electrical state for the SBU1/2 and SSTX/SSRX for DFPs, UFPs, and Active Cables when transitioning between USB and an Alternate Mode. Therefore before entering to or exiting from four lane DP mode it is recommended to first enter the Disable state (CTLSEL = 2'b00 or (CTL0 pin = 0 and CTL1 pin = 0)).

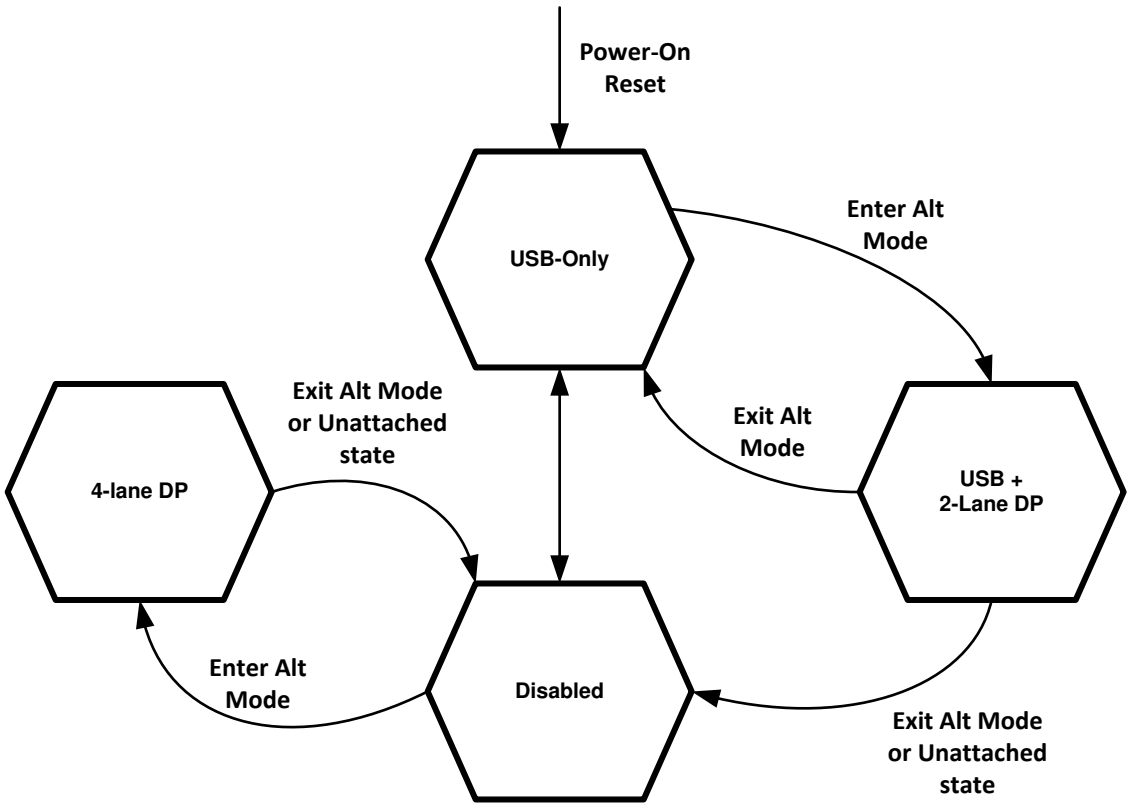


Figure 28. Recommended Mode Transitions

8.5.2 Pseudocode Examples

8.5.2.1 Fast AEQ with linear redriver mode

```
// (address, data)
// Initial power-on configuration.

                (0x0A, 0x11), // EQ_OVERRIDE and USB3.1 default.

                (0x1C, 0x81), // Fast AEQ enable

                (0x10, 0x55), // DP lanes 0 and 1 EQ

                (0x11, 0x55), // DP lanes 2 and 2 EQ

                (0x1D, 0x10), // FASTAEQ_LIMITS to 80mV

                (0x1E, 0x55), // USB-C Rx1/Rx2 Long channel EQ.

                (0x20, 0x00), // USB-C Rx1/Rx2 Short channel EQ.
```

Programming (continued)

```
                (0x21, 0x05), // SSTX receiver EQ.

// Controls when selecting between USB and DP modes.
If (USBonly_normal)

                { (0x0A,0x11); }
Else if (USBonly_flip)

                { (0x0A, 0x15); }
Else if (Dponly_normal)

                { (0x0A, 0x12); }
Else if (Dponly_flip)

                { (0x0A, 0x16); }
Else if (DPUSB_normal)

                { (0x0A, 0x13); }
Else if (DPUSB_flip)

                { (0x0A,0x17); }
Else // Nothing connected to Type-C

                { (0x0A, 0x10); }
```

8.5.2.2 Fast AEQ with limited redriver mode

```
// (address, data)
// Initial power-on configuration.

                (0x0A, 0x91), // EQ_OVERRIDE and USB3.1 default.

                (0x0B, 0x24), // Pre-shoot and De-emphasis control

                (0x1C, 0x81), // Fast AEQ enable

                (0x10, 0x55), // DP lanes 0 and 1 EQ

                (0x11, 0x55), // DP lanes 2 and 2 EQ

                (0x1D, 0x10), // FASTAEQ_LIMITS to 80mV

                (0x1E, 0x55), // USB-C Rx1/Rx2 Long channel EQ.

                (0x20, 0x00), // USB-C Rx1/Rx2 Short channel EQ.

                (0x21, 0x05), // SSTX receiver EQ.

                (0x32, 0x40), // VOD Control.

// Controls when selecting between USB and DP modes.
If (USBonly_normal)

                { (0x0A,0x91); }
Else if (USBonly_flip)

                { (0x0A, 0x95); }
Else if (Dponly_normal)

                { (0x0A, 0x92); }
Else if (Dponly_flip)

                { (0x0A, 0x96); }
Else if (DPUSB_normal)

                { (0x0A, 0x93); }
Else if (DPUSB_flip)

                { (0x0A,0x97); }
Else // Nothing connected to Type-C
```

Programming (continued)

```
                { (0x0A, 0x90); }
```

8.5.2.3 Full AEQ with linear redriver mode

```
// (address, data)
// Initial power-on configuration.

                (0x0A, 0x11), // EQ_OVERRIDE and USB3.1 default.

                (0x1C, 0x83), //Full AEQ enable

                (0x10, 0x55), // DP lanes 0 and 1 EQ

                (0x11, 0x55), // DP lanes 2 and 2 EQ

                (0x20, 0x11), // USB-C Rx1/Rx2 EQ. Not used in Full AEQ

                (0x21, 0x05), // SSTX receiver EQ.

// Controls when selecting between USB and DP modes.
If (USBonly_normal)

                { (0x0A,0x11); }
Else if (USBonly_flip)

                { (0x0A, 0x15); }
Else if (Dponly_normal)

                { (0x0A, 0x12); }
Else if (Dponly_flip)

                { (0x0A, 0x16); }
Else if (DPUSB_normal)

                { (0x0A, 0x13); }
Else if (DPUSB_flip)

                { (0x0A,0x17); }
Else // Nothing connected to Type-C

                { (0x0A, 0x10); }
```

8.5.2.4 Full AEQ with limited redriver mode

```
// (address, data)
// Initial power-on configuration.

                (0x0A, 0x91), // Limited Redriver, EQ_OVERRIDE and USB3.1 default.

                (0x0B, 0x24), // Pre-shoot and De-emphasis control

                (0x1C, 0x83), //Full AEQ enable

                (0x10, 0x55), // DP lanes 0 and 1 EQ

                (0x11, 0x55), // DP lanes 2 and 2 EQ

                (0x20, 0x11), // USB-C Rx1/Rx2 EQ. Not used in Full AEQ

                (0x21, 0x05), // SSTX receiver EQ.

                (0x32, 0x40), // VOD Control.

// Controls when selecting between USB and DP modes.
If (USBonly_normal)

                { (0x0A,0x91); }
Else if (USBonly_flip)
```

Programming (continued)

```
                { (0x0A, 0x95); }
Else if (Dponly_normal)

                { (0x0A, 0x92); }
Else if (Dponly_flip)

                { (0x0A, 0x96); }
Else if (DPUSB_normal)

                { (0x0A, 0x93); }
Else if (DPUSB_flip)

                { (0x0A,0x97); }
Else // Nothing connected to Type-C

                { (0x0A, 0x90); }
```

8.5.3 TUSB1146 I²C Address Options

For further programmability, the TUSB1146 can be controlled using I²C. The SCL and SDA pins are used for I²C clock and I²C data respectively.

Table 10. TUSB1146 I²C Target Address

DPEQ0/A1 PIN LEVEL	SSEQ0/A0 PIN LEVEL	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
0	0	1	0	0	0	1	0	0	0/1
0	R	1	0	0	0	1	0	1	0/1
0	F	1	0	0	0	1	1	0	0/1
0	1	1	0	0	0	1	1	1	0/1
R	0	0	1	0	0	0	0	0	0/1
R	R	0	1	0	0	0	0	1	0/1
R	F	0	1	0	0	0	1	0	0/1
R	1	0	1	0	0	0	1	1	0/1
F	0	0	0	1	0	0	0	0	0/1
F	R	0	0	1	0	0	0	1	0/1
F	F	0	0	1	0	0	1	0	0/1
F	1	0	0	1	0	0	1	1	0/1
1	0	0	0	0	1	1	0	0	0/1
1	R	0	0	0	1	1	0	1	0/1
1	F	0	0	0	1	1	1	0	0/1
1	1	0	0	0	1	1	1	1	0/1

8.5.4 TUSB1146 I²C Slave Behavior

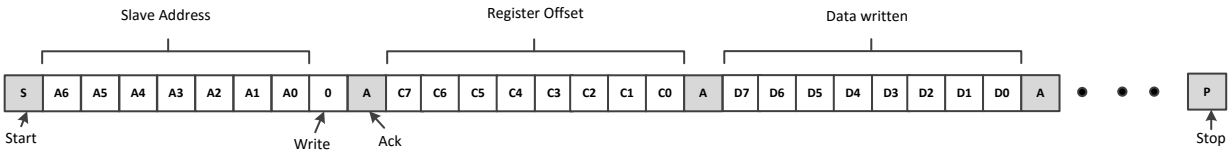


Figure 29. I2C Write with Data

The following procedure should be followed to write data to TUSB1146 I²C registers (refer to Figure 29):

1. The master initiates a write operation by generating a start condition (S), followed by the TUSB1146 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB1146 acknowledges the address cycle.
3. The master presents the register offset within TUSB1146 to be written, consisting of one byte of data, MSB-first.

4. The TUSB1146 acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I^{2}C register.
6. The TUSB1146 acknowledges the byte transfer
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TUSB1146.
8. The master terminates the write operation by generating a stop condition (P).

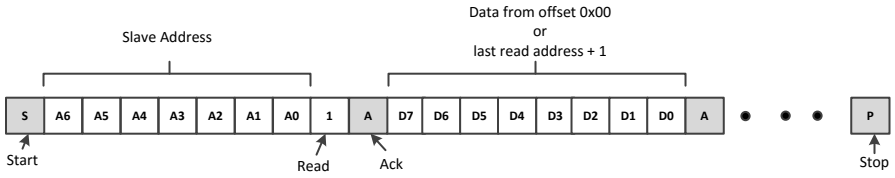


Figure 30. I2C Read without repeated Start

The following procedure should be followed to read the TUSB1146 I^{2}C registers without a repeated Start (refer Figure 30).

1. The master initiates a read operation by generating a start condition (S), followed by the TUSB1146 7-bit address and a zero-value “W/R” bit to indicate a read cycle.
2. The TUSB1146 acknowledges the 7-bit address cycle.
3. Following the acknowledge the master continues sending clock.
4. The TUSB1146 transmit the contents of the memory registers MSB-first starting at register 00h or last read register offset+1. If a write to the I^{2}C register occurred prior to the read, then the TUSB1146 shall start at the register offset specified in the write.
5. The TUSB1146 waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I^{2}C master acknowledges reception of each data byte transfer.
6. If an ACK is received, the TUSB1146 transmits the next byte of data as long as master provides the clock. If a NAK is received, the TUSB1146 stops providing data and waits for a stop condition (P).
7. The master terminates the write operation by generating a stop condition (P).

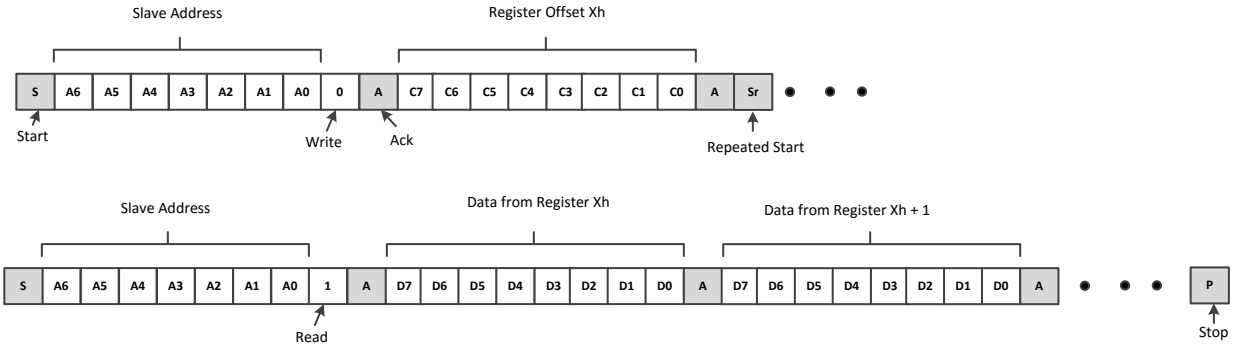


Figure 31. I2C Read with repeated Start

The following procedure should be followed to read the TUSB1146 I^{2}C registers with a repeated Start (refer Figure 31).

1. The master initiates a read operation by generating a start condition (S), followed by the TUSB1146 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB1146 acknowledges the 7-bit address cycle.
3. The master presents the register offset within TUSB1146 to be written, consisting of one byte of data, MSB-first.
4. The TUSB1146 acknowledges the register offset cycle.
5. The master presents a repeated start condition (Sr).
6. The master initiates a read operation by generating a start condition (S), followed by the TUSB1146 7-bit

address and a one-value “W/R” bit to indicate a read cycle.

7. The TUSB1146 acknowledges the 7-bit address cycle.
8. The TUSB1146 transmit the contents of the memory registers MSB-first starting at the register offset.
9. The TUSB1146 shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I^2C master acknowledges reception of each data byte transfer.
10. If an ACK is received, the TUSB1146 transmits the next byte of data as long as master provides the clock. If a NAK is received, the TUSB1146 stops providing data and waits for a stop condition (P).
11. The master terminates the read operation by generating a stop condition (P).

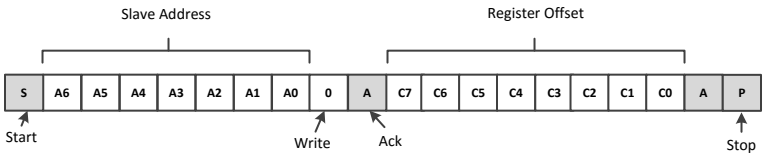


Figure 32. I2C Write without data

The following procedure should be followed for setting a starting sub-address for I^2C reads (refer to Figure 32).

1. The master initiates a write operation by generating a start condition (S), followed by the TUSB1146 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB1146 acknowledges the address cycle.
3. The master presents the register offset within TUSB1146 to be written, consisting of one byte of data, MSB-first.
4. The TUSB1146 acknowledges the register offset cycle.
5. The master terminates the write operation by generating a stop condition (P).

NOTE

After initial power-up, if no register offset is included for the read procedure (refer to Figure 30), then reads start at register offset 00h and continue byte by byte through the registers until the I^2C master terminates the read operation. During a read operation, the TUSB1146 auto-increments the I^2C internal register address of the last byte transferred independent of whether or not an ACK was received from the I2C master.

8.6 Register Maps

8.6.1 TUSB1146 Registers

Table 11 lists the TUSB1146 registers. All register offset addresses not listed in Table 11 should be considered as reserved locations and the register contents should not be modified.

Table 11. TUSB1146 Registers

Offset	Acronym	Register Name	Section
0xA	General_1	General Register	Go
0xB	DCI_TXEQ_CTRL	DCI and TX EQ Control	Go
0x10	DP01EQ_SEL	DisplayPort Lane 0 and 1 EQ Control	Go
0x11	DP23EQ_SEL	DisplayPort Lane 2 and 3 EQ Control	Go
0x12	DisplayPort_1	AUX Snoop Status	Go
0x13	DisplayPort_2	DP Lane Enable/Disable Control	Go
0x1C	AEQ_CONTROL1	AEQ Controls	Go
0x1D	AEQ_CONTROL2	AEQ Controls	Go
0x1E	AEQ_LONG	AEQ setting for Long channel	Go
0x20	USBC_EQ	EQ control for RX1 and RX2 receivers	Go
0x21	SS_EQ	EQ Control for SSTX receiver	Go
0x22	USB3_MISC	Misc USB3 Controls	Go
0x24	USB_STATUS	USB state machine status	Go
0x32	VOD_CTRL	VOD Linearity and AEQ Controls	Go
0x3B	AEQ_STATUS	Full and Fast AEQ status	Go

Complex bit access types are encoded to fit into small table cells. Table 12 shows the codes that are used for access types in this section.

Table 12. TUSB1146 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1S	W 1S	Write 1 to set
WS	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.1.1 General_1 Register (Offset = 0xA) [reset = 0x1]

General_1 is shown in Table 13.

Return to the Summary Table.

This register is used to select between USB and DisplayPort modes as well as selecting the orientation of the MUX. Software should set EQ_OVERRIDE bit in order for EQ registers to be used instead of pins.

Table 13. General_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SSRX_LIMIT_ENABLE	R/W	0x0	Limited redriver mode enable for SSRX transmitter. 0x0 = Linear Redriver 0x1 = Limited Redriver
6	RESERVED	R	0x0	Reserved
5	SWAP_HPDIN	R/W	0x0	Controls which pin HPDIN is derived from. Please note a sideaffect of setting this bit is DCI function will be disabled. Therefore if DCI support is required, then this field must remain cleared. 0x0 = HPDIN is in default location 0x1 = HPDIN location is swapped (PIN 23 to PIN 32, or PIN 32 to PIN 23).
4	EQ_OVERRIDE	R/W	0x0	Setting this field will allow software to use EQ settings from registers instead of value sampled from pins. 0x0 = EQ settings based on sampled state of EQ pins. 0x1 = EQ settings based on programmed value of each of the EQ registers.
3	HPDIN_OVERRIDE	R/W	0x0	Overrides HPDIN pin state. 0x0 = HPD_IN based on HPD_IN pin. 0x1 = HPD_IN high.
2	FLIP_SEL	R/W	0x0	This field controls the orientation. 0x0 = Normal Orientation 0x1 = Flip orientation.
1-0	CTLSEL	R/W	0x1	Controls the DP and USB modes. 0x0 = Disabled. All RX and TX for USB3 and DisplayPort are disabled. 0x1 = USB3.1 only enabled. 0x2 = Four Lanes of DisplayPort enabled. 0x3 = USB3.1 and Two DisplayPort Lanes.

8.6.1.2 DCI_TXEQ_CTRL Register (Offset = 0xB) [reset = 0x6C]

DCI_TXEQ_CTRL is shown in Table 14.

Return to the Summary Table.

This register controls the pre-shoot and de-emphasis levels for SSRX when limited redriver mode is enabled.

Table 14. DCI_TXEQ_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	TX_PRESHOOT	R/W	0x1	SSRX TX preshoot level (pre-cursor). 0x0 = 1.5dB 0x1 = 2dB 0x2 = 2.3dB 0x3 = 2.8dB
5	TX_PRESHOOT_EN	R/W	0x1	SSRX TX preshoot (pre-cursor) enabled. Valid only when SSRX_LIMIT_ENABLE = 1. 0x0 = Disabled (0dB) 0x1 = Enabled

Table 14. DCI_TXEQ_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-3	TX_DEEPHASIS	R/W	0x1	SSRX TX de-emphasis level (post-cursor) 0x0 = -1.5dB 0x1 = -2.1dB 0x2 = -3.2dB 0x3 = -3.8dB
2	TX_DEEPHASIS_EN	R/W	0x1	SSRX TX de-emphasis (post-cursor) enable. Valid only when SSRX_LIMIT_ENABLE = 1. 0x0 = Disabled (0dB) 0x1 = Enabled
1-0	DCI_CTL	R/W	0x0	Controls whether or not DCI function is enabled by FSM or software. 0x0 = DCI controlled by FSM 0x1 = DCI enabled using RX1P/N 0x2 = DCI enabled using RX2P/N 0x3 = DCI disabled.

8.6.1.3 DP01EQ_SEL Register (Offset = 0x10) [reset = 0x0]

DP01EQ_SEL is shown in Table 15.

Return to the Summary Table.

This register controls the receiver equalization setting for the DisplayPort receivers 0 and 1.

Table 15. DP01EQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DP1EQ_SEL	RH/W	0x0	Field selects EQ for DP lane 1 pins. When EQ_OVERRIDE = 0b, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for DP Lane 1 based on value written to this field.
3-0	DP0EQ_SEL	RH/W	0x0	Field selects EQ for DP lane 0 pins. When EQ_OVERRIDE = 0b, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for DP Lane 0 based on value written to this field.

8.6.1.4 DP23EQ_SEL Register (Offset = 0x11) [reset = 0x0]

DP23EQ_SEL is shown in Table 16.

Return to the Summary Table.

This register controls the receiver equalization setting for the DisplayPort receivers 2 and 3.

Table 16. DP23EQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DP3EQ_SEL	RH/W	0x0	Field selects EQ for DP lane 3 pins. When EQ_OVERRIDE = 0b, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for DP Lane 3 based on value written to this field.
3-0	DP2EQ_SEL	RH/W	0x0	Field selects EQ for DP lane 2 pins. When EQ_OVERRIDE = 0b, this field reflects the sampled state of DPEQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for DP Lane 2 based on value written to this field.

8.6.1.5 DisplayPort_1 Register (Offset = 0x12) [reset = 0x0]

DisplayPort_1 is shown in Table 17.

Return to the Summary Table.

This register provides status of AUX snooping when AUX Snooping is enabled.

Table 17. DisplayPort_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6-5	SET_POWER_STATE	RH	0x0	This field represents the snooped value of the AUX write to DPCD address 0x00600. When AUX_SNOOP_DISABLE = 0b, the enable/disable of DP lanes based on the snooped value. When AUX_SNOOP_DISABLE = 1b, then DP lane enable/disable are determined by state of DPx_DISABLE registers, where x = 0, 1, 2, or 3. This field is reset to 0h by hardware when CTLSEL1 changes from a 1b to a 0b.
4-0	LANE_COUNT_SET	RH	0x0	This field represents the snooped value of AUX write to DPCD address 0x00101 register. When AUX_SNOOP_DISABLE = 0b, DP lanes enabled specified by the snoop value. Unused DP lanes will be disabled to save power. When AUX_SNOOP_DISABLE = 1b, then DP lanes enable/disable are determined by DPx_DISABLE registers, where x = 0, 1, 2, or 3. This field is reset to 0h by hardware when CTLSEL1 changes from a 1b to a 0b.

8.6.1.6 DisplayPort_2 Register (Offset = 0x13) [reset = 0x0]

DisplayPort_2 is shown in Table 18.

Return to the Summary Table.

This register provides controls for enabling and disabling AUX snooping and individual DP lanes.

Table 18. DisplayPort_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	AUX_SNOOP_DISABLE	R/W	0x0	Controls whether DP lanes are enabled based on AUX snooped value or registers. 0x0 = AUX snoop enabled. 0x1 = AUX snoop disabled. DP lanes are controlled by registers.
6	RESERVED	R	0x0	Reserved
5-4	AUX_SBU_OVR	R/W	0x0	This field overrides the AUXP/N to SBU1/2 connect and disconnect based on CTL1 and FLIP. Changing this field to 01b or 10b will allow traffic to pass through AUX to SBU regardless of the state of CTLSEL1 and FLIPSEL register. 0x0 = AUX to SBU connection determined by CTLSEL1 and FLIPSEL 0x1 = AUXP -> SBU1 and AUXN -> SBU2 0x2 = AUXP -> SBU2 and AUXN -> SBU1 0x3 = AUX to SBU open.
3	DP3_DISABLE	R/W	0x0	When AUX_SNOOP_DISABLE = 1b, this field can be used to enable or disable DP lane 3. When AUX_SNOOP_DISABLE = 0b, changes to this field will have no effect on lane 3 functionality. 0x0 = DP Lane 3 enabled. 0x1 = DP Lane 3 disabled.

Table 18. DisplayPort_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	DP2_DISABLE	R/W	0x0	When AUX_SNOOP_DISABLE = 1b, this field can be used to enable or disable DP lane 2. When AUX_SNOOP_DISABLE = 0b, changes to this field will have no effect on lane 2 functionality. 0x0 = DP Lane 2 enabled. 0x1 = DP Lane 2 disabled.
1	DP1_DISABLE	R/W	0x0	When AUX_SNOOP_DISABLE = 1b, this field can be used to enable or disable DP lane 1. When AUX_SNOOP_DISABLE = 0b, changes to this field will have no effect on lane 1 functionality. 0x0 = DP Lane 1 enabled. 0x1 = DP Lane 1 disabled.
0	DP0_DISABLE	R/W	0x0	When AUX_SNOOP_DISABLE = 1b, this field can be used to enable or disable DP lane 0. When AUX_SNOOP_DISABLE = 0b, changes to this field will have no effect on lane 0 functionality. 0x0 = DP Lane 0 enabled. 0x1 = DP Lane 0 disabled.

8.6.1.7 AEQ_CONTROL1 Register (Offset = 0x1C) [reset = 0xF0]

AEQ_CONTROL1 is shown in Table 19.

Return to the Summary Table.

This register is used to enable adaptive EQ and select between Fast and Full adaptive EQ.

Table 19. AEQ_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	FULLAEQ_UPPER_EQ	R/W	0xF	Maximum EQ value to check for full AEQ mode
3	USB3_U1_DISABLE	R/W	0x0	This field when set will cause entry to U3 instead of U1 when electrical idle is detected. 0x0 = U1 entry after electrical idle. 0x1 = U3 entry after electrical idle.
2-1	AEQ_MODE	R/W	0x0	Selects between Fast and 2 Full Adaption modes 0x0 = Fast AEQ. 0x1 = Full AEQ with hits counted at mideye for every EQ. 0x2 = Fast AEQ. 0x3 = Full AEQ with hits counted at mideye only for EQ equal 0.
0	AEQ_EN	R/W	0x0	Controls whether or not adaptive EQ for USB downstream facing port is enabled. 0x0 = AEQ disabled 0x1 = AEQ enabled

8.6.1.8 AEQ_CONTROL2 Register (Offset = 0x1D) [reset = 0x20]

AEQ_CONTROL2 is shown in Table 20.

Return to the Summary Table.

This register allows for controls for the Fast AEQ limits as well as adding or reducing final EQ value used by the Full AEQ function.

Table 20. AEQ_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OVER_EQ_SIGN	R/W	0x0	Selects the sign for OVER_EQ_CTRL field. 0x0 = positive 0x1 = negative
6	RESERVED	R	0x0	Reserved
5-3	FASTAEQ_LIMITS	R/W	0x4	Selects the upper/lower limits of DAC for determining short vs long channel. 0x0 = +/- 0mV 0x1 = +/- 40mV 0x2 = +/- 80mV 0x3 = +/- 120mV 0x4 = +/- 160mV 0x5 = +/- 200mV 0x6 = +/- 240mV 0x7 = +/- 280mV
2-0	OVER_EQ_CTRL	R/W	0x0	This field will increase or decrease the AEQ by value programmed into this field. For example, full AEQ value is 6 and this field is programmed to 2 and OVER_EQ_SIGN = 0, then EQ value used will be 8. This field is only used in Full AEQ mode. 0x0 = 0 or -8 0x1 = 1 or -7 0x2 = 2 or -6 0x3 = 3 or -5 0x4 = 4 or -4 0x5 = 5 or -3 0x6 = 6 or -2 0x7 = 7 or -1

8.6.1.9 AEQ_LONG Register (Offset = 0x1E) [reset = 0x77]

AEQ_LONG is shown in Table 21.

Return to the Summary Table.

This register is used to program the EQ used for long channel setting when Fast AEQ is enabled.

Table 21. AEQ_LONG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LONG_EQ2	R/W	0x7	When AEQ_EN = 1 and AEQ_MODE = x0, selects EQ setting for USB downstream facing port1 (RX2) when long channel is detected. Value programmed into this field should provide best Rx JTOL results for long channel configuration.
3-0	LONG_EQ1	R/W	0x7	When AEQ_EN = 1 and AEQ_MODE = x0, selects EQ setting for USB downstream facing port2 (RX1) when long channel is detected. Value programmed into this field should provide best Rx JTOL results for long channel configuration.

8.6.1.10 USBC_EQ Register (Offset = 0x20) [reset = 0x0]

USBC_EQ is shown in Table 22.

Return to the Summary Table.

This register controls the receiver equalization setting for the DFP (RX1 and RX2).

Table 22. USBC_EQ Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	EQ2_SEL	RH/W	0x0	If AEQ_EN = 0, this field selects EQ for USB3.1 RX2 receiver which faces the USB-C receptacle. When EQ_OVERRIDE = 0b, this field reflects the sampled state of EQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for RX2p/n pins based on value written to this field. When AEQ_EN = 1 and AEQ_MODE = x0, selects EQ setting for USB downstream facing port1 (RX2) when short channel is detected. Value programmed into this field should provide best Rx JTOL results for short channel configuration.
3-0	EQ1_SEL	RH/W	0x0	If AEQ_EN = 0, this field selects EQ for USB3.1 RX1 receiver which faces the USB-C receptacle. When EQ_OVERRIDE = 0b, this field reflects the sampled state of EQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for RX1p/n pins based on value written to this field. When AEQ_EN = 1 and AEQ_MODE = x0, selects EQ setting for USB downstream facing port1 (RX1) when short channel is detected. Value programmed into this field should provide best Rx JTOL results for short channel configuration.

8.6.1.11 SS_EQ Register (Offset = 0x21) [reset = 0x0]

SS_EQ is shown in Table 23.

Return to the Summary Table.

This register controls the receiver equalization setting for the UFP (SSTX).

Table 23. SS_EQ Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0x0	Reserved
3-0	SSEQ_SEL	RH/W	0x0	This field selects EQ for USB3.1 SSTX receiver which faces the USB host. When EQ_OVERRIDE = 0b, this field reflects the sampled state of SSEQ[1:0] pins. When EQ_OVERRIDE = 1b, software can change the EQ setting for SSTXp/n pins based on value written to this field.

8.6.1.12 USB3_MISC Register (Offset = 0x22) [reset = 0x44]

USB3_MISC is shown in Table 24.

Return to the Summary Table.

Table 24. USB3_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RXD_START_TERM	R/W	0x0	Termination setting at start of RX detection following warm reset and at entry to SS.Inactive. 0x0 = Maintain termination. Same as tusb1046 0x1 = Turn off termination. Avoid compliance failures due to race between local and remote rxd in case of disconnect. If connection remains next state was polling regardless.
6	LFPS_EQ	R/W	0x1	Controls whether settings of EQ based on EQ1_SEL, EQ2_SEL, and SSEQ_SEL applies to received LFPS signal. 0x0 = EQ set to zero when receiving LFPS 0x1 = EQ set by the related registers when receiving LFPS.
5	U2U3_LFPS_DEBOUNCE	R/W	0x0	Controls whether or not incoming LFPS is debounced or not. 0x0 = No debounce of LFPS before U2/U3 exit. 0x1 = 200us debounce of LFPS before U2/U3 exit.

Table 24. USB3_MISC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DISABLE_U2U3_RXDET	R/W	0x0	Controls whether or not Rx.Detect is performed in U2/U3 state. 0x0 = Rx.Detect in U2/U3 enabled. 0x1 = Rx.Detect in U2/U3 disabled.
3-2	DFP_RXDET_INTERVAL	R/W	0x1	This field controls the Rx.Detect interval for the downstream facing port (TX1P/N and TX2P/N). 0x0 = 4ms 0x1 = 6ms 0x2 = 36ms 0x3 = 84ms
1	DIS_WARM_RESET_RXD	R/W	0x0	Disables receiver detection following warm reset if device starts polling during warm reset.. 0x0 = whether receiver detection is done following warm reset depends on other settings. 0x1 = if USB FSM detects that device started polling during warm reset, it will not do receiver detection.
0	USB_COMPLIANCE_CTRL	R/W	0x0	Controls whether compliance mode detection is determined by FSM or disabled 0x0 = Compliance mode determined by FSM. 0x1 = Compliance mode disabled.

8.6.1.13 USB_STATUS Register (Offset = 0x24) [reset = 0x41]

USB_STATUS is shown in Table 25.

Return to the Summary Table.

Table 25. USB_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	USB_FASTAEQ_STAT	RH	0x0	When AEQ_EN = 1 and AEQ_MODE = x0, this status field indicates whether short or long EQ setting is used. When AEQ_EN = 0, this field will always default to 0h. 0x0 = Short channel EQ used. 0x1 = Long channel EQ used.
6	USB_AEQDONE_STAT	RH	0x1	This field is low while AEQ is active and high when it is done. It is valid when U0_STAT and AEQ_EN = 1 or when FORCE_AEQ_EN = 1 and HW has reset FORCE_AEQ back to 0. 0x0 = AEQ is running 0x1 = AEQ is done
5	AEQ_HC_OVERFLOW	RH	0x0	13-bit AEQ hit counter overflow status
4	RESERVED	R	0x0	Reserved
3	CM_ACTIVE	RH	0x0	Compliance mode status. 0x0 = Not in USB3.1 compliance mode. 0x1 = In USB3.1 compliance mode.
2	U0_STAT	RH	0x0	U0 Status. Set if enters U0 state.
1	U2U3_STAT	RH	0x0	U2/U3 Status. Set if enters U2/U3 state.
0	DISC_STAT	RH	0x1	Disconnect Status. Set if enters Disconnect state.

8.6.1.14 VOD_CTRL Register (Offset = 0x32) [reset = 0x40]

VOD_CTRL is shown in Table 26.

Return to the Summary Table.

This register controls the transmitters output linearity range for both UFP and DFP. When device is configured for limited redriver (SSRX_LIMIT_ENABLE field is set), USB_SSRX_VOD controls the VOD level for SSRX limited driver.

Table 26. VOD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LFPS_TX12_VOD	R/W	0x1	VOD linearity control for TX1 or TX2 when LFPS is being transmitted. 0x0 = LINR_L3 (highest) 0x1 = LINR_L2 0x2 = LINR_L1 0x3 = LINR_L0 (lowest)
5-4	DP_VOD	R/W	0x0	VOD linearity control for DP paths. 0x0 = LINR_L3 (highest) 0x1 = LINR_L2 0x2 = LINR_L1 0x3 = LINR_L0 (lowest)
3-2	USB_TX12_VOD	R/W	0x0	VOD linearity control for USB downstream facing ports (TX1 and TX2). 0x0 = LINR_L3 (highest) 0x1 = LINR_L2 0x2 = LINR_L1 0x3 = LINR_L0 (lowest)
1-0	USB_SSRX_VOD	R/W	0x0	VOD linearity control for USB upstream facing port (SSRX). When SSRX_LIMIT_ENABLE = 1, then this field controls the limited VOD for SSRX. 0x0 = LINR_L3 (highest) 0x1 = LINR_L2 0x2 = LINR_L1 0x3 = LINR_L0 (lowest)

8.6.1.15 AEQ_STATUS Register (Offset = 0x3B) [reset = 0x0]

AEQ_STATUS is shown in Table 27.

Return to the Summary Table.

This register provides the status of AEQ function.

Table 27. AEQ_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved
4	DONE_STAT	RH	0x0	This flag is set after DAC wait timer expires.
3-0	AEQ_STAT	RH	0x0	Optimal EQ determined by FSM after the completion of Full AEQ. This field will also indicate EQ used for Fast AEQ. This field will include the value programmed into OVER_EQ_CTRL field.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TUSB1146 is a linear redriver designed specifically to compensation for intersymbol interference (ISI) jitter caused by signal attenuation through a passive medium like PCB traces and cables. Because the TUSB1146 has four independent DisplayPort 2.0 inputs, one upstream facing USB 3.1 Gen1/Gen2 input, and two downstream facing USB 3.1 Gen1/Gen2 inputs, it can be optimized to correct ISI on all those seven inputs through 16 different equalization choices. Placing the TUSB1146 between a USB3.1 Host/DisplayPort 2.0 GPU and a USB3.1 Type-C receptacle can correct signal integrity issues resulting in a more robust system.

9.2 Typical Application

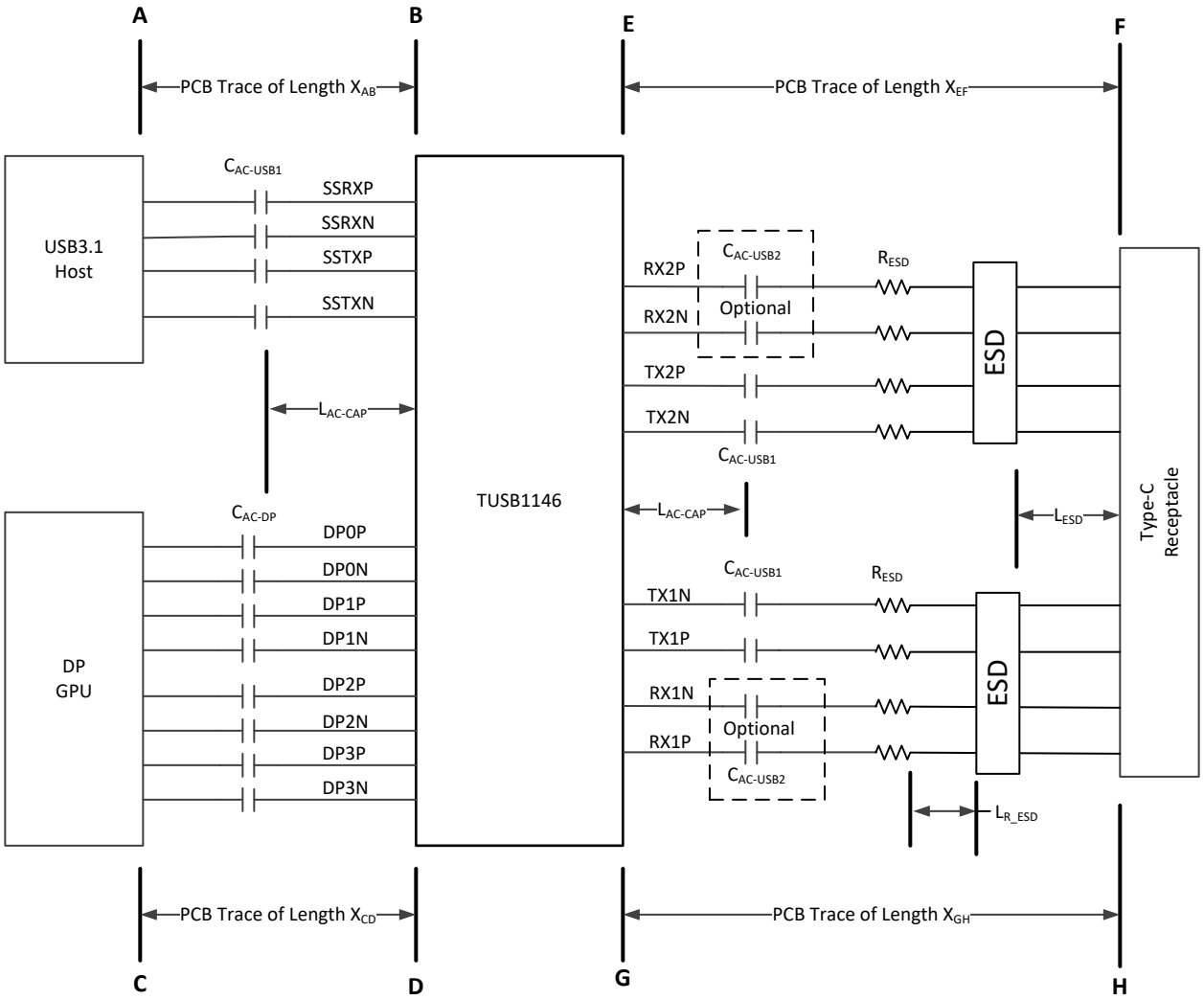


Figure 33. TUSB1146 in a Host Application

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters shown in Table 28.

Table 28. Design Parameters

PARAMETER		VALUE
10Gbps USB3.1 pre-channel A to B PCB trace length, X_{AB}. Refer to Figure 33.		2 inches <= X_{AB} <= 12 inches - [MAX (X_{EF} or X_{GH})]
10Gbps DP pre-channel C to D PCB trace length, X_{CD}. Refer to Figure 33.		4 inches <= X_{CD} <= 14 inches - [MAX (X_{EF} or X_{GH})]
10Gbps USB and DP post channel E to F PCB trace length, X_{EF}. Refer to Figure 33.		up to 4 inches
10Gbps USB and DP post channel G to H PCB trace length, X_{GH}. Refer to Figure 33.		up to 4 inches
Minimum distance of the AC capacitors from TUSB1146, L_{AC-CAP}		0.4 inches
Maximum distance of ESD component from the USB-C receptacle, L_{ESD}		0.5 inches
Maximum distance of series resistor (R_{ESD}) from ESD component, L_{R_ESD}.		0.25 inches
DCI Support (Y/N)		Yes
$C_{AC-USB1}$ AC-coupling capacitor (75 nF to 265 nF)		220 nF
$C_{AC-USB2}$ AC-coupling capacitor (297 nF to 363 nF)	DCI Supported	No AC capacitor. RX1 and RX2 must be DC coupled to USB-C receptacle.
	DCI Not Supported	Options: • RX1 and RX2 are DC coupled to USB-C receptacle • 330nF AC couple with R_{RX} resistor • 330nF AC couple without R_{RX} resistor
Optional R_{RX} resistor (220kΩ +/- 5%)		No used
C_{AC-DP} AC-coupling capacitor (75 nF to 265 nF)		220 nF
R_{ESD} (0 ohms to 2.2 ohms)		1 ohm
V_{CC} supply (3 V to 3.6 V)		3.3 V
I^2C Mode or GPIO Mode		I^2C Mode. (I2C_EN pin != "0")
1.8V or 3.3V I2C Interface		3.3V I2C. Pull-up the I2C_EN pin to 3.3V with a 1K ohm resistor.

9.2.2 Detailed Design Procedure

A typical usage of the TUSB1146 device is shown in Figure 34. The device can be controlled either through its GPIO pins or through its I^2C interface. In the example shown below, a Type-C PD controller is used to configure the device through the I^2C interface. When configured for I^2C mode and system does not support DCI, pins 29 and 32 can be left unconnected. If DCI is supported in the system, then connect through a 22-ohm resistor DCI_CLK and DCI_DAT to appropriate PCH GPIO pins. In I^2C mode, the equalization settings for each receiver can be independently controlled through I^2C registers. For this reason, all of the equalization pins (EQ[1:0], SSEQ[1:0], and DPEQ[1:0]) can be left unconnected. If these pins are left unconnected, the TUSB1146 7-bit I2C slave address will be 0x12 because both DPEQ0/A1 and SSEQ0/A0 will be at pin level "F". If a different I2C slave address is desired, DPEQ0/A1 and SSEQ0/A0 pins should be set to a level which produces the desired I2C slave address.

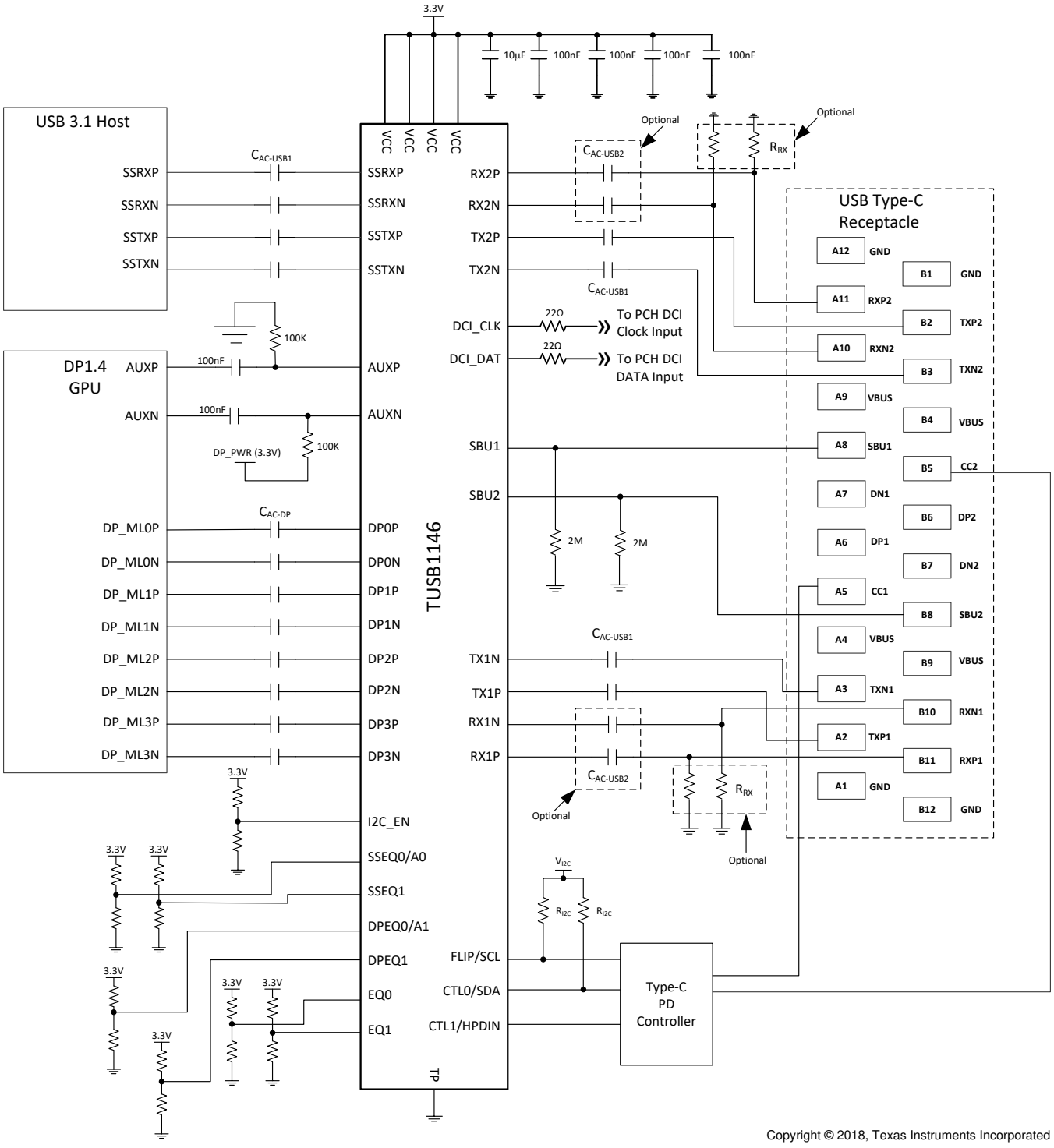


Figure 34. Application Circuit

9.2.2.1 USB and DP Upstream Facing Port (USB Host / DP GPU to USB-C receptacle) Configuration

Configuring the TUSB1146 for the USB and DP downstream direction involves understanding the insertion loss (SDD21) of the pre-channel (X_{AB} and X_{CD}). The TUSB1146's DPEQ[1:0] pins and SSEQ[1:0] pins if GPIO mode ,or if I2C mode, SSEQ_SEL and DPEQx_SEL registers should be set to the level of the pre-channel insertion loss at 5GHz. A good rule of thumb for FR4 trace insertion loss at 5GHz is ~-1dB per inch. Using this rule of thumb, if the pre-channel for USB (X_{AB}) is 8-inches, the TUSB1146 SSEQ should be programmed to -8dB. If the pre-channel insertion loss for DP (X_{CD}) is 10-inches, then DPEQ should be programmed to -10dB. Refer to Table 8 for USB SSEQ settings and to Table 9 for DP EQ settings.

9.2.2.2 USB Downstream Facing Port (USB-C receptacle to USB Host) Configuration

9.2.2.2.1 Fixed Equalization

In Fixed EQ operation, a single EQ setting is used for all possible devices inserted into the USB-C receptacle (with or without USB cable). It is recommended to set TUSB1146 EQ[1:0] pins if GPIO mode, or EQ1_SEL and EQ2_SEL if I2C mode to about 4db to 5dB greater than loss of the post channel (MIN(X_{EF}, X_{GH})). For example, if post channel is 0.5 inches, then assuming -1dB per inch at 5GHz, EQ1_SEL and EQ2_SEL should be programmed to 4.5 to 5.5dB. It is recommended to perform USB3.1 Rx JTOL long and short channel tests to optimize the setting. Depending of the USB 3.1 Host, a single EQ setting which satisfies both the long and short channel tests may not be possible. If this is the case, then it is recommended to use Fast AEQ mode.

9.2.2.2.2 Fast Adaptive Equalization

Fast Adaptive EQ will distinguish between a short and long channel and select a pre-determined EQ setting based on which channel is detected. Fast AEQ is available in both GPIO and I2C mode but it is highly recommended to use this feature when TUSB1146 is configured in I2C mode. In I2C mode Fast AEQ is enabled when AEQ_MODE = 0 and AEQ_EN = 1.

The EQ setting used for short channel should be programmed into EQ1_SEL and EQ2_SEL registers. It is recommended to program these registers about 1dB to 2dB more than the loss of post channel (MIN(X_{EF}, X_{GH})). For example, if post channel is 0.5 inches, then assuming -1dB insertion loss per inch at 5GHz, EQ1_SEL and EQ2_SEL should be programmed to 1.5 to 2.5dB. It is recommended to perform USB3.1 Rx JTOL Short channel test to find the optimal short channel setting.

The EQ setting used for long channel should be programmed into LONG_EQ1 and LONG_EQ2. It is recommended to program these registers about 4 to 5dB more than the loss of post channel (MIN(X_{EF}, X_{GH})). For example, if post channel is 0.5 inches, then assuming -1dB per inch at 5GHz, LONG_EQ1 and LONG_EQ2 should be programmed to 4.5 to 5.5dB. It is recommended to perform USB3.1 Rx JTOL Long channel test to find the optimal long channel setting.

9.2.2.2.3 Full Adaptive Equalization

In Full AEQ mode, the TUSB1146 will always determine the best settings regardless if the channel is short, long or somewhere in between. The Full AEQ feature is disabled by default. Full AEQ is enabled when AEQ_MODE = 1 and AEQ_EN = 0x1 or 0x3.

9.2.3 Application Curve

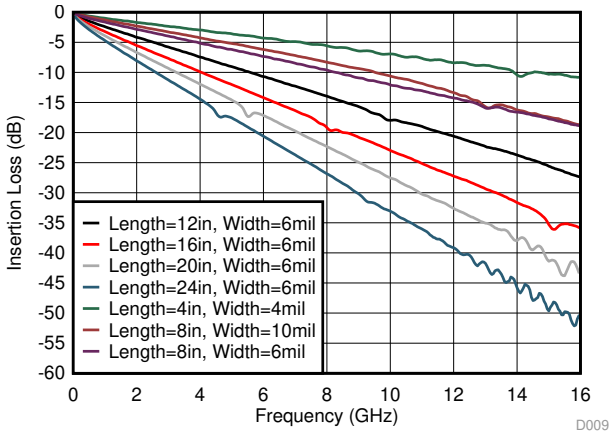


Figure 35. Insertion Loss of FR4 PCB Traces

9.3 System Examples

9.3.1 USB 3.1 Only

The TUSB1146 is in USB3.1 only when the CTL1 pin is low and CTL0 pin is high.

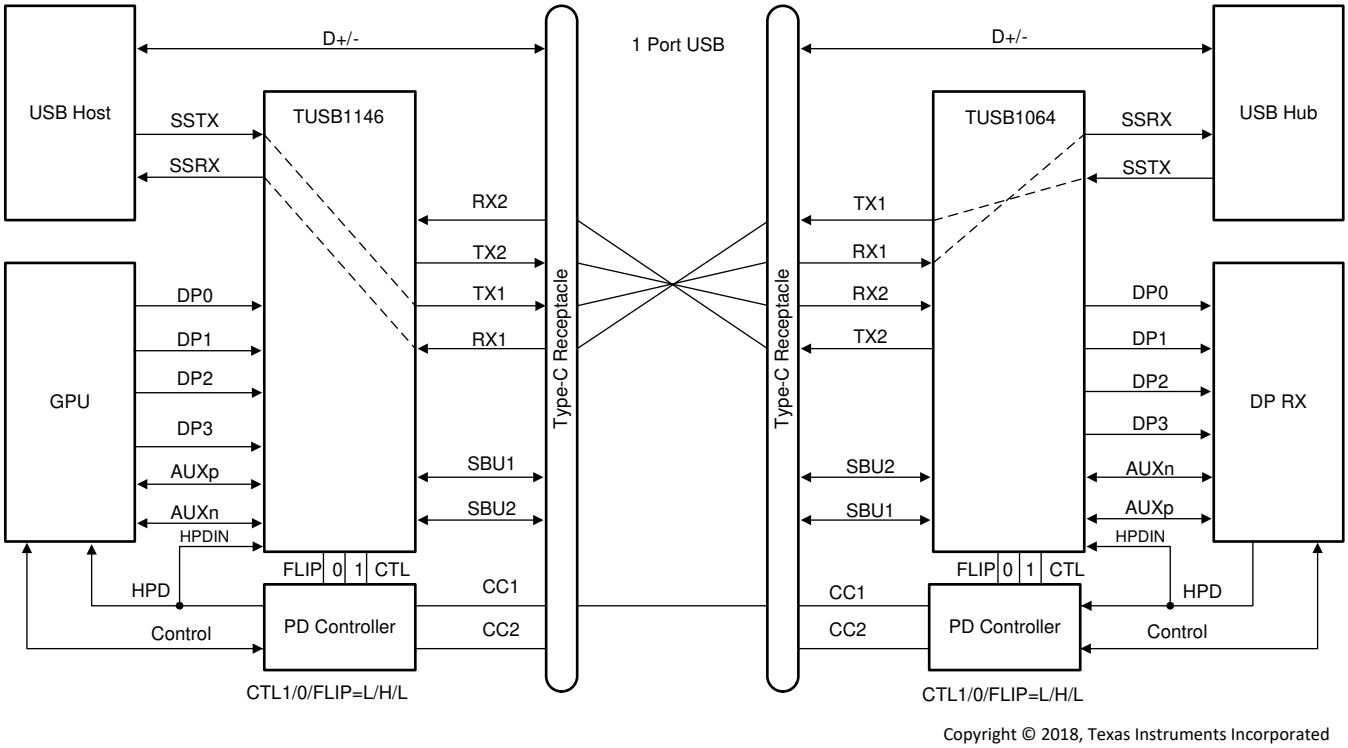


Figure 36. USB3.1 Only – No Flip (CTL1 = L, CTL0 = H, FLIP = L)

System Examples (continued)

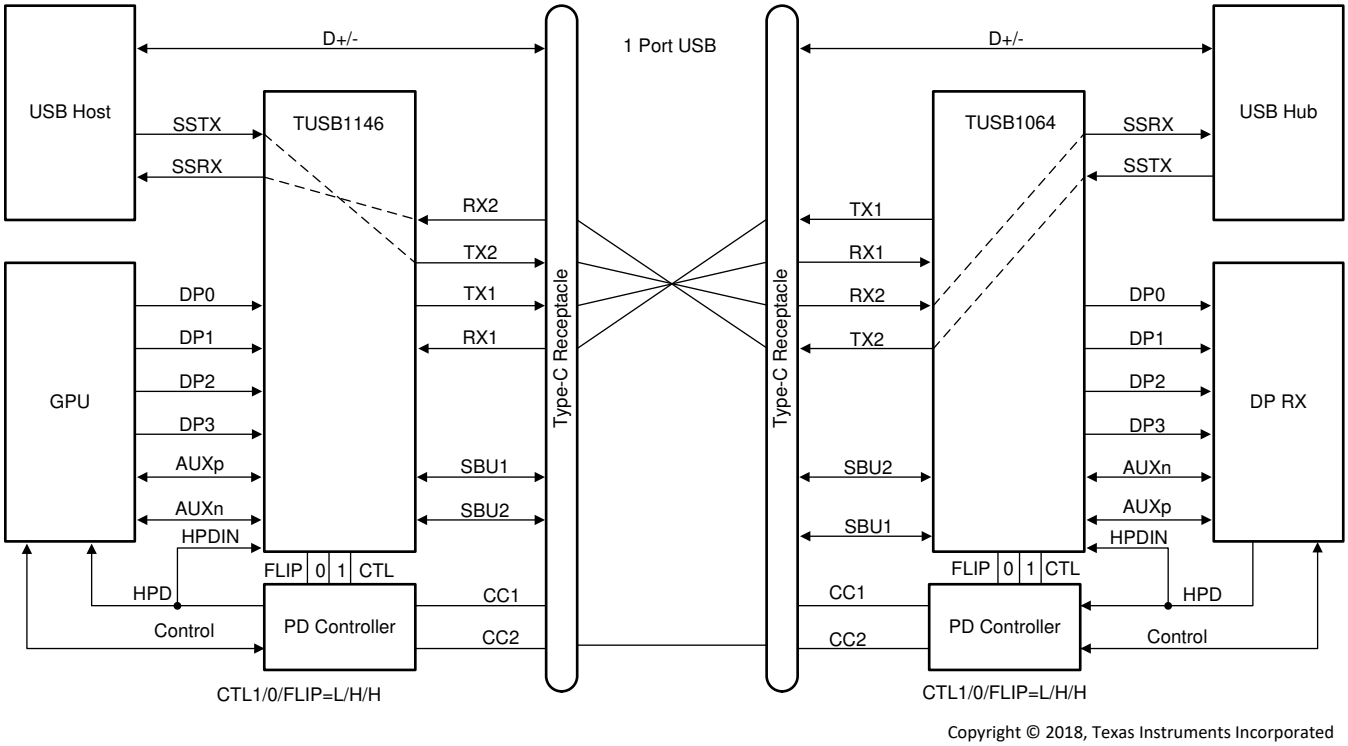


Figure 37. USB3.1 Only – With Flip (CTL1 = L, CTL0 = H, FLIP = H)

System Examples (continued)

9.3.2 USB 3.1 and 2 Lanes of DisplayPort

The TUSB1146 operates in USB3.1 and 2 Lanes of DisplayPort mode when the CTL1 pin is high and CTL0 pin is high.

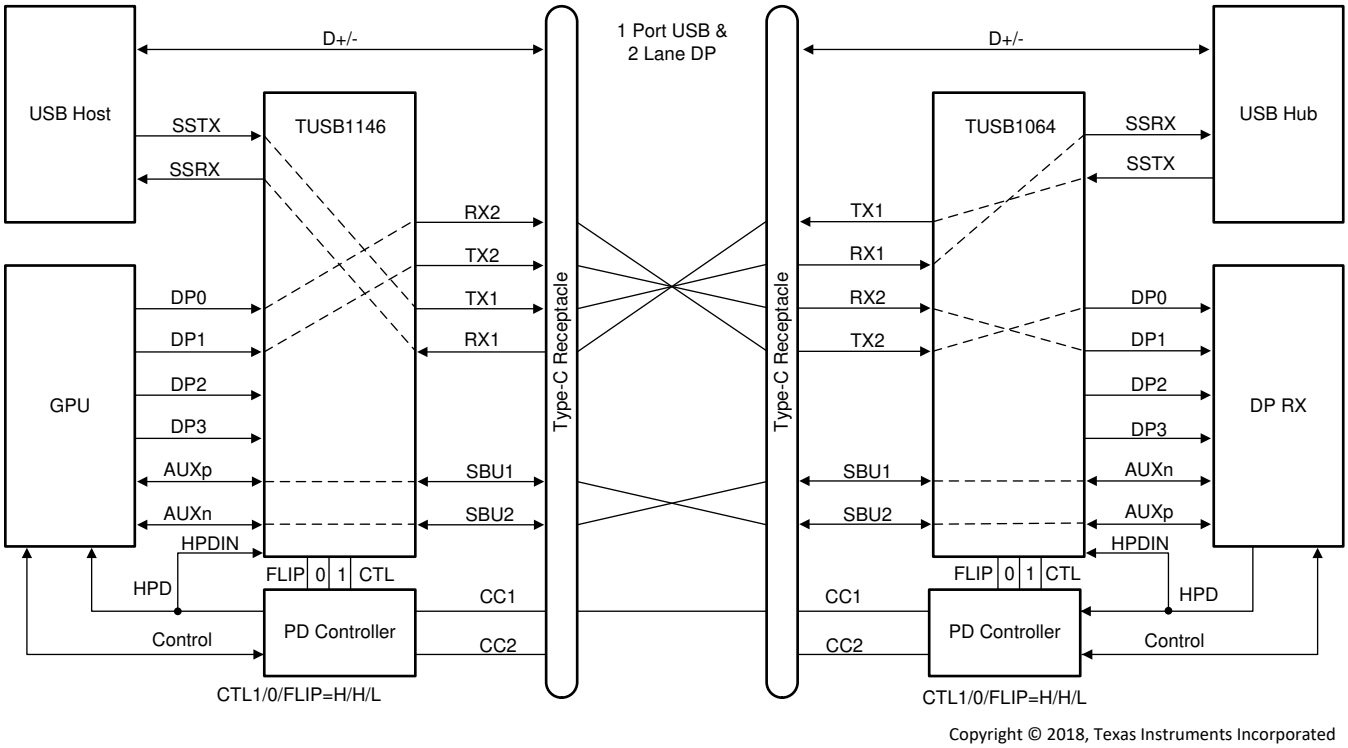


Figure 38. USB3.1 + 2 Lane DP – No Flip (CTL1 = H, CTL0 = H, FLIP = L)

System Examples (continued)

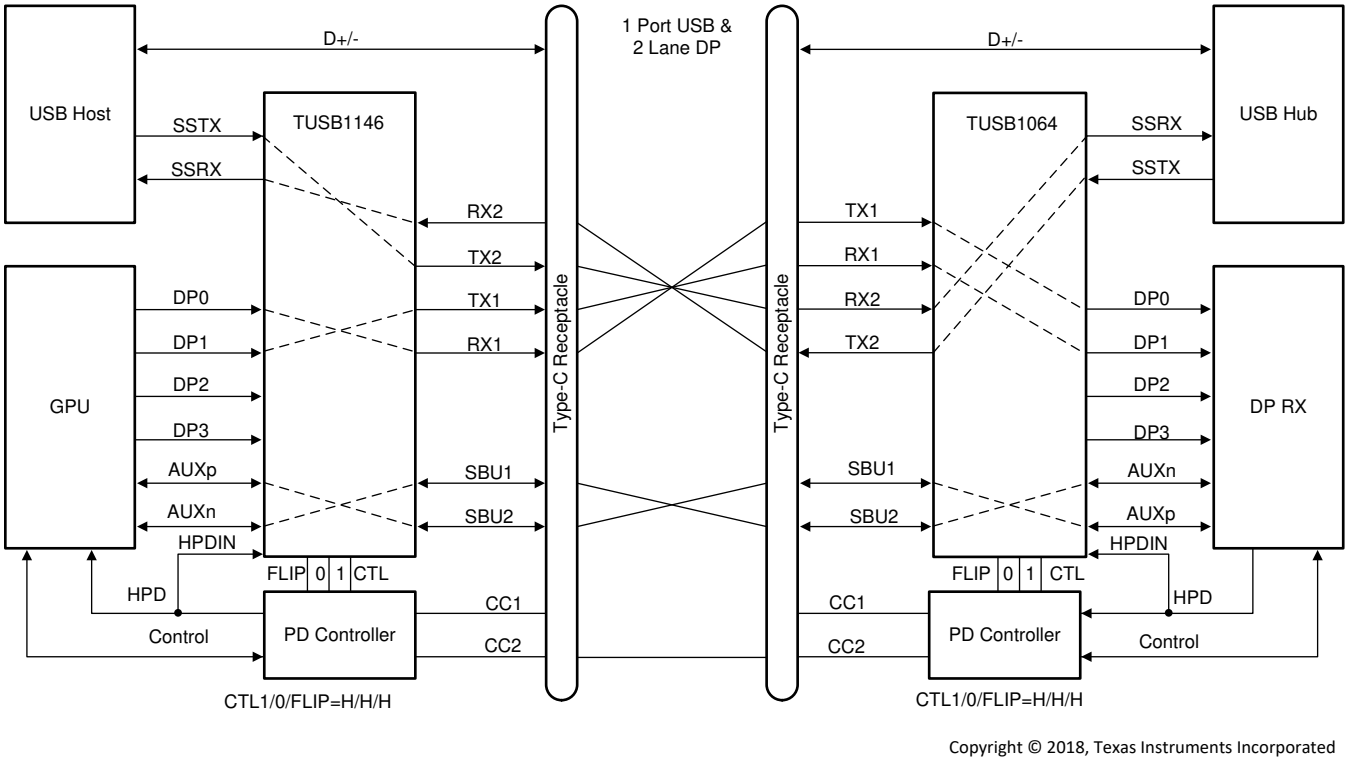


Figure 39. USB 3.1 + 2 Lane DP – Flip (CTL1 = H, CTL0 = H, FLIP = H)

System Examples (continued)

9.3.3 DisplayPort Only

The TUSB1146 operates in 4 Lanes of DisplayPort only mode when the CTL1 pin is high and CTL0 pin is low.

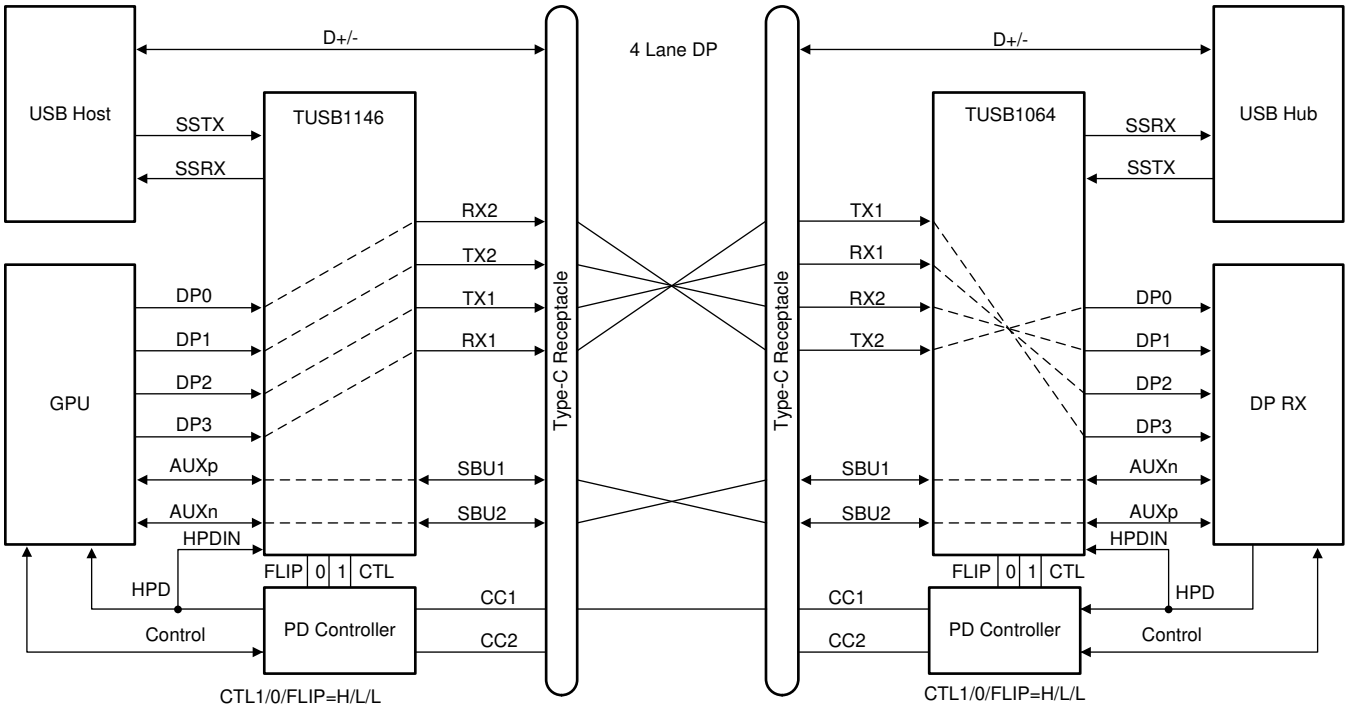


Figure 40. Four Lane DP – No Flip (CTL1 = H, CTL0 = L, FLIP = L)

System Examples (continued)

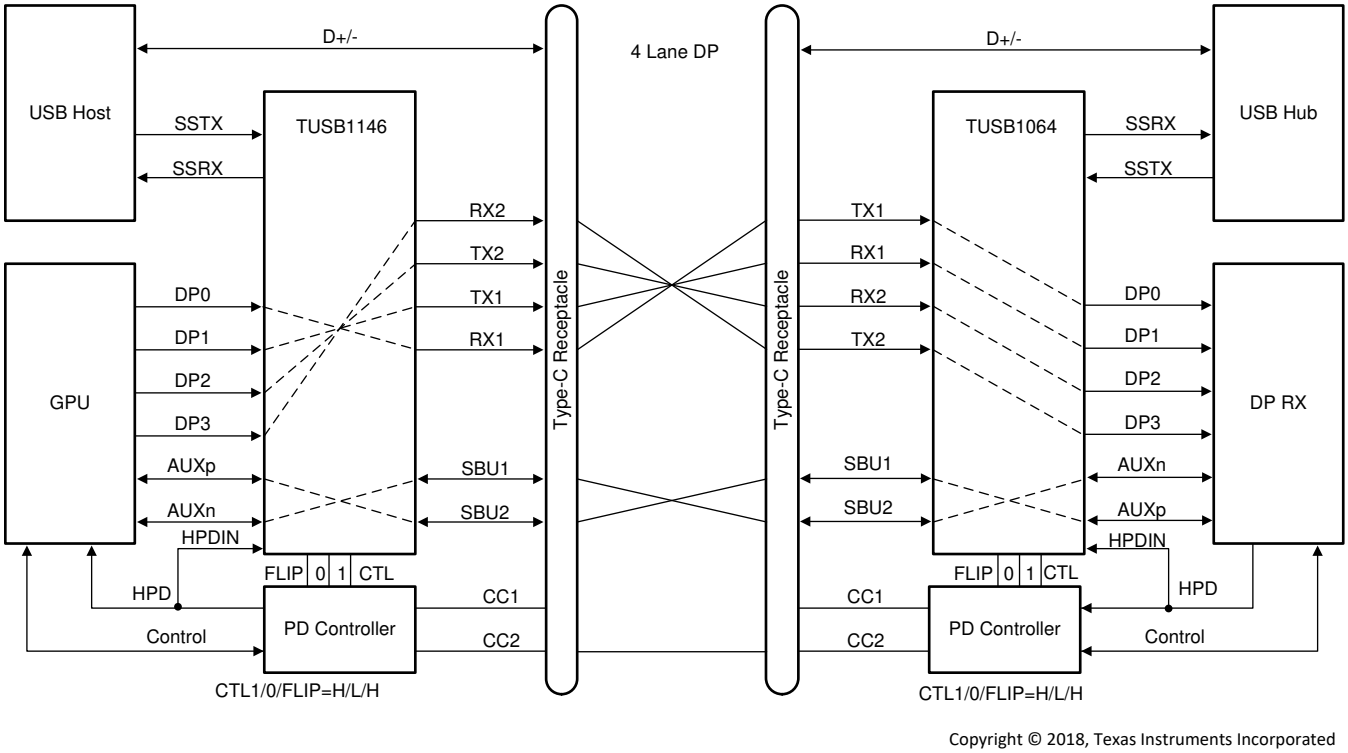


Figure 41. Four Lane DP – With Flip (CTL1 = H, CTL0 = L, FLIP = H)

10 Power Supply Recommendations

The TUSB1146 is designed to operate with a 3.3-V power supply. Levels above those listed in the *Absolute Maximum Ratings* table should not be used. If using a higher voltage system power supply, a voltage regulator can be used to step down to 3.3 V. Decoupling capacitors should be used to reduce noise and improve power supply integrity. A 0.1-µF capacitor should be used on each power pin.

11 Layout

11.1 Layout Guidelines

1. SSTXP/N, SSRXP/N, RX1P/N, RX2PN, TX1P/N, and TX2P/N pairs should be routed with controlled 90-Ω differential impedance (±10%).
2. DP[3:0]P/N pairs should be routed with controlled 90-Ω differential impedance (±10%).
3. There is no inter-pair length match requirement between SSTXP/N and SSRXP/N.
4. Inter-pair matching between DP lanes (DP[3:0]) from GPU through TUSB1146 to the USB-C receptacle should be kept to less than 100 mils.
5. Keep away from other high speed signals.
6. Intra-pair routing (between P and N) should be kept to less than 5 mils.
7. Length matching should be near the location of mismatch.
8. Each pair should be separated at least by 3 times the signal trace width.
9. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This will minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
10. Route all differential pairs on the same of layer.
11. The number of vias should be kept to a minimum. It is recommended to keep the vias count to 2 or less.
12. Keep traces on layers adjacent to ground plane.
13. Do not route differential pairs over any plane split.
14. Adding Test points will cause impedance discontinuity, and therefore, negatively impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.
15. Highly recommended to have reference plane void under USB-C receptacle's super speed pins to minimize the capacitance effect of the receptacle.
16. Highly recommended to have reference plane void under the AC coupling capacitances.

11.2 Layout Example

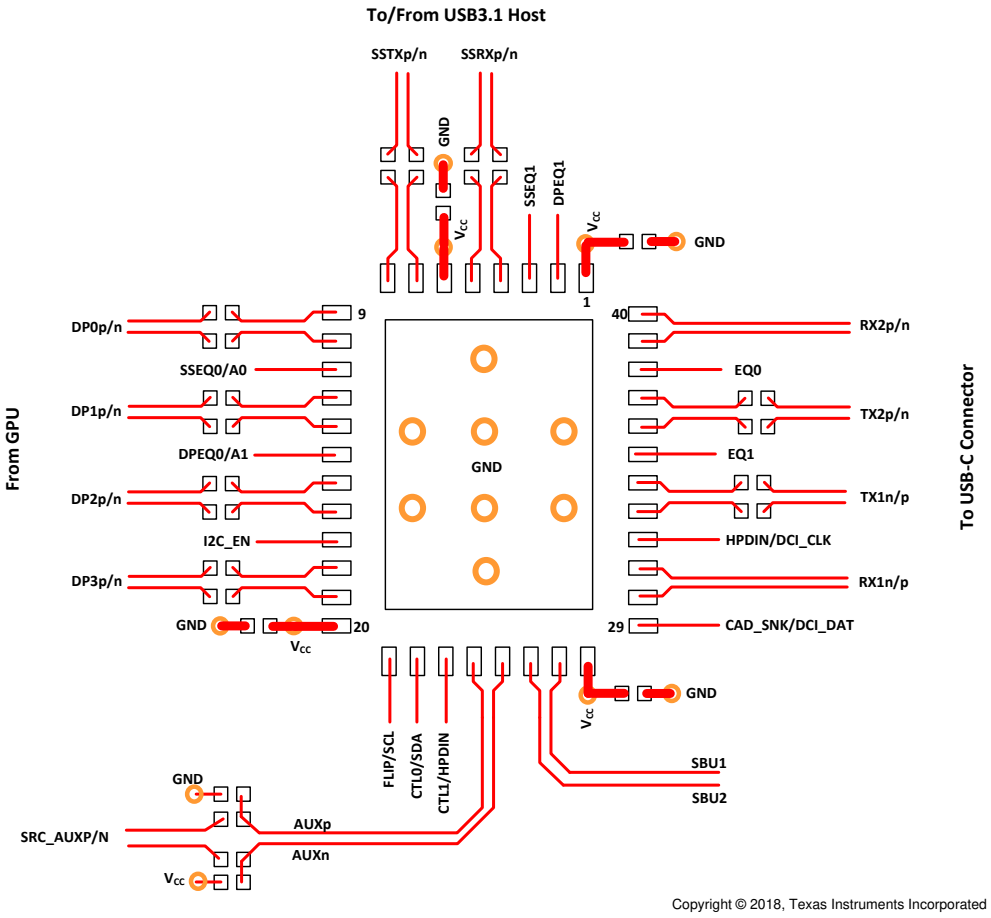


Figure 42. Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

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VESA is a registered trademark of Video Electronics Standards Association Corporation California.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB1146IRNQR	ACTIVE	WQFN	RNQ	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UB11	Samples
TUSB1146IRNQT	ACTIVE	WQFN	RNQ	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UB11	Samples
TUSB1146RNQR	ACTIVE	WQFN	RNQ	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UB11	Samples
TUSB1146RNQT	ACTIVE	WQFN	RNQ	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UB11	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

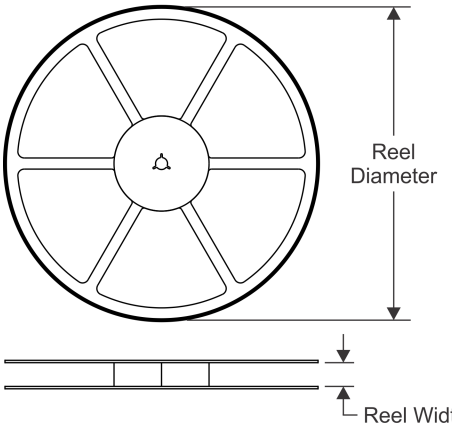
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

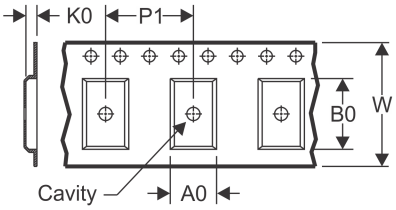
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

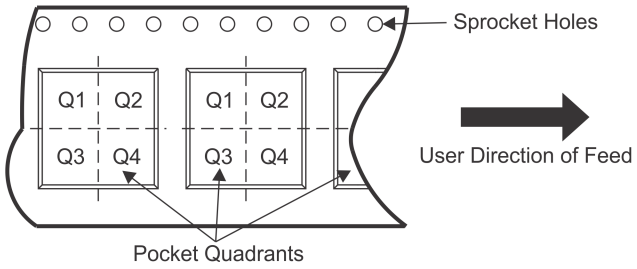


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

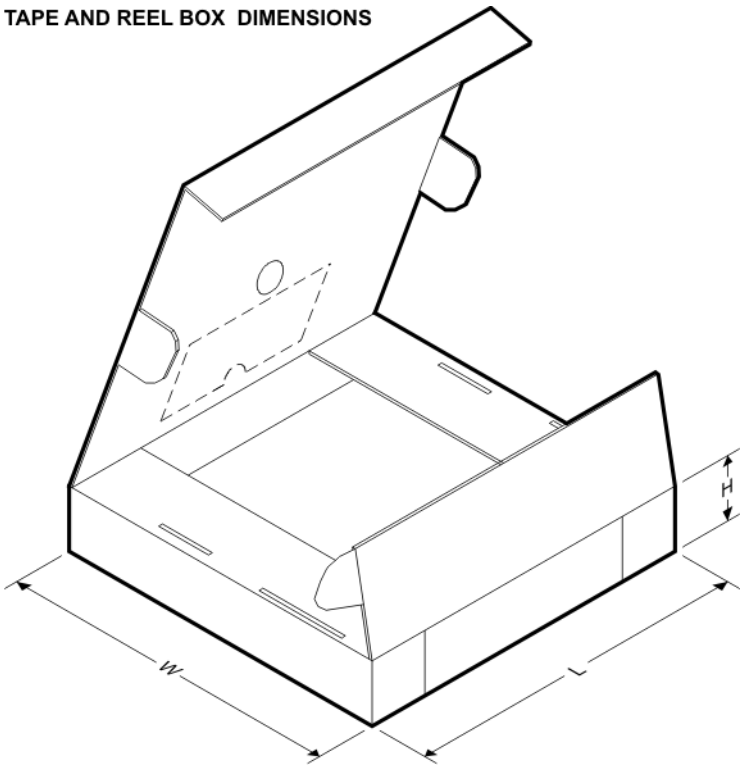
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB1146IRNQR	WQFN	RNQ	40	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TUSB1146IRNQT	WQFN	RNQ	40	250	180.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TUSB1146RNQR	WQFN	RNQ	40	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2
TUSB1146RNQT	WQFN	RNQ	40	250	180.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

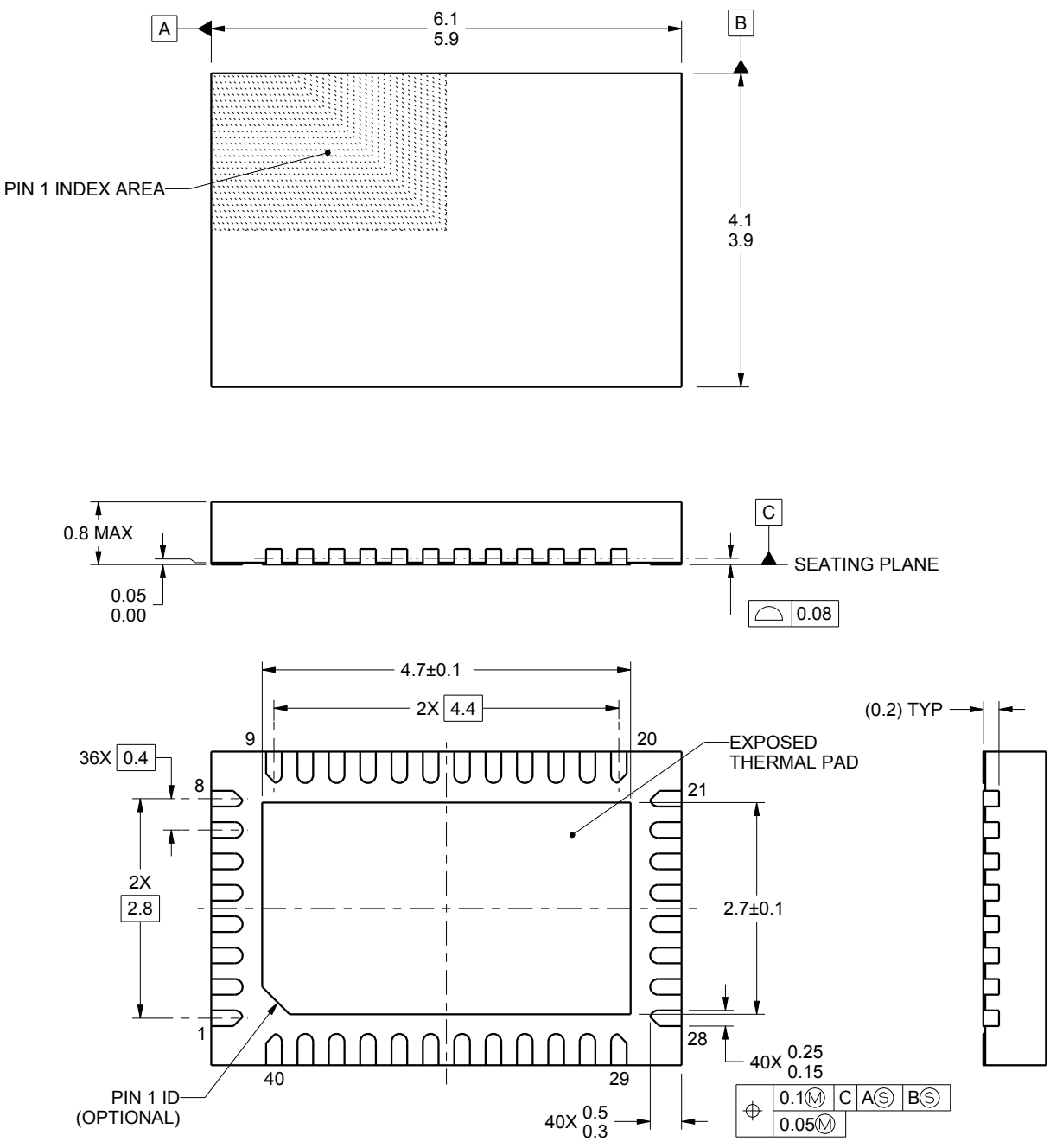
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB1146IRNQR	WQFN	RNQ	40	3000	367.0	367.0	35.0
TUSB1146IRNQT	WQFN	RNQ	40	250	210.0	185.0	35.0
TUSB1146RNQR	WQFN	RNQ	40	3000	367.0	367.0	35.0
TUSB1146RNQT	WQFN	RNQ	40	250	210.0	185.0	35.0

PACKAGE OUTLINE

RNQ0040A

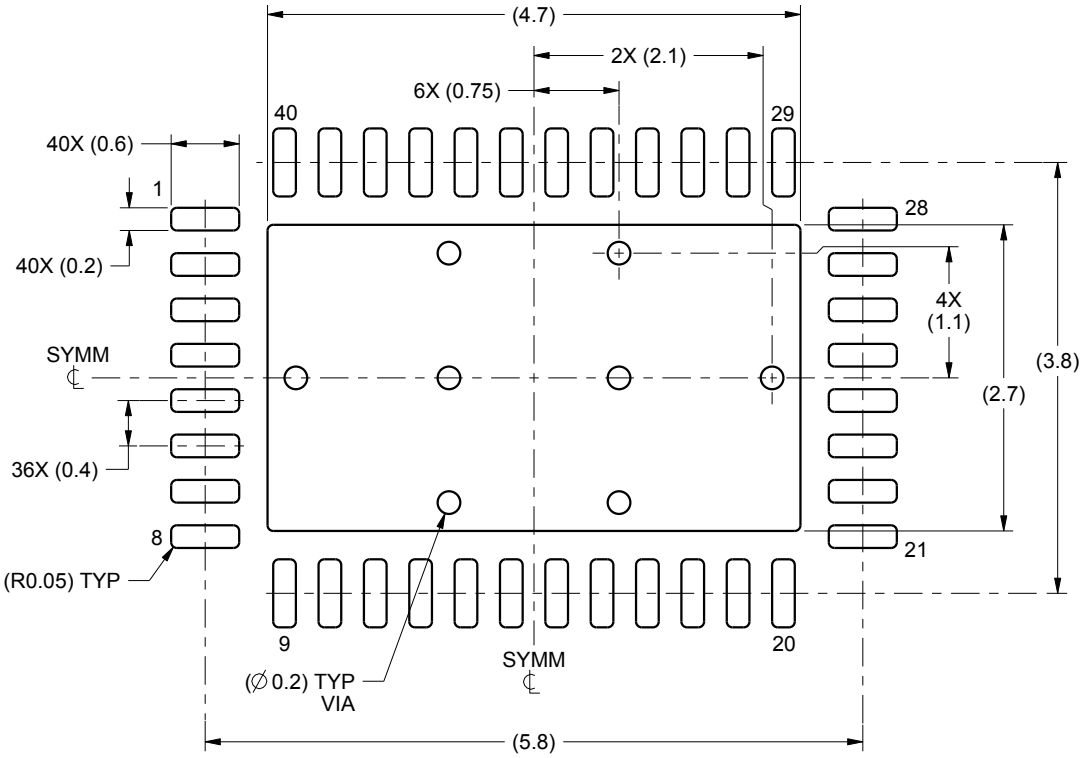
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

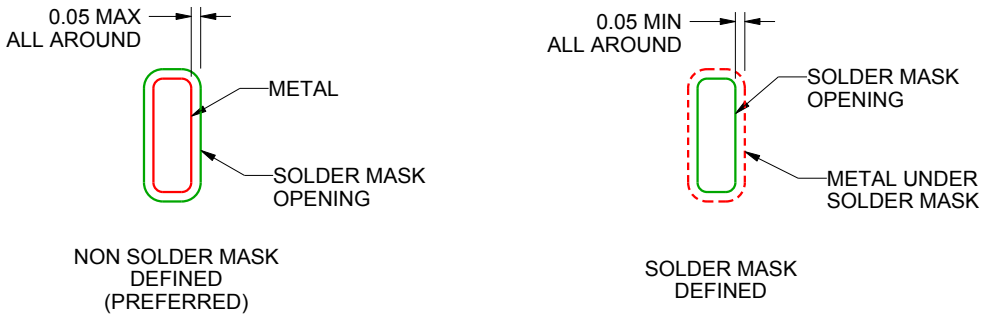


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

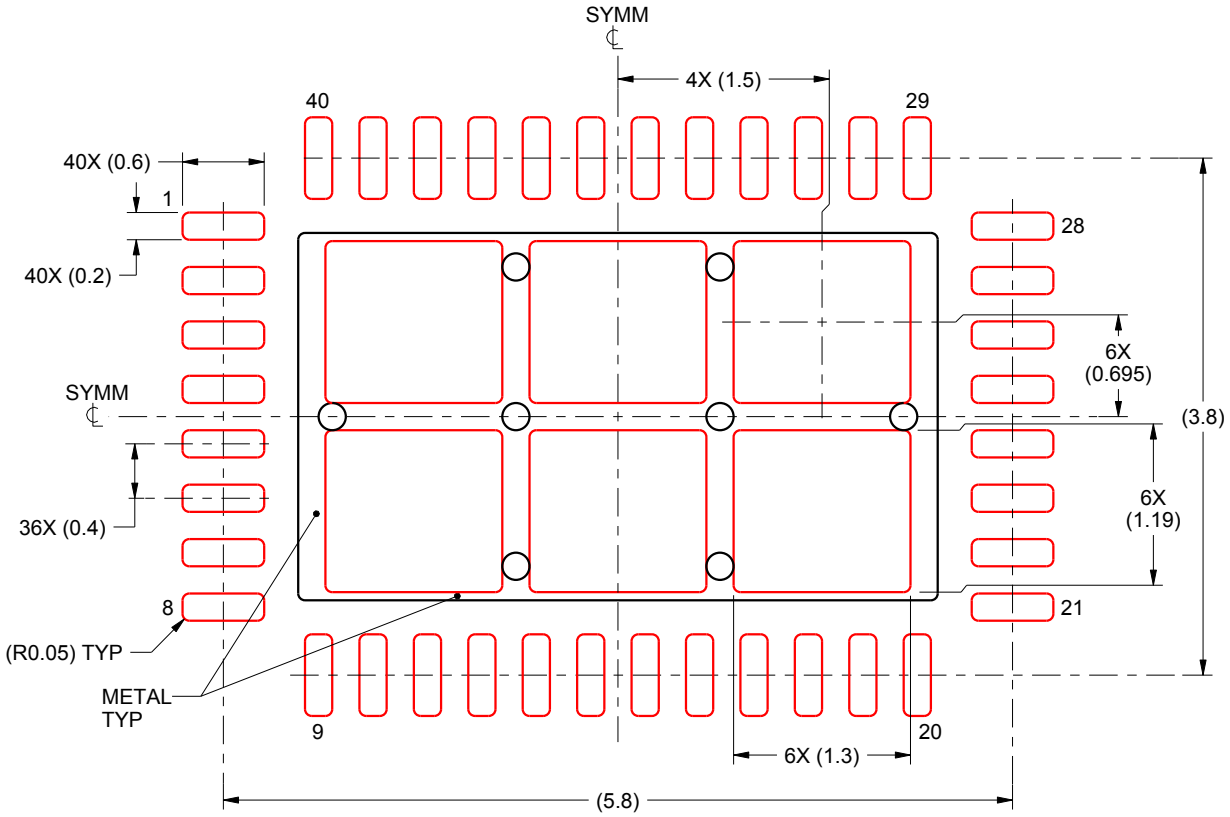


SOLDER MASK DETAILS

4222125/B 01/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
73% PRINTED SOLDER COVERAGE BY AREA
SCALE:18X

4222125/B 01/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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