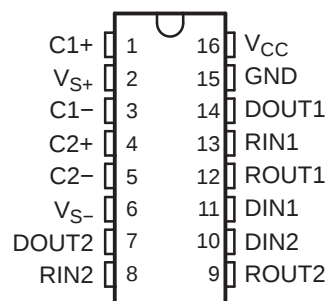


DUAL RS-232 DRIVER/RECEIVER WITH IEC61000-4-2 PROTECTION

FEATURES

- Meets or Exceeds TIA/RS-232-F and ITU Recommendation V.28
- Operates From a Single 5-V Power Supply With 1.0- μ F Charge-Pump Capacitors
- Operates up to 250 kbit/s
- Two Drivers and Two Receivers
- ± 30 -V Input Levels
- Low Supply Current . . . 8 mA Typical
- ESD Protection for RS-232 Bus Pins
 - ± 15 -kV Human-Body Model (HBM)
 - ± 8 -kV IEC61000-4-2, Contact Discharge
 - ± 15 -kV IEC61000-4-2, Air-Gap Discharge

D, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



APPLICATIONS

- TIA/RS-232-F
- Battery-Powered Systems
- Terminals
- Modems
- Computers

DESCRIPTION/ORDERING INFORMATION

The TRS232E is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/RS-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/RS-232-F inputs to 5-V TTL/CMOS levels. This receiver has a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept ± 30 -V inputs. Each driver converts TTL/CMOS input levels into TIA/RS-232-F levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinASIC is a trademark of Texas Instruments.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube of 25	TRS232ECN	TRS232ECN
	SOIC – D	Tube of 40	TRS232ECD	TRS232EC
		Reel of 2500	TRS232ECDR	
	SOIC – DW	Tube of 40	TRS232ECDW	TRS232EC
		Reel of 2000	TRS232ECDWR	
	SOP – NS	Reel of 2000	TRS232ECNSR	PREVIEW
	TSSOP – PW	Tube of 25	TRS232ECPW	RU32EC
		Reel of 2000	TRS232ECPWR	
–40°C to 85°C	PDIP – N	Tube of 25	TRS232EIN	TRS232EIN
	SOIC – D	Tube of 40	TRS232EID	TRS232EI
		Reel of 2500	TRS232EIDR	
	SOIC – DW	Tube of 40	TRS232EIDW	TRS232EI
		Reel of 2000	TRS232EIDWR	
	SOP – NS	Reel of 2000	TRS232EINSR	PREVIEW
	TSSOP – PW	Tube of 25	TRS232EIPW	RU32EI
		Reel of 2000	TRS232EIPWR	

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLES

Each Driver⁽¹⁾

INPUT DIN	OUTPUT DOUT
L	H
H	L

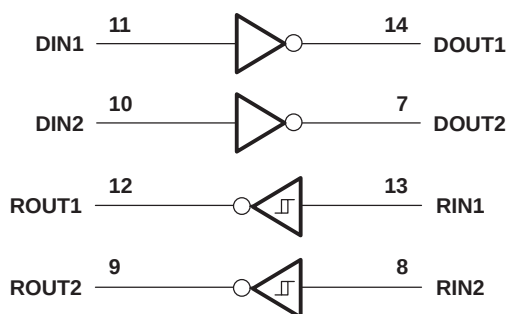
(1) H = high level, L = low level

Each Receiver⁽¹⁾

INPUT RIN	OUTPUT ROUT
L	H
H	L

(1) H = high level, L = low level

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Input supply voltage range ⁽²⁾		–0.3	6	V
V _{S+}	Positive output supply voltage range		V _{CC} – 0.3	15	V
V _{S–}	Negative output supply voltage range		–0.3	–15	V
V _I	Input voltage range	Driver	–0.3	V _{CC} + 0.3	V
		Receiver		±30	
V _O	Output voltage range	DOUT	V _{S–} – 0.3	V _{S+} + 0.3	V
		ROUT	–0.3	V _{CC} + 0.3	
	Short-circuit duration	DOUT		Unlimited	
θ _{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾	D package		73	°C/W
		DW package		57	
		N package		67	
		NS package		64	
		PW package		108	
T _J	Operating virtual junction temperature			150	°C
T _{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.
- (3) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_J(max) – T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.5	5	5.5	V
V _{IH}	High-level input voltage (DIN1, DIN2)		2			V
V _{IL}	Low-level input voltage (DIN1, DIN2)				0.8	V
	Receiver input voltage (RIN1, RIN2)				±30	V
T _A	Operating free-air temperature	TRS232EC	0		70	°C
		TRS232EI	–40		85	

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 4](#))

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
I _{CC} Supply current	V _{CC} = 5.5 V, All outputs open, T _A = 25°C		8	10	mA

- (1) Test conditions are C1–C4 = 1 μF at V_{CC} = 5 V ± 0.5 V.
- (2) All typical values are at V_{CC} = 5 V and T_A = 25°C.

DRIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER			TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	DOUT	R _L = 3 kΩ to GND	5	7		V
V _{OL}	Low-level output voltage ⁽³⁾	DOUT	R _L = 3 kΩ to GND		–7	–5	V
r _o	Output resistance	DOUT	V _{S+} = V _{S–} = 0, V _O = ±2 V	300			Ω
I _{OS} ⁽⁴⁾	Short-circuit output current	DOUT	V _{CC} = 5.5 V, V _O = 0		±10		mA
I _{IS}	Short-circuit input current	DIN	V _I = 0			200	μA

(1) Test conditions are C1–C4 = 1 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.

(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

(4) Not more than one output should be shorted at a time.

Switching Characteristics⁽¹⁾

V_{CC} = 5 V, T_A = 25°C (see Note 4)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Driver slew rate		R _L = 3 kΩ to 7 kΩ, See Figure 2			30	V/μs
SR(t)	Driver transition region slew rate		See Figure 3		3		V/μs
	Data rate		One DOUT switching		250		kbit/s

(1) Test conditions are C1–C4 = 1 μF at V_{CC} = 5 V ± 0.5 V.

ESD protection

PARAMETER	TEST CONDITIONS	TYP	UNIT
DOUT, RIN	HBM	±15	kV
	IEC61000-4-2, Air-Gap Discharge	±15	kV
	IEC61000-4-2, Contact Discharge	±8	kV

RECEIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER			TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	ROUT	I _{OH} = –1 mA	3.5			V
V _{OL}	Low-level output voltage ⁽³⁾	ROUT	I _{OL} = 3.2 mA			0.4	V
V _{IT+}	Receiver positive-going input threshold voltage	RIN	V _{CC} = 5 V, T _A = 25°C		1.7	2.4	V
V _{IT–}	Receiver negative-going input threshold voltage	RIN	V _{CC} = 5 V, T _A = 25°C	0.8	1.2		V
V _{hys}	Input hysteresis voltage	RIN	V _{CC} = 5 V	0.2	0.5	1	V
r _i	Receiver input resistance	RIN	V _{CC} = 5 V, T _A = 25°C	3	5	7	kΩ

(1) Test conditions are C1–C4 = 1 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.

(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

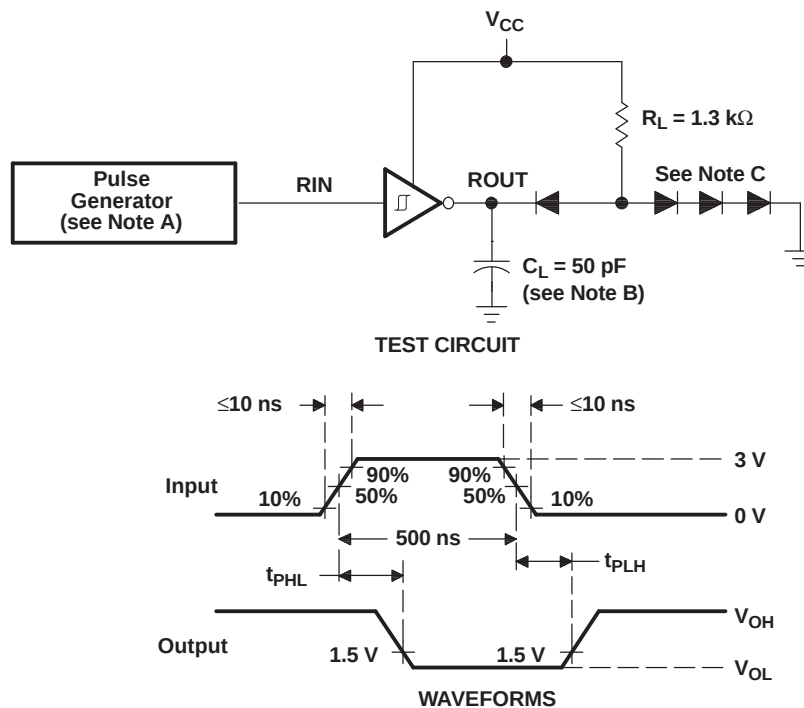
Switching Characteristics⁽¹⁾

V_{CC} = 5 V, T_A = 25°C (see [Figure 1](#))

PARAMETER		TYP	UNIT
t _{PLH(R)}	Receiver propagation delay time, low- to high-level output	500	ns
t _{PHL(R)}	Receiver propagation delay time, high- to low-level output	500	ns

(1) Test conditions are C1–C4 = 1 μF at V_{CC} = 5 V ± 0.5 V.

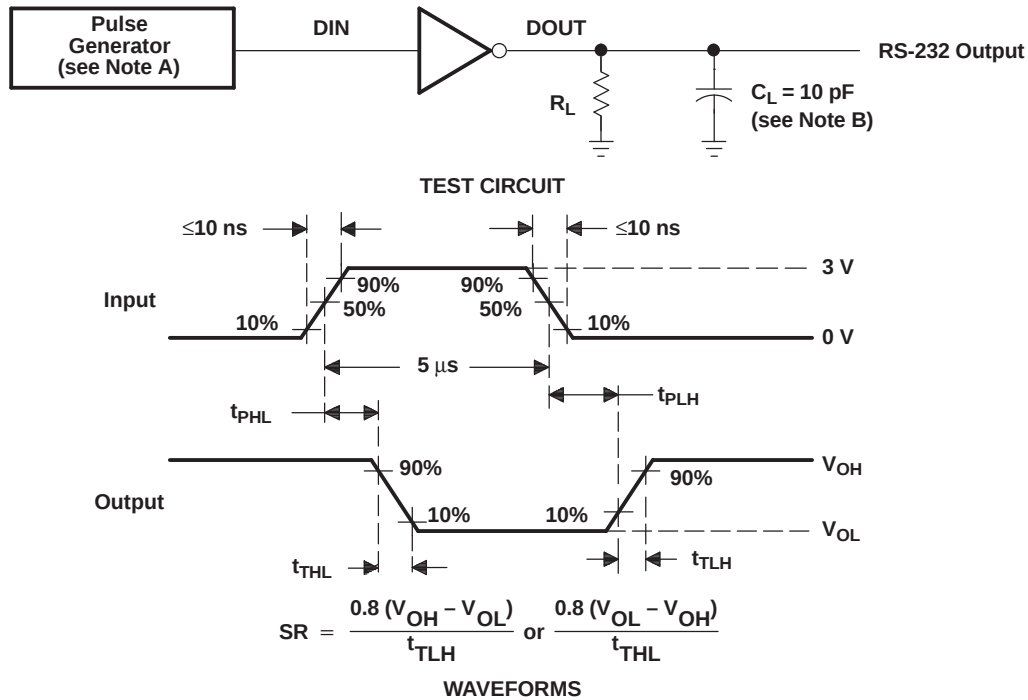
PARAMETER MEASUREMENT INFORMATION



- A. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, duty cycle $\leq 50\%$.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.

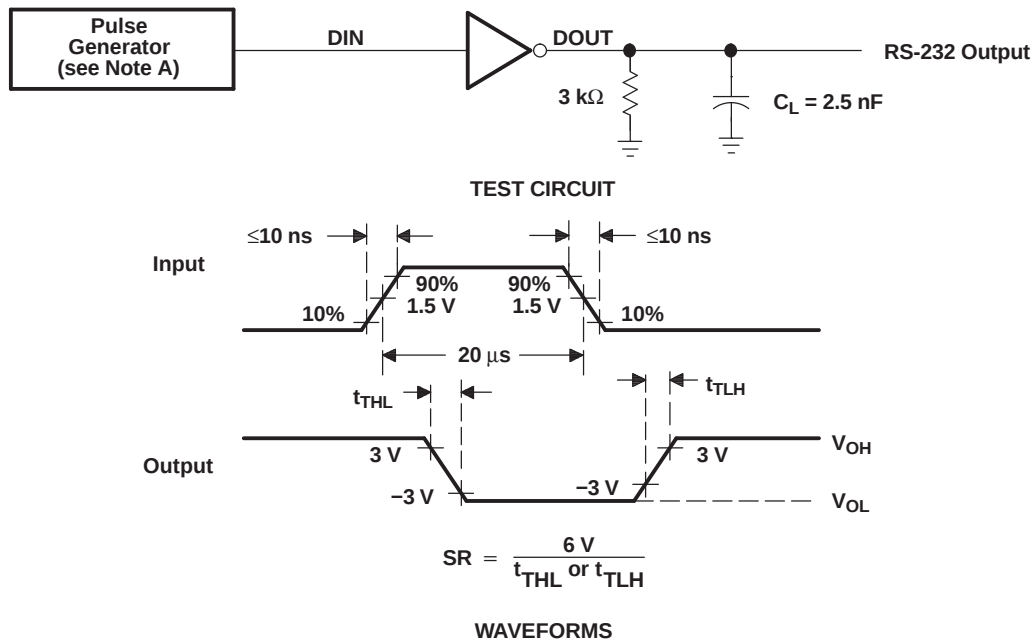
Figure 1. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements

PARAMETER MEASUREMENT INFORMATION (continued)



- A. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, duty cycle $\leq 50\%$.
- B. C_L includes probe and jig capacitance.

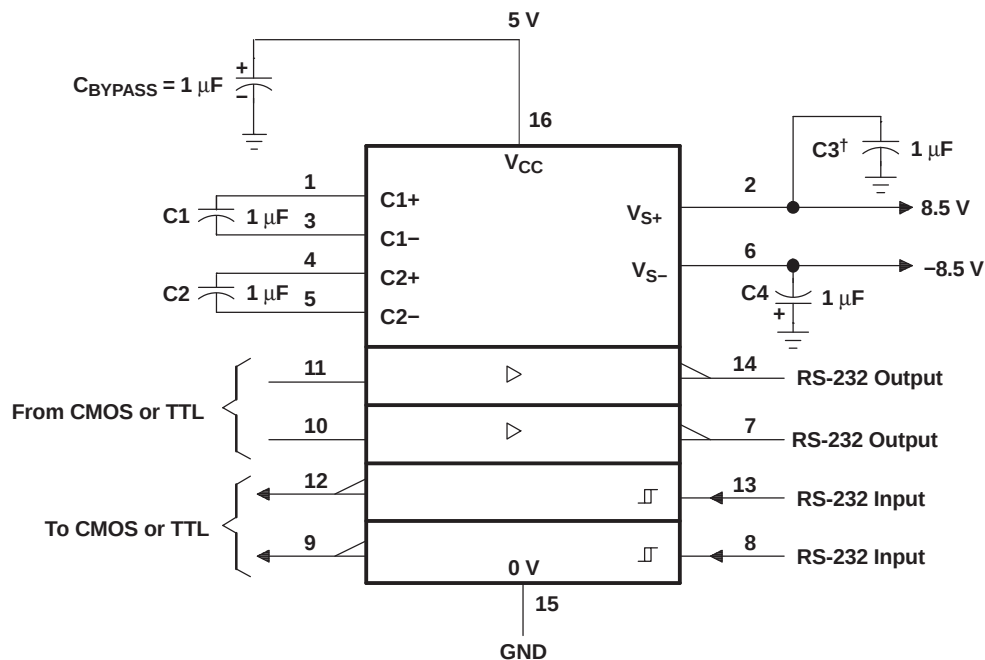
Figure 2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5- μs Input)



- A. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, duty cycle $\leq 50\%$.

Figure 3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20- μs Input)

APPLICATION INFORMATION



[†] C3 can be connected to V_{CC} or GND.

- A. Resistor values shown are nominal.
- B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown. In addition to the 1-μF capacitors shown, the TRS202E can operate with 0.1-μF capacitors.

Figure 4. Typical Operating Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS232ECD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS232EC	Samples
TRS232ECDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS232EC	Samples
TRS232ECDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS232EC	Samples
TRS232ECN	ACTIVE	PDIP	N	16	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	TRS232ECN	Samples
TRS232ECPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	RU32EC	Samples
TRS232ECPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	RU32EC	Samples
TRS232EID	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS232EI	Samples
TRS232EIDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS232EI	Samples
TRS232EIDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS232EI	Samples
TRS232EIN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TRS232EIN	Samples
TRS232EIPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RU32EI	Samples
TRS232EIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RU32EI	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

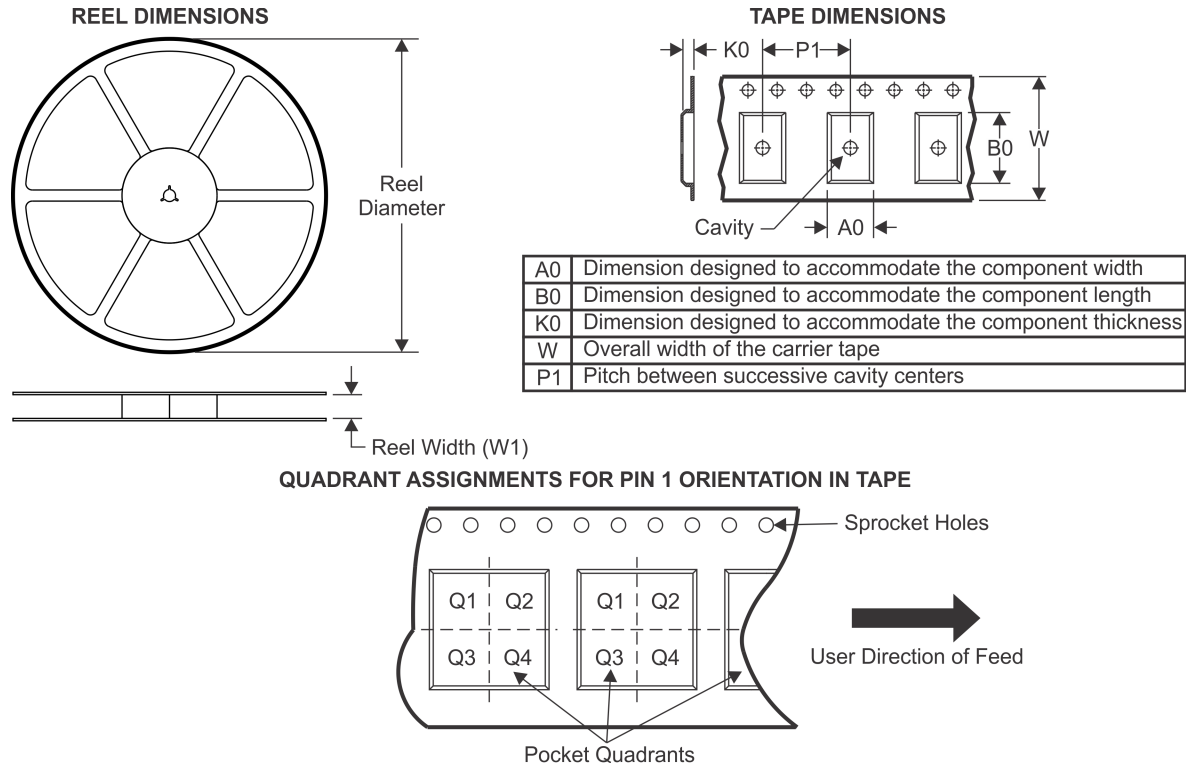
⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

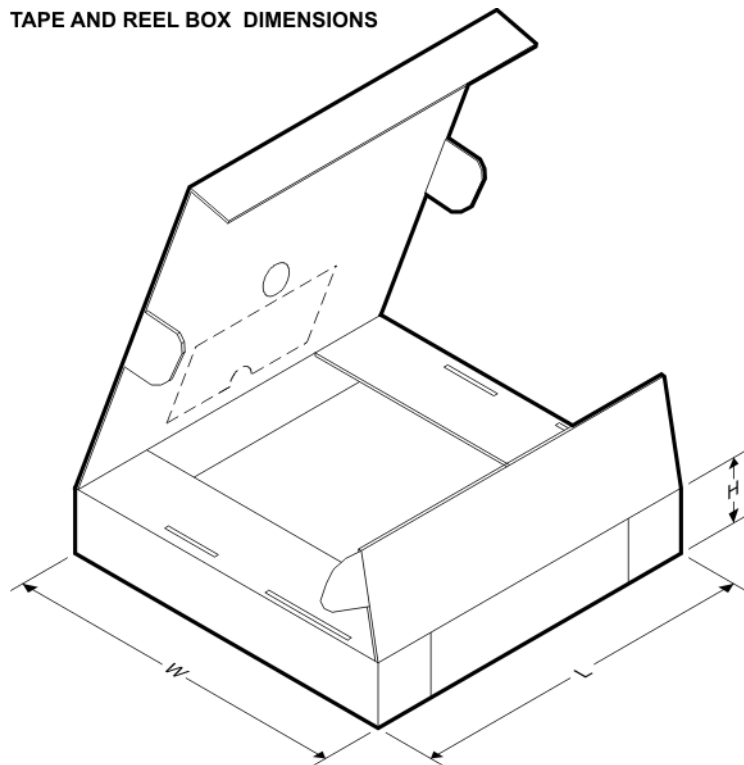
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS232ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS232ECDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS232ECDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRS232ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRS232EIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TRS232EIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TRS232EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

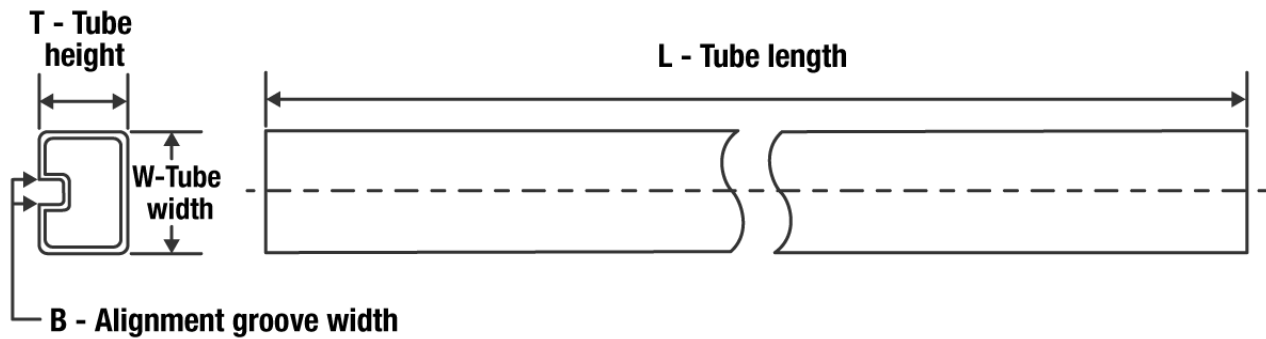
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS232ECDR	SOIC	D	16	2500	340.5	336.1	32.0
TRS232ECDR	SOIC	D	16	2500	853.0	449.0	35.0
TRS232ECDWR	SOIC	DW	16	2000	350.0	350.0	43.0
TRS232ECPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TRS232EIDR	SOIC	D	16	2500	853.0	449.0	35.0
TRS232EIDWR	SOIC	DW	16	2000	350.0	350.0	43.0
TRS232EIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

TUBE

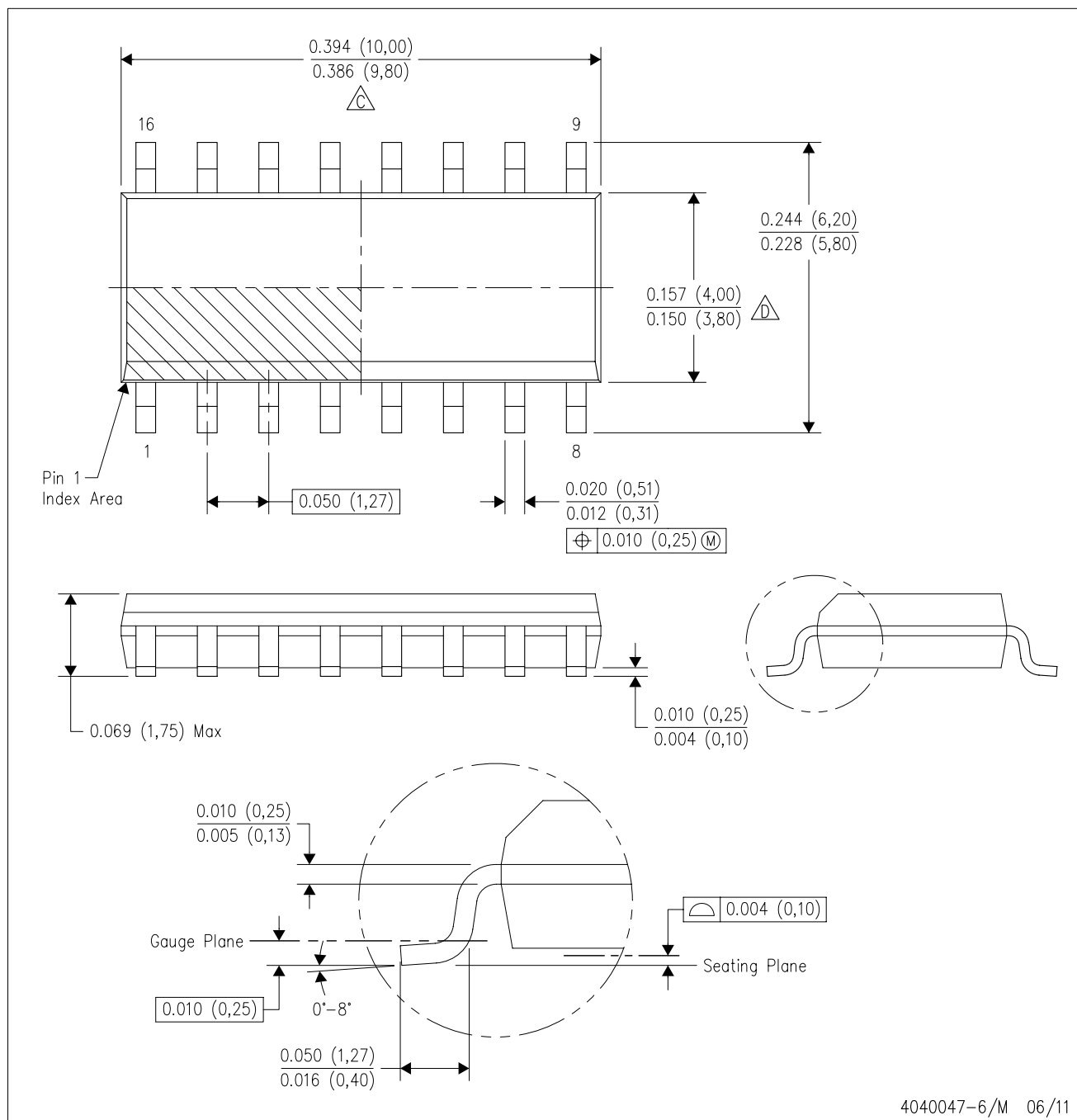


*All dimensions are nominal

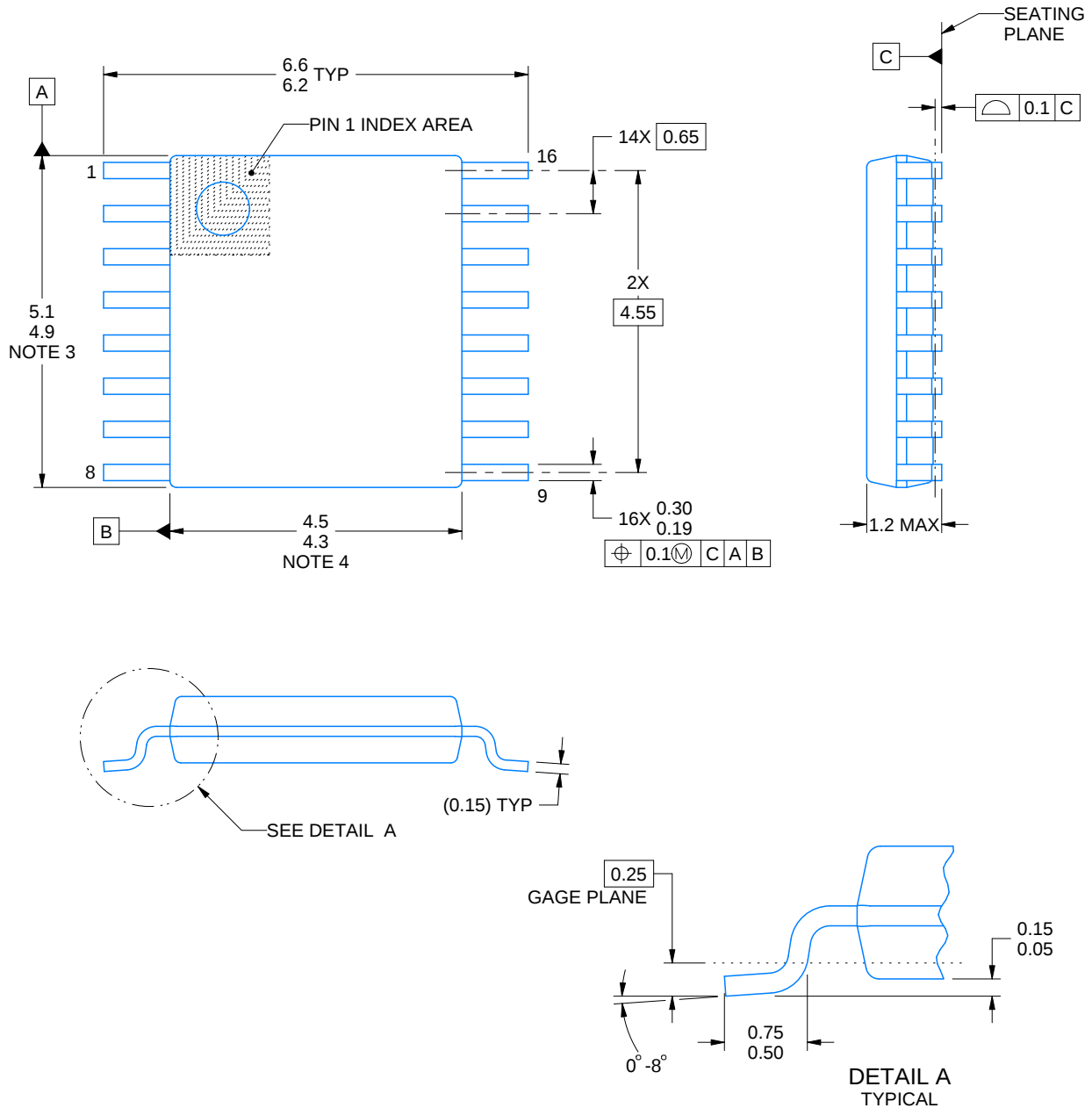
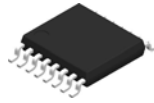
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TRS232ECD	D	SOIC	16	40	506.6	8	3940	4.32
TRS232ECN	N	PDIP	16	25	506	13.97	11230	4.32
TRS232ECPW	PW	TSSOP	16	90	530	10.2	3600	3.5
TRS232EID	D	SOIC	16	40	506.6	8	3940	4.32
TRS232EIN	N	PDIP	16	25	506	13.97	11230	4.32
TRS232EIN	N	PDIP	16	25	506	13.97	11230	4.32
TRS232EIPW	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

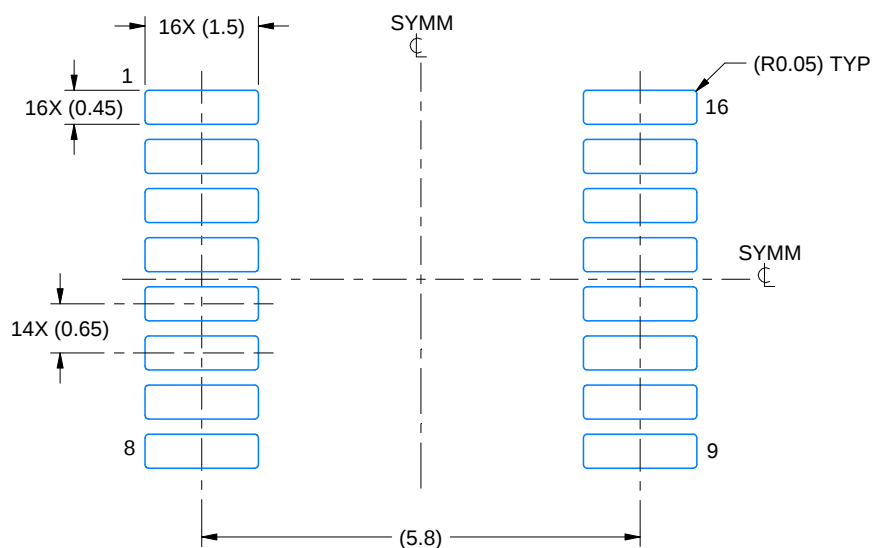
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

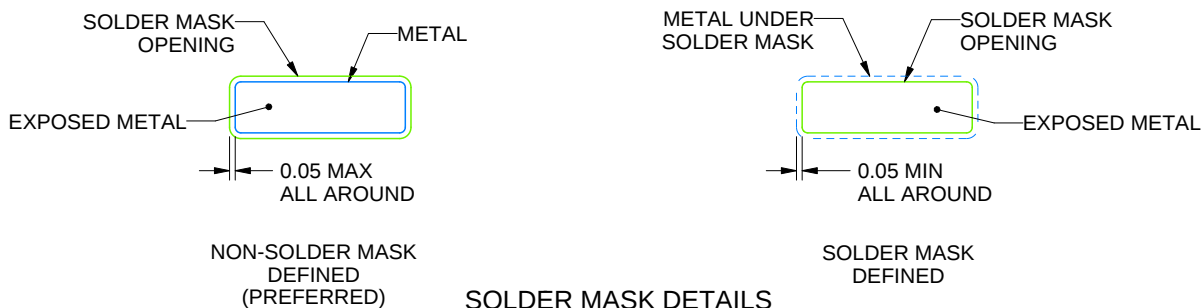
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

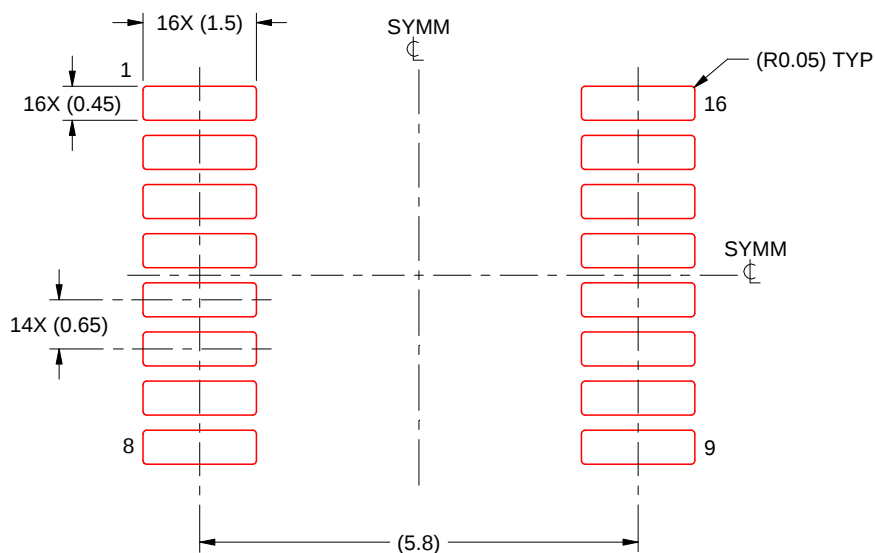
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

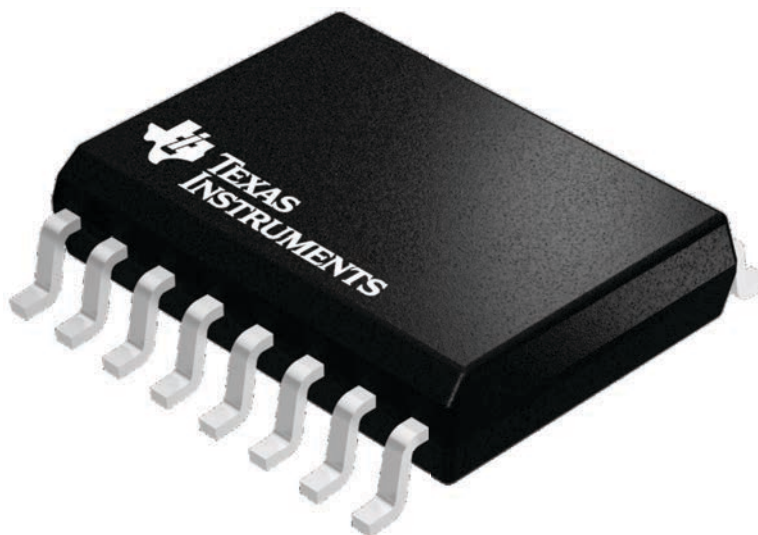
DW 16

SOIC - 2.65 mm max height

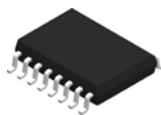
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

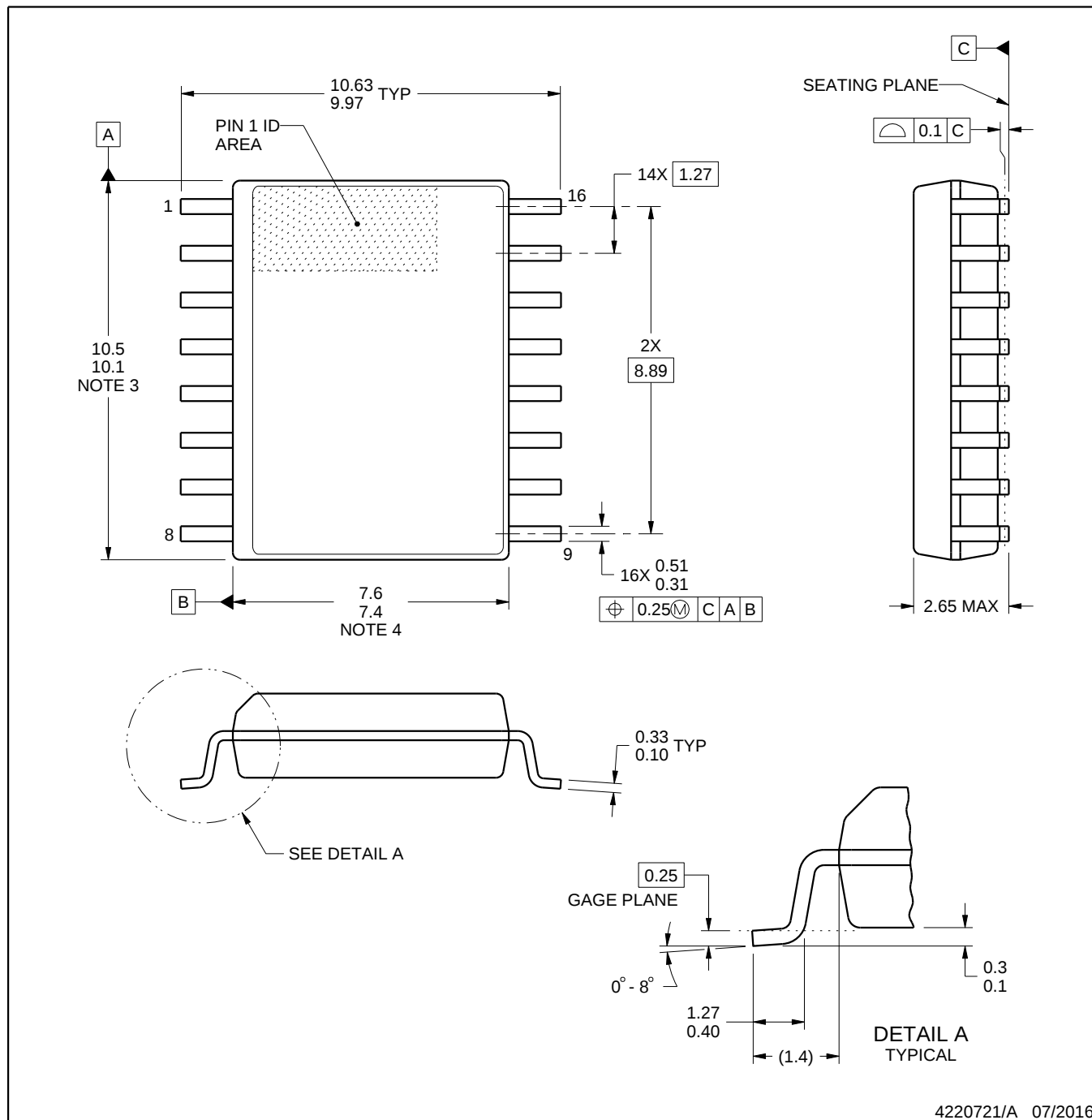


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

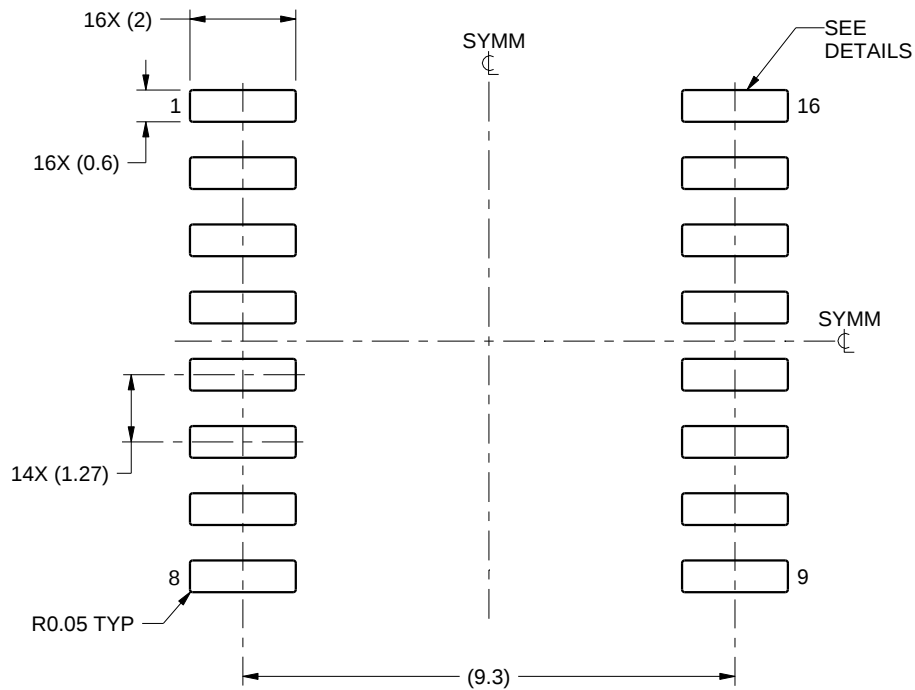
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

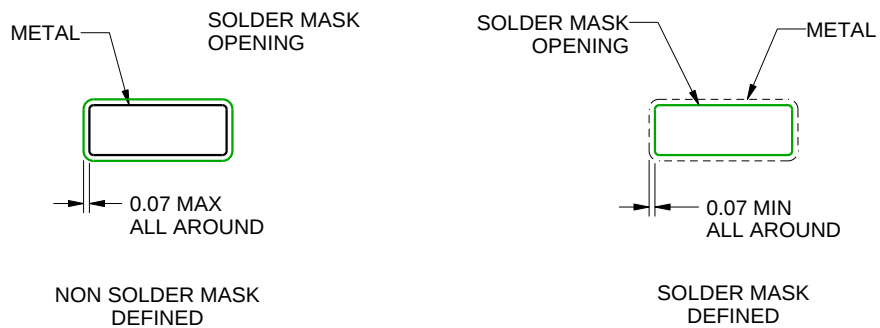
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

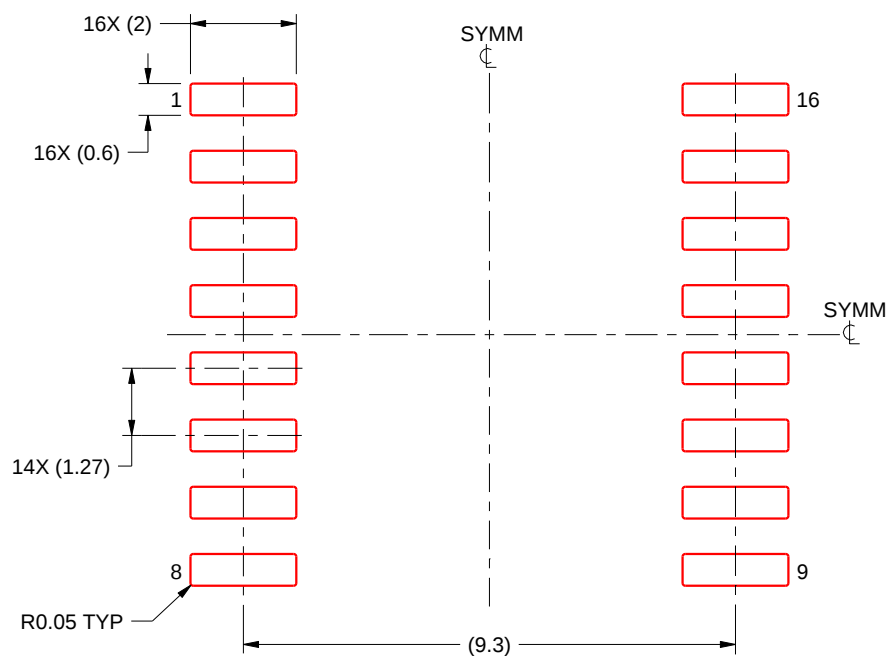
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

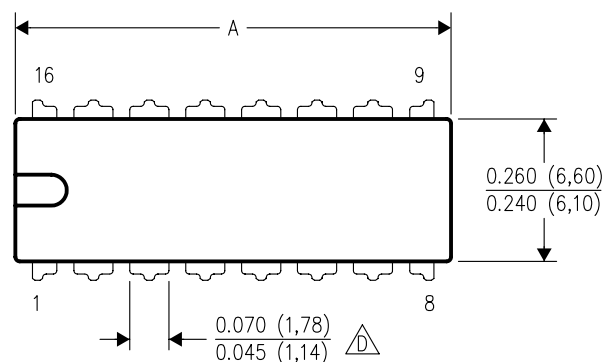
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

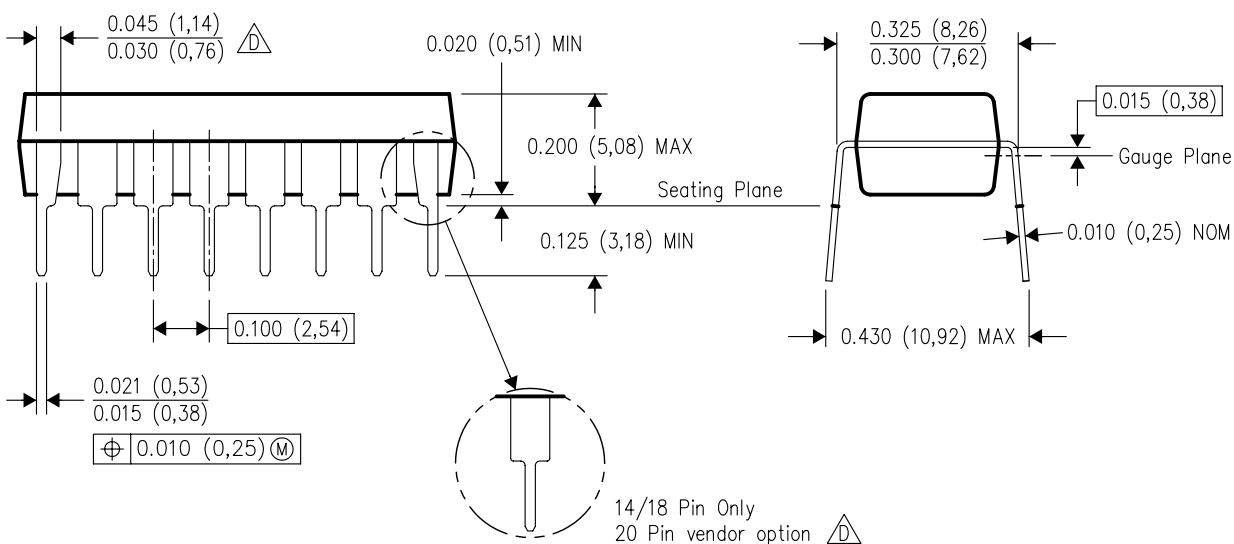
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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