Unitrode Products from Texas Instruments

application INFO available

UCC15701/2
UCC25701/2
UCC35701/2

Advanced Voltage Mode Pulse Width Modulator

FEATURES

- 700kHz Operation
- Integrated Oscillator/ Voltage Feed Forward Compensation
- Accurate Duty Cycle Limit
- Accurate Volt-second Clamp
- Optocoupler Interface
- Fault Counting Shutdown
- Fault Latch off or Automatic Shutdown
- Soft Stop Optimized for Synchronous Rectification
- 1A Peak Gate Drive Output
- 130μA Start-up Current
- 750μA Operating Current

DESCRIPTION

The UCC35701/UCC35702 family of pulse width modulators is intended for isolated switching power supplies using primary side control. They can be used for both off-line applications and DC/DC converter designs such as in a distributed power system architecture or as a telecom power source.

The devices feature low startup current, allowing for efficient off-line starting, yet have sufficient output drive to switch power MOSFETs in excess of 500kHz.

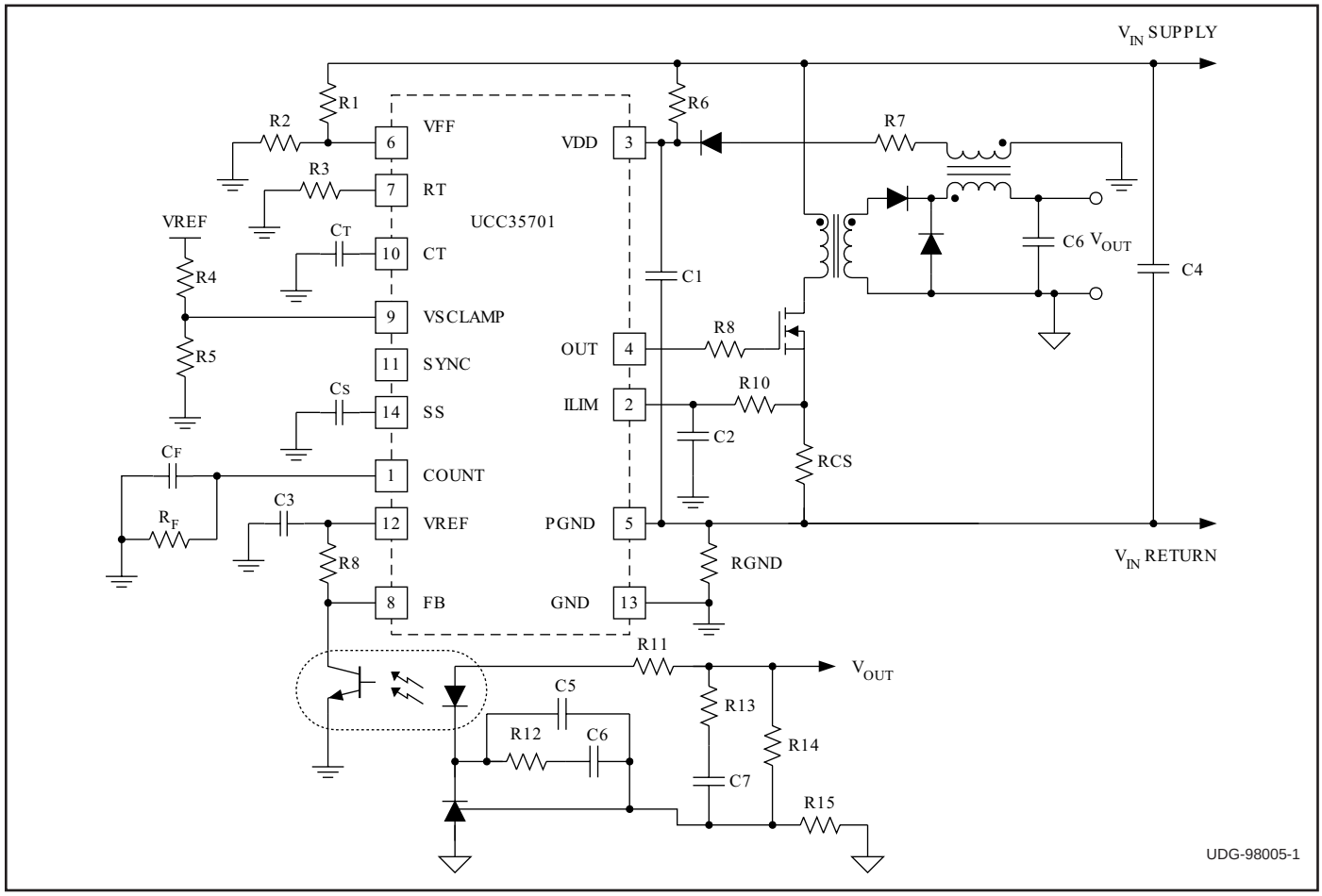
Voltage feed forward compensation is operational over a 5:1 input range and provides fast and accurate response to input voltage changes over a 4:1 range. An accurate volt-second clamp and maximum duty cycle limit are also featured.

Fault protection is provided by pulse by pulse current limiting as well as the ability to latch off after a programmable number of repetitive faults has occurred.

Two UVLO options are offered. UCC35701 family has turn-on and turn-off thresholds of 13V/9V and UCC35702 family has thresholds of 9.6V/8.8V.

The UCC35701/2 and the UCC25701/2 are offered in the 14 pin SOIC (D), 14 pin PDIP (N) or in 14 pin TSSOP (PW) packages. The UCC15701/2 is offered in the 14 pin CDIP (J) package.

TYPICAL APPLICATION DIAGRAM



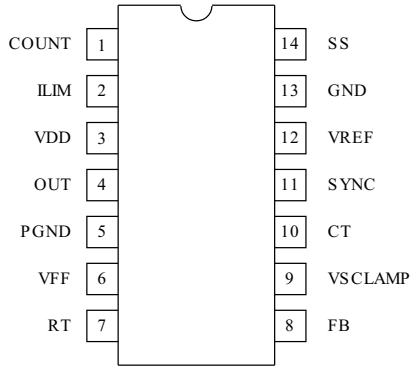
ABSOLUTE MAXIMUM RATINGS

Supply voltage (Supply current limited to 20mA) 15V
Supply Current. 20mA
Input pins (ILIM,VFF,RT,CT,VSCLAMP,SYNC,SS, FB) . . . 6V
Output Current (OUT) DC. . . . . +/–180mA
Output Current (OUT) Pulse (0.5ms) . . . . . +/–1.2A
Storage Temperature. . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Note: All voltages are with respect to GND. Currents are positive into the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-14, SOIC-14, TSSOP-14 (TOP VIEW)
N or J, D, PW PACKAGE



ORDERING INFORMATION

$T_A = T_J$	UVLO Option	Package	Part Number
–55°C to +125°C	13V / 9V	CDIP-14	UCC15701J
	9.6V / 8.8V	CDIP-14	UCC15702J
–40°C to +85°C	13V / 9V	SOIC-14	UCC25701D
		PDIP-14	UCC25701N
		TSSOP-14	UCC25701PW
	9.6V / 8.8V	SOIC-14	UCC25702D
		PDIP-14	UCC25702N
		TSSOP-14	UCC25702PW
0°C to +70°C	13V / 9V	SOIC-14	UCC35701D
		PDIP-14	UCC35701N
		TSSOP-14	UCC35701PW
	9.6V / 8.8V	SOIC-14	UCC35702D
		PDIP-14	UCC35702N
		TSSOP-14	UCC35702PW

The D and PW packages are available taped and reeled. Add TR suffix to the device type (e.g., UCC35701DTR).

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, V_{DD} = 11V, RT = 60.4k, C_T = 330pF, C_{REF} = C_{VDD} = 0.1 F, V_{FF} = 2.0V, and no load on the outputs.

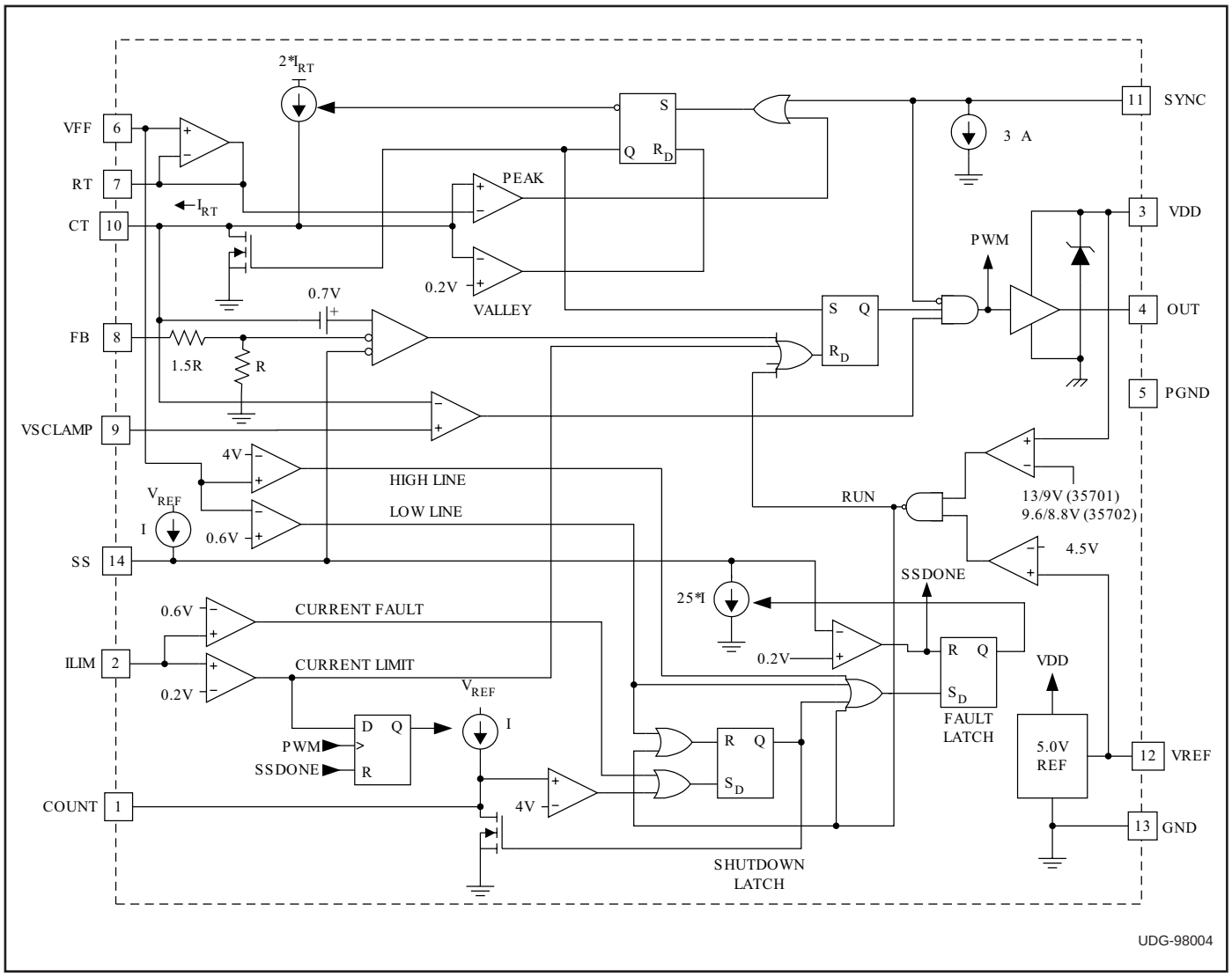
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Section					
Start Threshold	(UCCX5701)	12	13	14	V
	(UCCX5702)	8.8	9.6	10.4	V
Stop Threshold	(UCCX5701)	8	9	10	V
	(UCCX5702)	8.0	8.8	9.6	V
Hysteresis	(UCCX5701)	3	4		V
	(UCCX5702)	0.3	0.8		V
Supply Current					
Start-up Current	(UCCX5701) V_{DD} = 11V, V_{DD} Comparator Off		130	200	µA
	(UCCX5702) V_{DD} = 8V, V_{DD} Comparator Off		120	190	µA
I_{DD} Active	V_{DD} Comparator On		0.75	1.5	mA
V_{DD} Clamp Voltage	(UCCX5701) I_{DD} = 10mA	13.5	14.3	15	V
	(UCCX5702) I_{DD} = 10mA	13	13.8	15	V
V_{DD} Clamp – Start Threshold	(UCCX5701)		1.3		V
	(UCCX5702)		4.2		V
Voltage Reference					
V_{REF}	V_{DD} = 10V to 13V, I_{VREF} = 0mA to 2mA	4.9	5	5.1	V
Line Regulation	V_{DD} = 10V to 13V		20		mV
Load Regulation	I_{VREF} = 0mA to 2mA		2		mV
Short Circuit Current	V_{REF} = 0V, T_J = 25°C		20	50	mA

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, V_{DD} = 11V, RT = 60.4k, C_T = 330pF, C_{REF} = C_{VDD} = 0.1 F, V_{FF} = 2.0V, and no load on the outputs.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Line Sense					
Vth High Line Comparator		3.9	4	4.1	V
Vth Low Line Comparator		0.5	0.6	0.7	V
Input Bias Current		–100		100	nA
Oscillator Section					
Frequency	V_{FF} = 0.8V to 3.2V	90	100	110	kHz
Frequency	V_{FF} = 0.6V to 3.4V (Note 1)	90	100	110	kHz
SYNC VIH		2			V
SYNC VIL				0.8	V
SYNC Input Current	VSYNC = 2.0V		3	10	μA
RT Voltage	VFF = 0.4V	0.5	0.6	0.7	V
	VFF = 0.8V	0.75	0.8	0.85	V
	VFF = 2.0V	1.95	2.0	2.05	V
	VFF = 3.2V	3.15	3.2	3.25	V
	VFF = 3.6V	3.3	3.4	3.5	V
C_T Peak Voltage	VFF = 0.8V (Note 1)		0.8		V
	VFF = 3.2V (Note 1)		3.2		V
C_T Valley Voltage	(Note 1)		0		V
Soft Start/Shutdown/Duty Cycle Control Section					
I_{SS} Charging Current		10	18	30	μA
I_{SS} Discharging Current		300	500	750	μA
Saturation	V_{DD} = 11V, IC Off		25	100	mV
Fault Counter Section					
Threshold Voltage	VFF = 0.8V to 3.2V	3.8	4	4.2	V
Saturation Voltage	VFF = 0.8V to 3.2V			100	mV
Count Charging Current		10	18	30	μA
Current Limit Section					
Input Bias Current		–100	0	100	nA
Current Limit Threshold		180	200	220	mV
Shutdown Threshold		500	600	700	mV
Pulse Width Modulator Section					
FB Pin Input Impedance	VFB = 3V	30	50	100	kΩ
Minimum Duty Cycle	VFB <= 1V			0	%
Maximum Duty Cycle	VFB >= 4.5V, VSCLAMP >= 2.0V	95	99	100	%
PWM Gain	VFF = 0.8V	35	50	70	%/V
Volt Second Clamp Section					
Maximum Duty Cycle	VFF = 0.8V, VSCLAMP = 0.6V	69	74	79	%
Minimum Duty Cycle	VFF = 3.2V, VSCLAMP = 0.6V	17	19	21	%
Output Section					
VOH	I_{OUT} = –100mA, (V_{DD} – V_{OUT})		0.4	1	V
VOL	I_{OUT} = 100mA		0.4	1	V
Rise Time	C_{LOAD} = 1000pF		20	100	ns
Fall Time	C_{LOAD} = 1000pF		20	100	ns

Note 1: Ensured by design. Not 100% tested in production.

DETAILED BLOCK DIAGRAM



PIN DESCRIPTIONS

VDD: Power supply pin. A shunt regulator limits supply voltage to 14V typical at 10mA shunt current.

PGND: Power Ground. Ground return for output driver and currents.

GND: Analog Ground. Ground return for all other circuits. This pin must be connected directly to PGND on the board.

OUT: Gate drive output. Output resistance is 10Ω maximum.

VFF: Voltage feedforward pin. This pin connects to the power supply input voltage through a resistive divider and provides feedforward compensation over a 0.8V to 3.2V range. A voltage greater than 4.0V or less than 0.6V on this pin initiates a soft stop cycle.

RT: The voltage on this pin mirrors VFF over a 0.8V to 3.2V range. A resistor to ground sets the ramp capacitor charge current. The resistor value should be between 20k and 200k.

CT: A capacitor to ground provides the oscillator/ feedforward sawtooth waveform. Charge current is 2 • I_{RT}, resulting in a CT slope proportional to the input voltage. The ramp voltage range is GND to V_{RT}.

Period and oscillator frequency is given by:

$$T = \frac{V_{RT} \bullet C_T}{2 \bullet I_{RT}} + t_{DISCH} \approx 0.5 \bullet R_T \bullet C_T$$

$$F \approx \frac{2}{RT \bullet CT}$$

PIN DESCRIPTIONS (cont.)

VSCLAMP: Voltage at this pin is compared to the CT voltage, providing a constant volt-second limit. The comparator output terminates the PWM pulse when the ramp voltage exceeds VSCLAMP. The maximum on time is given by:

$$t_{ON} = \frac{V_{VSCLAMP} \bullet CT}{2 \bullet I_{RT}}$$

The maximum duty cycle limit is given by:

$$D_{MAX} = \frac{t_{ON}}{T} = \frac{V_{VSCLAMP}}{V_{RT}}$$

FB: Input to the PWM comparator. This pin is intended to be driven with an optocoupler circuit. Input impedance is 50kΩ Typical modulation range is 1.6V to 3.6V.

SYNC: Level sensitive oscillator sync input. A high level forces the gate drive output low and resets the ramp capacitor. On-time starts at the negative edge the pulse. There is a 3μA pull down current on the pin, allowing it to be disconnected when not used.

VREF: 5.0V trimmed reference with 2% variation over line, load and temperature. Bypass with a minimum of 0.1μF to ground.

SS: Soft Start pin. A capacitor is connected between this pin and ground to set the start up time of the converter. After power up (V_{DD}>13V AND V_{REF}>4.5V), or after a fault condition has been cleared, the soft start capacitor is charged to V_{REF} by a nominal 18μA internal current source. While the soft start capacitor is charging, and while V_{SS} < (0.4 V_{FB}), the duty cycle, and therefore the output voltage of the converter is determined by the soft start circuitry.

At High Line or Low Line fault conditions, the soft start capacitor is discharged with a controlled discharge current of about 500μA. During the discharge time, the duty cycle of the converter is gradually decreased to zero. This soft stop feature allows the synchronous rectifiers to gradually discharge the output LC filter. An abrupt shut off can cause the LC filter to oscillate, producing unpredictable output voltage levels.

All other fault conditions (UVLO, VREF Low, Over Current (0.6V on ILIM) or COUNT) will cause an immediate stop of the converter. Furthermore, both the Over Current fault and the COUNT fault will be internally latched until V_{DD} drops below 9V or V_{FF} goes below the 600mV threshold at the input of the Low Line comparator.

After all fault conditions are cleared and the soft start capacitor is discharged below 200 mV, a soft start cycle will be initiated to restart the converter.

ILIM: Provides a pulse by pulse current limit by terminating the PWM pulse when the input is above 200mV. An input over 600mV initiates a latched soft stop cycle.

COUNT: Capacitor to ground integrates current pulses generated when ILIM exceeds 200mV. A resistor to ground sets the discharge time constant. A voltage over 4V will initiate a latched soft stop cycle.

APPLICATION INFORMATION

(Note: Refer to the Typical Application Diagram on the first page of this datasheet for external component names.) All the equations given below should be considered as first order approximations with final values determined empirically for a specific application.

Power Sequencing

V_{DD} is normally connected through a high impedance (R6) to the input line, with an additional path (R7) to a low voltage bootstrap winding on the power transformer. VFF is connected through a divider (R1/R2) to the input line.

For circuit activation, all of the following conditions are required:

1. VFF between 0.6V and 4.0V (operational input voltage range).

2. VDD has been under the UVLO stop threshold to reset the shutdown latch.

3. VDD is over the UVLO start threshold.

The circuit will start at this point. I_{VDD} will increase from the start up value of 130μA to the run value of 750μA. The capacitor on SS is charged with a 18μA current. When the voltage on SS is greater than 0.8V, output pulses can begin, and supply current will increase to a level determined by the MOSFET gate charge requirements to I_{VDD} ~ 1mA + QT • fs. When the output is active, the bootstrap winding should be sourcing the supply current. If VDD falls below the UVLO stop threshold, the controller will enter a shutdown sequence and turn the controller off, returning the start sequence to the initial condition.

VDD Clamp

An internal shunt regulator clamps VDD so the voltage does not exceed a nominal value of 14V. If the regulator is active, supply current must be limited to less than 20mA.

APPLICATION INFORMATION (cont.)

Output Inhibit

During normal operation, OUT is driven high at the start of a clock period and is driven low by voltages on CT, FB or VSCLAMP.

The following conditions cause the output to be immediately driven low until a clock period starts where none of the conditions are true:

1. $I_{LIM} > 0.2V$

2. FB or SS is less than 0.8V

Current Limiting

ILIM is monitored by two internal comparators. The current limit comparator threshold is 0.2V. If the current limit comparator is triggered, OUT is immediately driven low and held low for the remainder of the clock cycle, providing pulse-by-pulse over-current control for excessive loads. This comparator also causes C_F to be charged for the remainder of the clock cycle.

If repetitive cycles are terminated by the current limit comparator causing COUNT to rise above 4V, the shutdown latch is set. The COUNT integration delay feature will be bypassed by the shutdown comparator which has a 0.6V threshold. The shutdown comparator immediately sets the shutdown latch. R_F in parallel with C_F resets the COUNT integrator following transient faults. R_F must be greater than $(4 \bullet R4) \bullet (1 - D_{MAX})$.

Latched Shutdown

If ILIM rises above 0.6V, or COUNT rises to 4V, the shutdown latch will be set. This will force OUT low, discharge SS and COUNT, and reduce I_{DD} to approximately 750μA. When, and if, V_{DD} falls below the UVLO stop threshold, the shutdown latch will reset and I_{DD} will fall to 130μA, allowing the circuit to restart. If V_{DD} remains above the UVLO stop threshold (within the UVLO band), an alternate restart will occur if VFF is momentarily reduced below 1V. External shutdown commands from any source may be added into either the COUNT or ILIM pins.

Voltage Feedforward

The voltage slope on CT is proportional to line voltage over a 4:1 range and equals 2•VFF (RT•CT). The capacitor charging current is set by the voltage across R_T. V(RT) tracks VFF over a range of 0.8V to 3.2V. A changing line voltage will immediately change the slope of V(CT), changing the pulse width in a proportional manner without using the feedback loop, providing excellent dynamic line regulation.

VFF is intended to operate accurately over a 4:1 range between 0.8V and 3.2V. Voltages at VFF below 0.6V or above 4.0V will initiate a soft stop cycle and a chip restart when the under/over voltage condition is removed.

Volt-Second Clamp

A constant volt-second clamp is formed by comparing the timing capacitor ramp voltage to a fixed voltage derived from the reference. Resistors R4 and R5 set the volt-second limit. For a volt-second product defined as VIN $t_{ON(max)}$, the required voltage at VSCLAMP is:

$$\frac{\left(\frac{R2}{R1+R2}\right) \bullet \left(V_{IN} \bullet t_{ON(\max)}\right)}{R_T \bullet C_T}.$$

The duty cycle limit is then:

$$\frac{V_{VSCLAMP}}{V_{VFF}}, \text{ or } \frac{V_{VSCLAMP}}{V_{IN} \bullet \left(\frac{R2}{R1+R2}\right)}.$$

The maximum duty cycle is realized when the feedforward voltage is set at the low end of the operating range (V_{FF} = 0.8V).

The absolute maximum duty cycle is:

$$D_{MAX} = \frac{V_{VSCLAMP}}{0.8} = \frac{V_{REF}}{0.8} \bullet \frac{R5}{R4+R5}$$

Frequency Set

The frequency is set by a resistor from RT to ground and a capacitor from CT to ground. The frequency is approximately: $F = \frac{2}{(R_T \bullet C_T)}$

External synchronization is via the SYNC pin. The pin has a 1.5V threshold , making it compatible with 5V and 3.3V CMOS logic. The input is level sensitive, with a high input forcing the oscillator ramp low and the output low. An active pull down on the SYNC pin allows it to be unconnected when not used.

Gate Drive Output

The UCC35701/2 is capable of a 1A peak output current. Bypass with at least 0.1μF directly to PGND. The capacitor must have a low equivalent series resistance and inductance. The connection from OUT to the power MOSFET gate should have a 2Ω or greater damping resistor and the distance between chip and MOSFET should be minimized. A low impedance path must be established between the MOSFET source (or ground side of the current sense resistor), the V_{DD} capacitor and PGND. PGND should then be connected by a single path (shown as RGND) to GND.

APPLICATION INFORMATION (cont.)

Transitioning From UCC3570 To UCC35701

The UCC35701/2 is an advanced version of the popular, low power UCC3570 PWM. Significant improvements were made to the IC's oscillator and PWM control sections to enhance overall system performance. All of the key attributes and functional blocks of the UCC3570 were maintained in the UCC35701/2. A typical application using UCC3570 and UCC35701/2 is shown in Fig. 6 for comparison.

The advantages of the UCC35701/2 over the UCC3570 are as follows.

Improved oscillator and PWM control section.

A precise maximum volt-second clamp circuit. The UCC3570 has a dual time base between oscillator and feedforward circuitry. The integated time base in UCC35701/2 improves the duty cycle clamp accuracy, providing better than ± 5% accurate volt- second clamp over full temperature range.

Separately programmable oscillator timing resistor (RT) and capacitor (CT) circuits provide a higher degree of versatility.

An independent SYNC input pin for simple external synchronization.

A smaller value filter capacitor (0.1μF) can be used with the enhanced reference voltage.

UCC35701/2 is pin to pin compatible to UCC3570 but is not a direct drop-in replacement for UCC3570 sockets. The changes required to the power supply printed circuit board of for existing UCC3570 designs are minimal. For conversion, only one extra resistor to set the volt-second clamp needs to be added to the existing PC board layouts. In addition, some component values will need to be changed due to the functionality change in of four of the IC pins.

The Pinout Changes from UCC3570 are as follows.

Pin 7 was changed from SLOPE to RT (for timing resistor)

Pin 8 was changed from ISET to VSCLAMP (requiring one additional resistor from pin 9 to VREF)

Pin 10 was changed from RAMP to CT (single timing capacitor)

Pin 11 was changed from FREQ to SYNC (input only)

Additional Information

Please refer to the following two Unitrode application topics on UCC3570 for additional information.

[1] Application Note U-150, Applying the UCC3570 Voltage-Mode PWM Controller to Both Off-line and DC/DC Converter Designs by Robert A. Mammano

[2] Design Note DN-62, Switching Power Supply Topology, Voltage Mode vs. Current Mode by Robert Mammano

TYPICAL WAVEFORMS

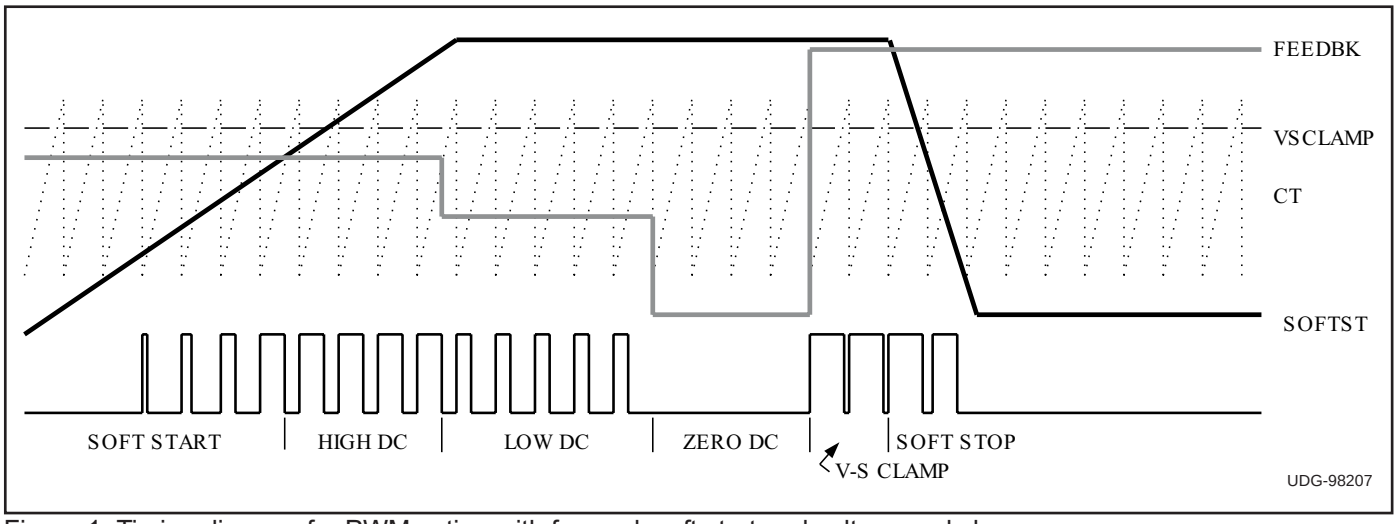


Figure 1. Timing diagram for PWM action with forward, soft start and volt-second clamp.

TYPICAL WAVEFORMS (cont.)

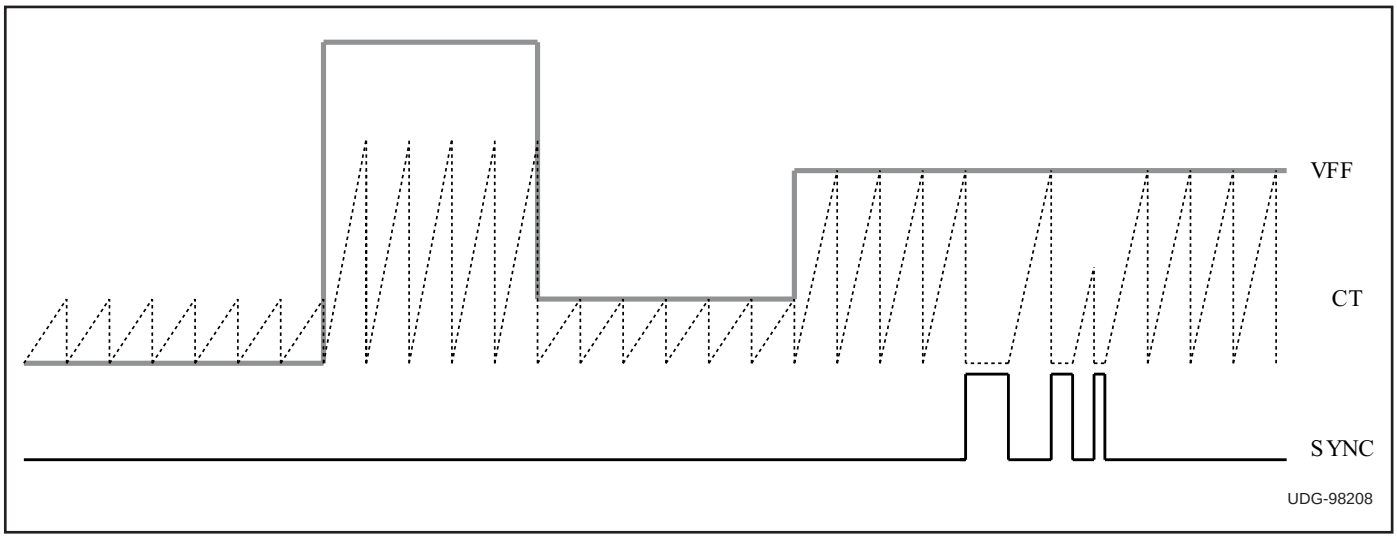


Figure 2. Timing diagram for oscillator waveforms showing feedforward action and synchronization.

TYPICAL CHARACTERISTIC CURVES

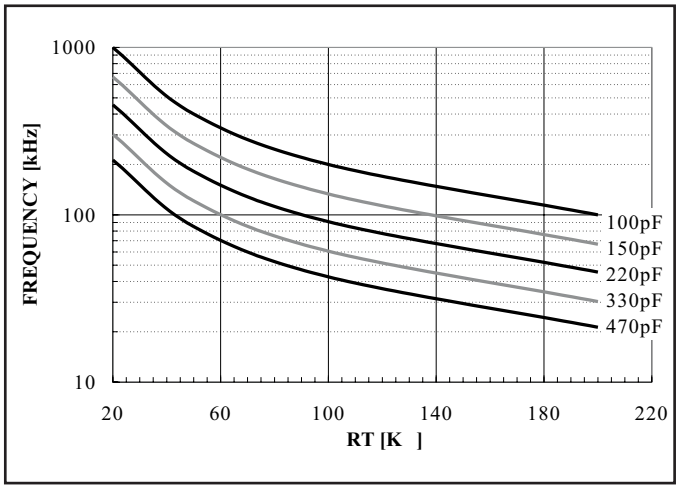


Figure 3. Oscillator frequency vs. RT and CT.

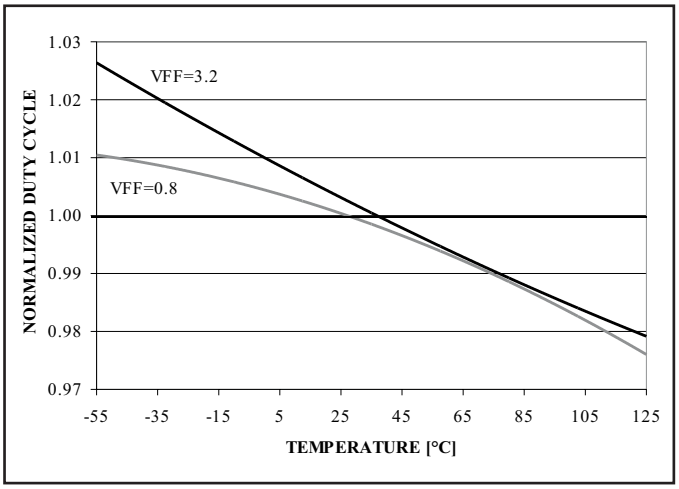


Figure 5. Normalized maximum duty cycle vs. temperature.

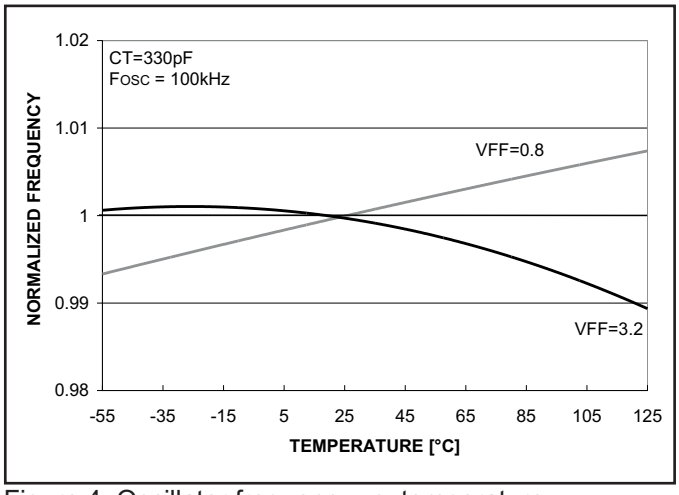
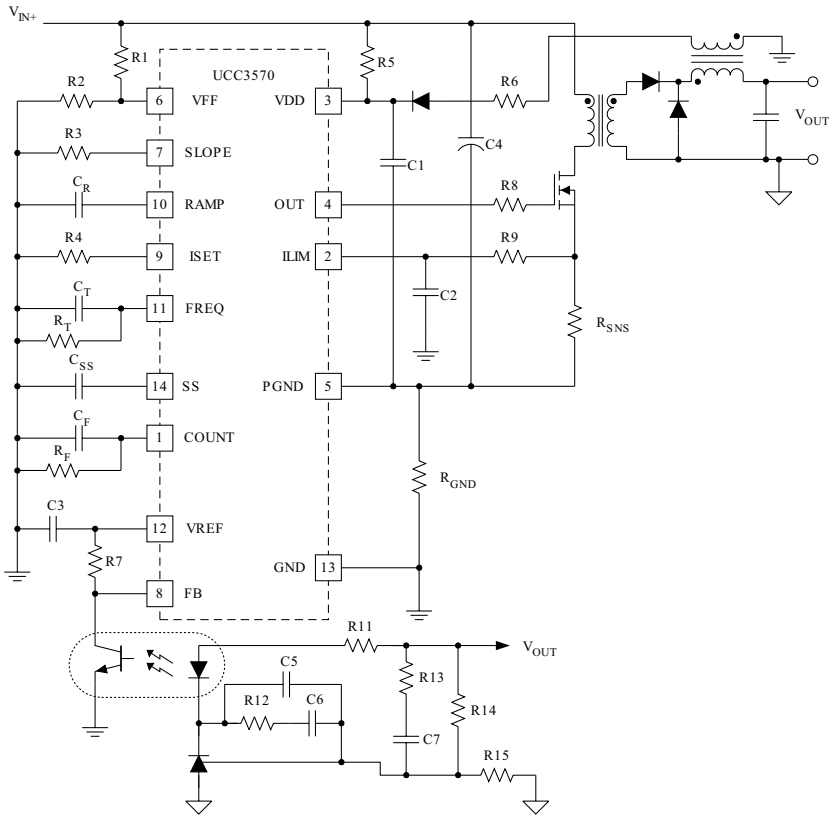


Figure 4. Oscillator frequency vs. temperature.

APPLICATION INFORMATION (cont.)



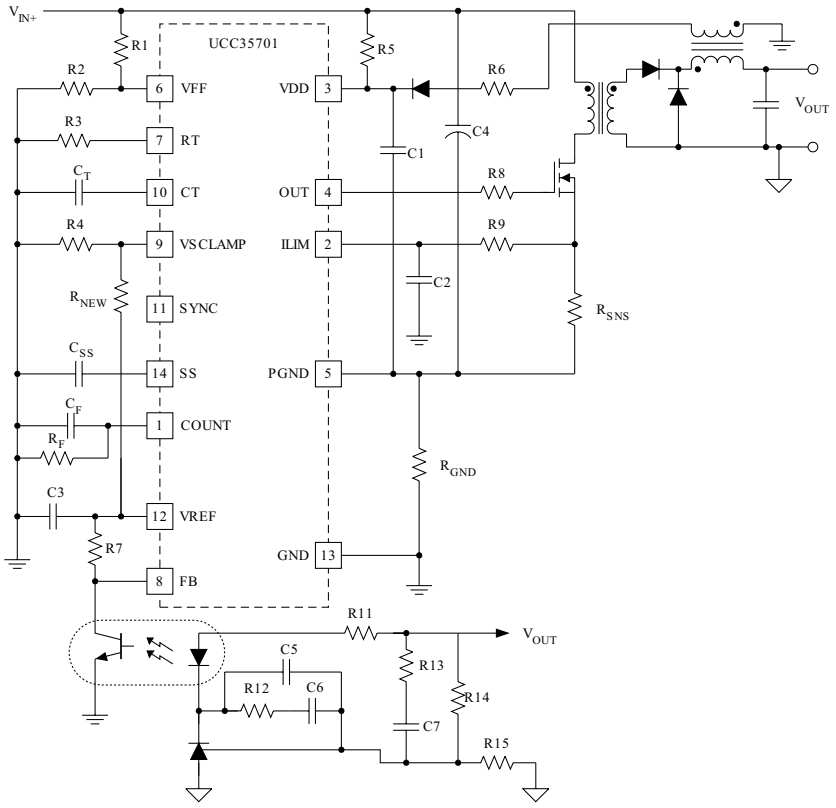


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Figure 6. Single-ended forward circuit comparison between UCC3570 and UCC37501.

REVISION HISTORY

DATE	REVISION	REASON
02/16/05	SLUS293B	Add FB to abs max table. Created revision history table.
6/16/05	SLUS293C	Updated block diagram and the SS pin description.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC25701D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC25701D	Samples
UCC25701DTR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC25701D	Samples
UCC25701N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	UCC25701N	Samples
UCC25701NG4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	UCC25701N	Samples
UCC25701PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25701	Samples
UCC25701PWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25701	Samples
UCC25702D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC25702D	Samples
UCC25702DTR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC25702D	Samples
UCC25702N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	UCC25702N	Samples
UCC25702PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25702	Samples
UCC25702PWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25702	Samples
UCC25702PWTR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25702	Samples
UCC25702PWTRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	25702	Samples
UCC35701D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC35701D	Samples
UCC35701DTR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC35701D	Samples
UCC35701N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UCC35701N	Samples
UCC35701PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	35701	Samples
UCC35702D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC35702D	Samples
UCC35702PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	35702	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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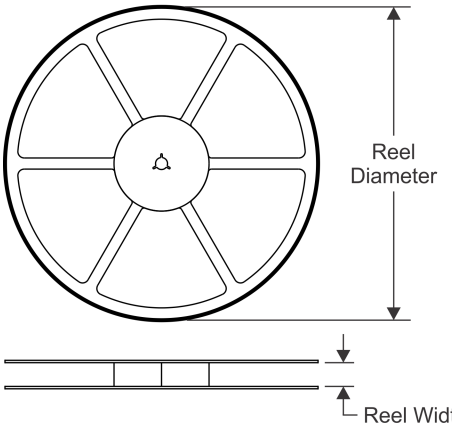
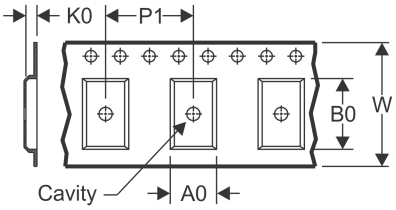
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

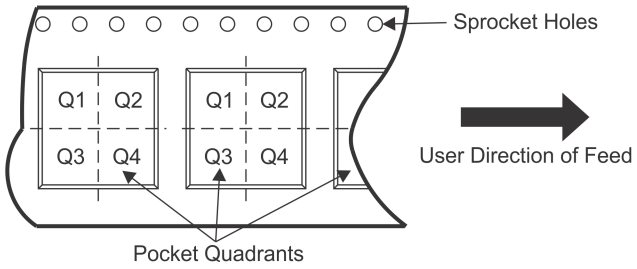


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

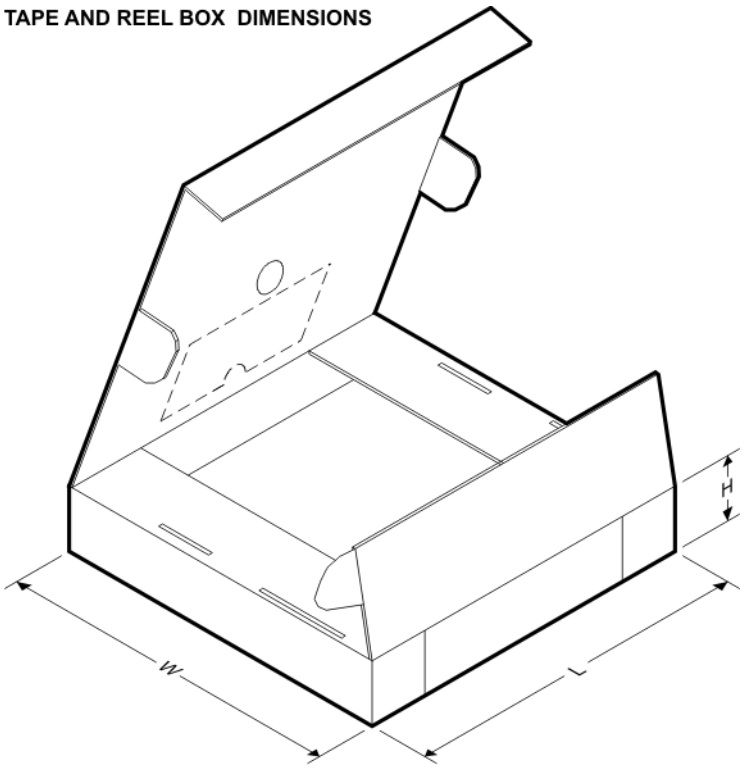
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC25701DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UCC25702DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UCC25702PWTR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
UCC35701DTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

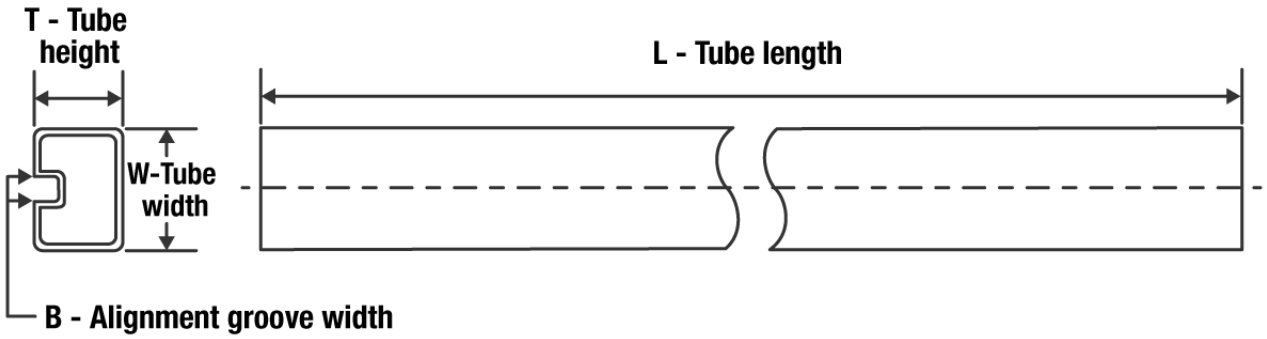
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC25701DTR	SOIC	D	14	2500	340.5	336.1	32.0
UCC25702DTR	SOIC	D	14	2500	340.5	336.1	32.0
UCC25702PWTR	TSSOP	PW	14	2000	853.0	449.0	35.0
UCC35701DTR	SOIC	D	14	2500	340.5	336.1	32.0

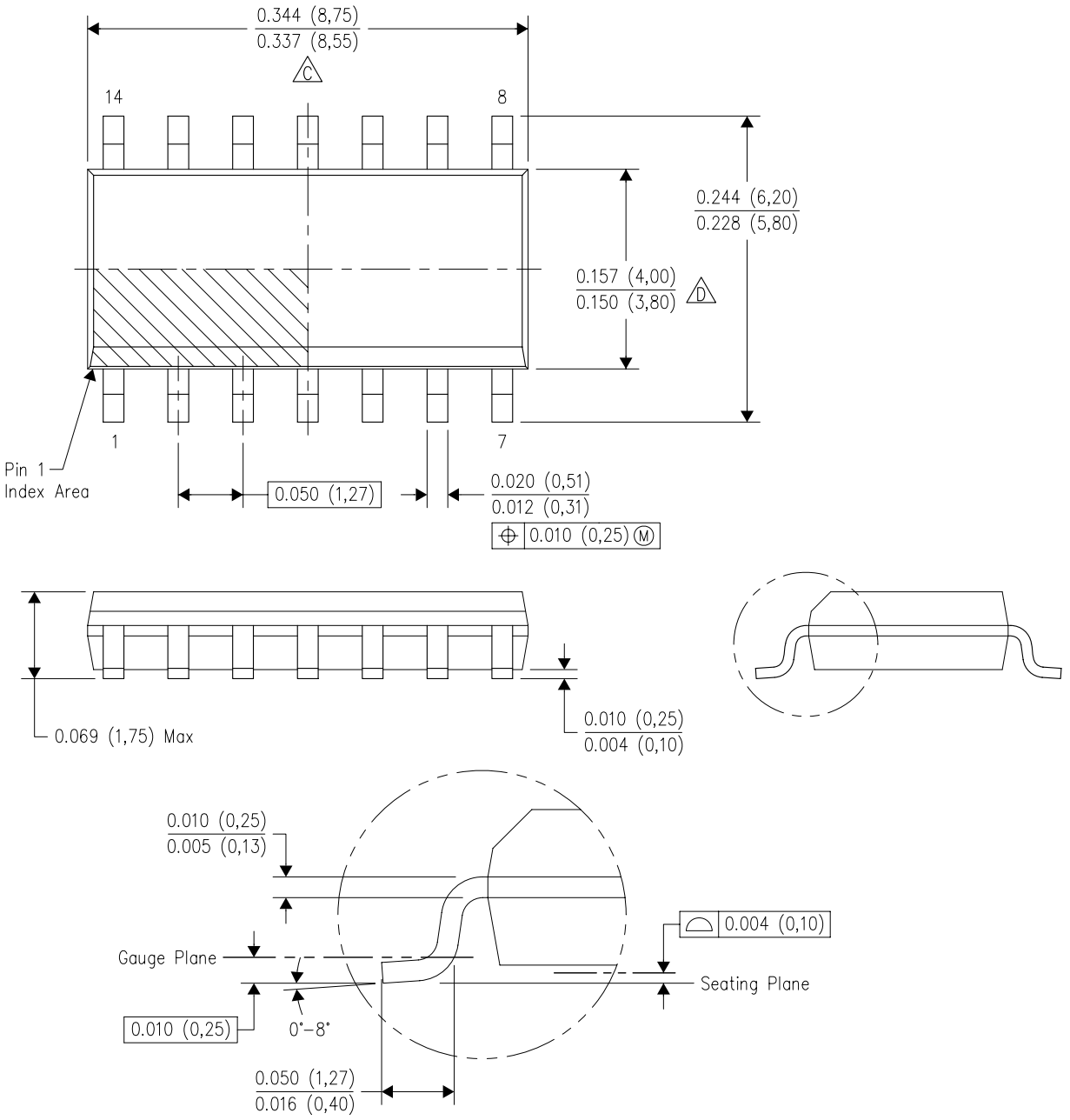
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC25701D	D	SOIC	14	50	507	8	3940	4.32
UCC25701N	N	PDIP	14	25	506	13.97	11230	4.32
UCC25701NG4	N	PDIP	14	25	506	13.97	11230	4.32
UCC25701PW	PW	TSSOP	14	90	530	10.2	3600	3.5
UCC25701PWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
UCC25702D	D	SOIC	14	50	507	8	3940	4.32
UCC25702N	N	PDIP	14	25	506	13.97	11230	4.32
UCC25702PW	PW	TSSOP	14	90	530	10.2	3600	3.5
UCC25702PWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
UCC35701D	D	SOIC	14	50	507	8	3940	4.32
UCC35701N	N	PDIP	14	25	506	13.97	11230	4.32
UCC35701PW	PW	TSSOP	14	90	530	10.2	3600	3.5
UCC35702D	D	SOIC	14	50	507	8	3940	4.32
UCC35702PW	PW	TSSOP	14	90	530	10.2	3600	3.5

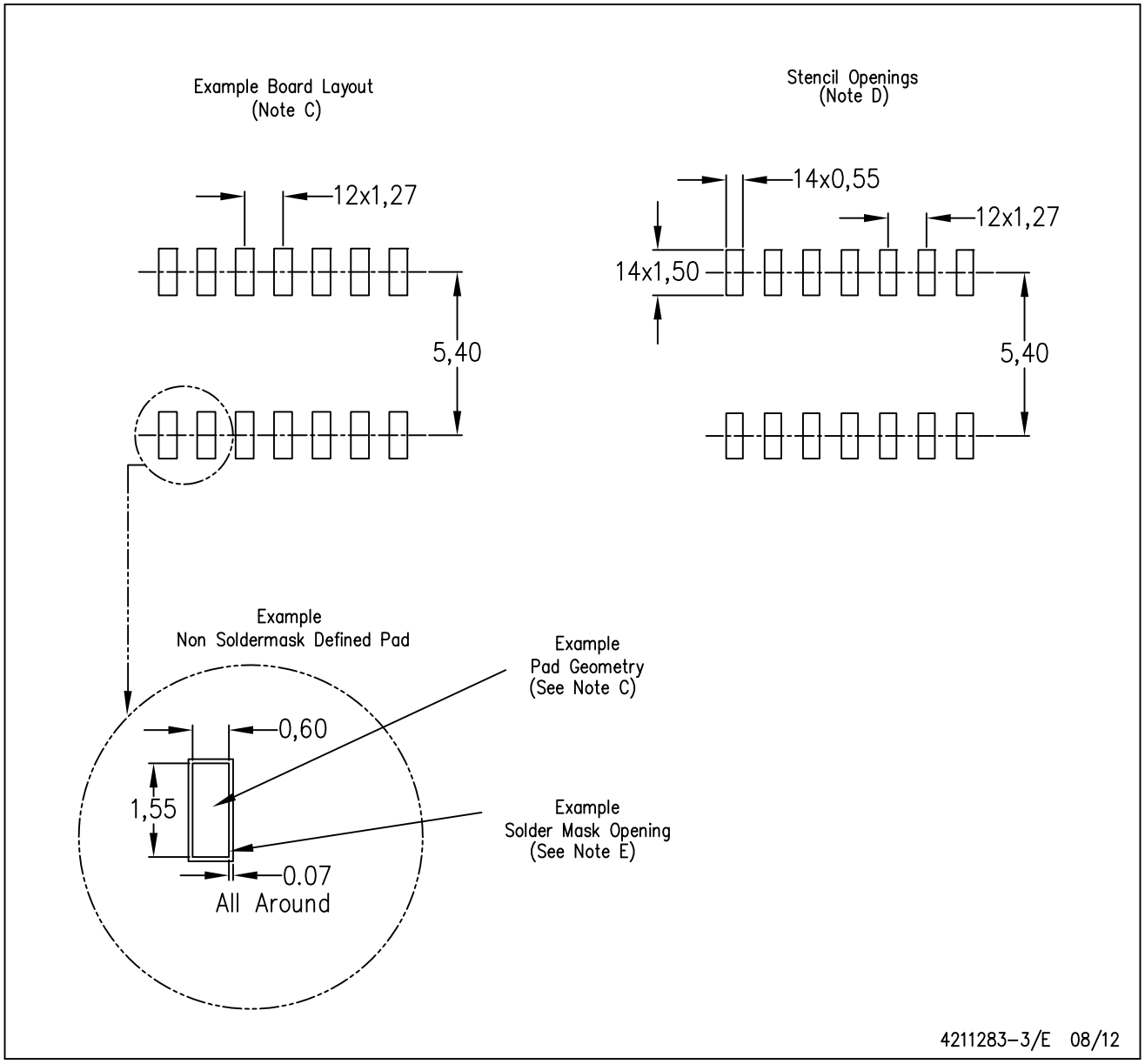
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

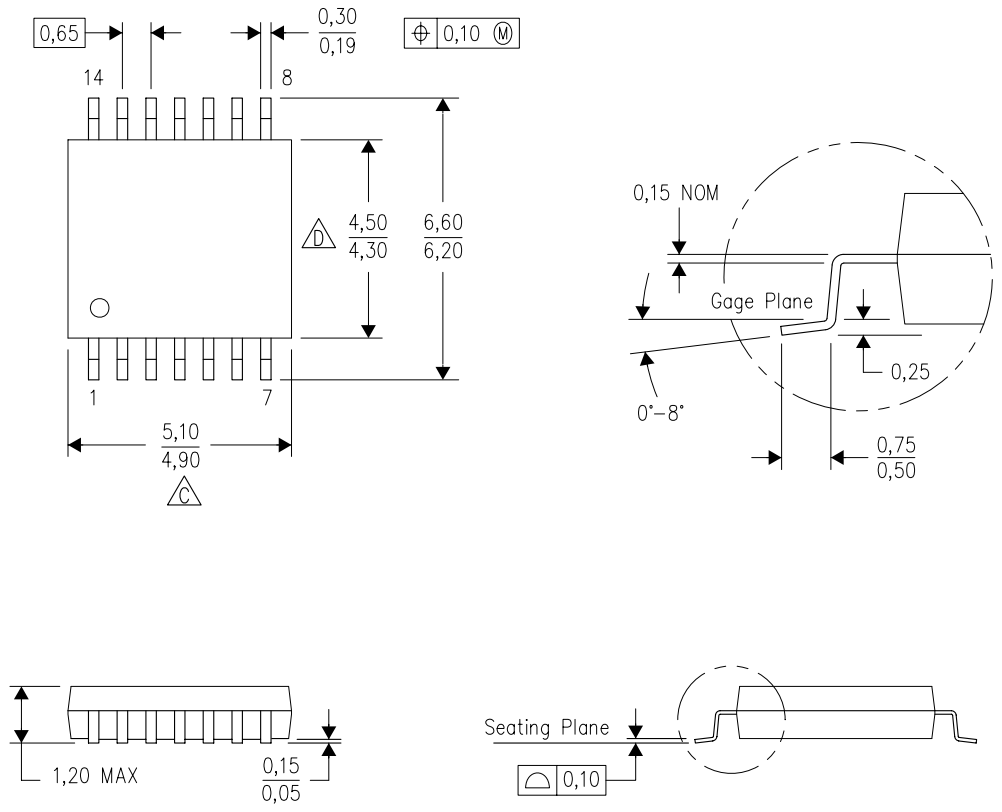
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

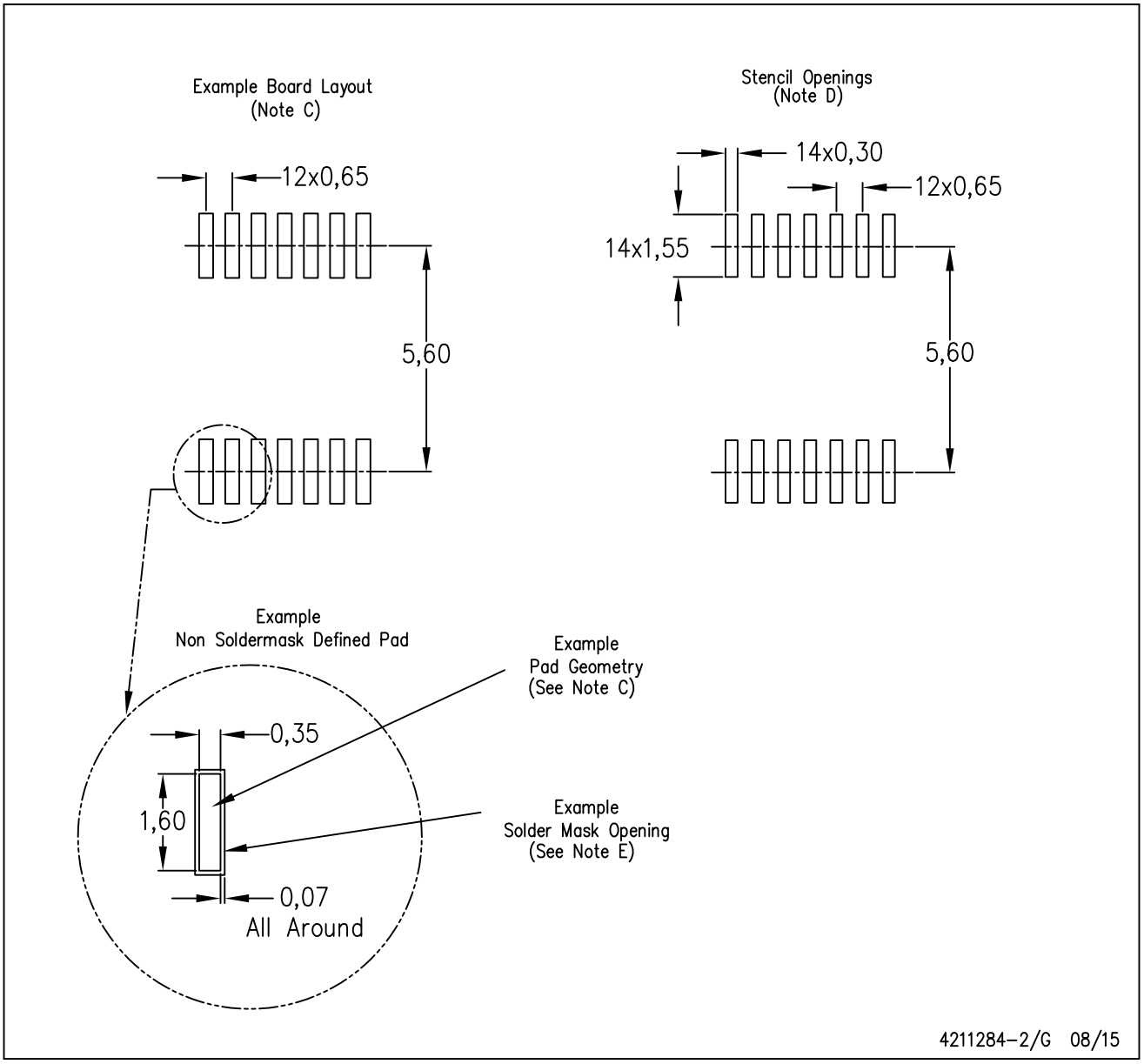
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

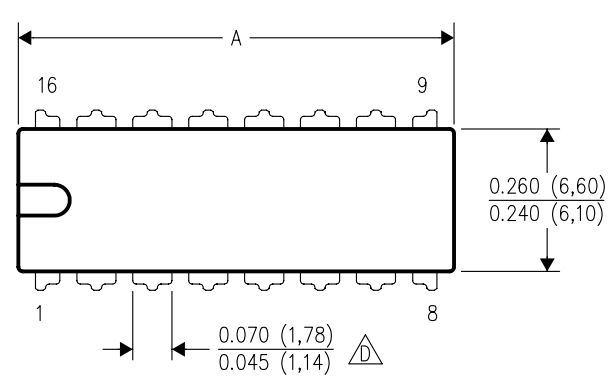


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

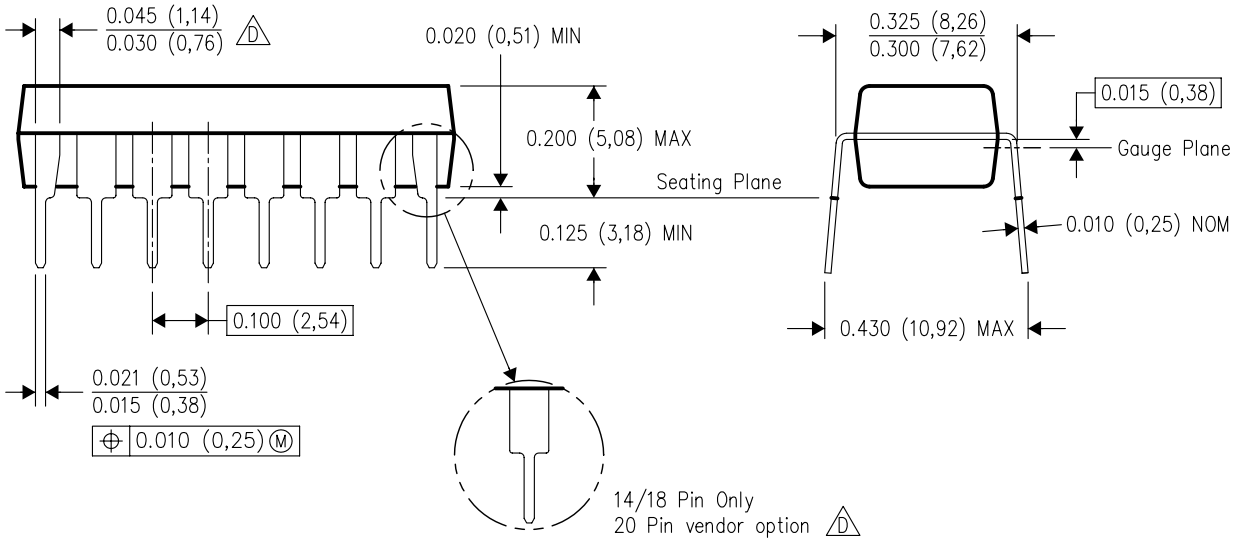
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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