

## LOW-POWER, DUAL-OUTPUT, CURRENT-MODE PWM CONTROLLER

### FEATURES

- BiCMOS Version of UC3846 Family
- 1.4-mA Maximum Operating Current
- 100- $\mu$ A Maximum Startup Current
- $\pm 0.5$ -A Peak Output Current
- 125-ns Circuit Delay
- Easier Parallelability
- Improved Benefits of Current Mode Control

### DESCRIPTION

The UCC3806 family of BiCMOS PWM controllers offers exceptionally improved performance with a familiar architecture. With the same block diagram and pinout of the popular UC3846 series, the UCC3806 line features increased switching frequency capability while greatly reducing the bias current used within the device. With a typical startup current of 50  $\mu$ A and a well defined voltage threshold for turn-on, these devices are favored

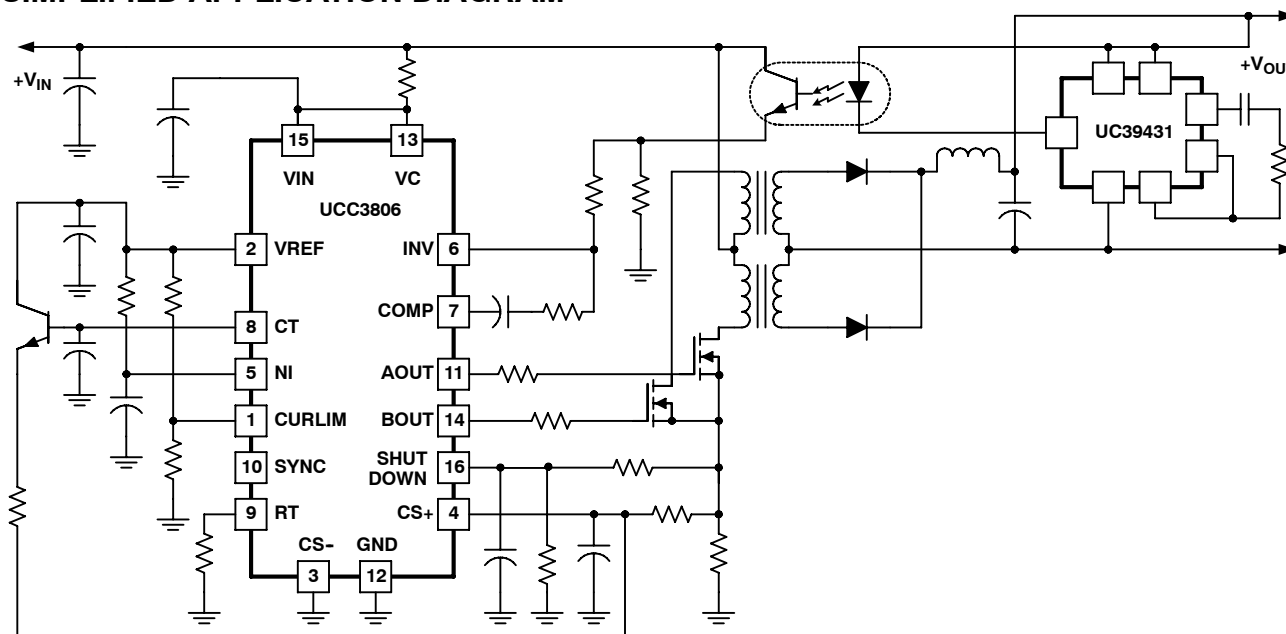
for applications ranging from off-line power supplies to battery operated portable equipment. Dual high-current, MOSFET driving outputs and a fast current sense loop further enhance device versatility.

All the benefits of current mode control including simpler loop closing, voltage feed-forward, parallelability with current sharing, pulse-by-pulse current limiting, and push/pull symmetry correction are readily achievable with the UCC3806 series.

These devices are available in multiple package options for both through-hole and surface mount applications; and in commercial, industrial, and military temperature ranges.

The UCC1806 is specified for operation from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , the UCC2806 is specified for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , and the UCC3806 is specified for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

### SIMPLIFIED APPLICATION DIAGRAM





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

|                                                                           |                             | UCx806                       | UNIT |
|---------------------------------------------------------------------------|-----------------------------|------------------------------|------|
| Supply voltage, $V_{IN}$                                                  | VIN, low impedance          | 15                           | V    |
| Supply current, $I_{IN}$                                                  | VIN, high impedance         | 25                           | mA   |
| Output supply voltage                                                     | VC                          | 18                           | V    |
| Output current                                                            | Continuous source or sink   | $\pm 200$                    | mA   |
|                                                                           | Gate drive                  | $\pm 500$                    |      |
|                                                                           | SYNC                        | $\pm 30$                     |      |
|                                                                           | COMP                        | $\pm 10$ to -(self-limiting) |      |
| Analog input voltage range                                                | CS-, CS+, NI, INV, SHUTDOWN | -0.3 to ( $V_{IN} + 0.3$ )   | V    |
| Storage temperature, $T_{stg}$                                            |                             | -65 to 150                   | °C   |
| Operating temperature, $T_J$                                              |                             | -55 to 150                   | °C   |
| Lead temperature, $T_{sol}$ , 1.6 mm (1/16 inch) from case for 10 seconds |                             | 300                          | °C   |

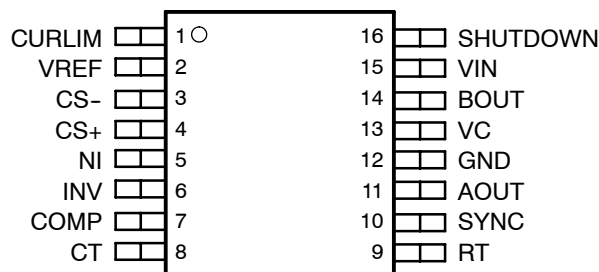
<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into and negative out of, the specified terminal.

## RECOMMENDED OPERATING CONDITIONS

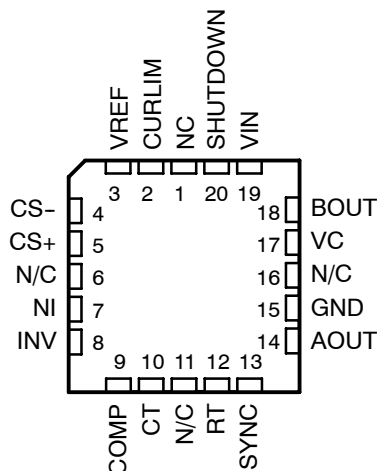
|                                       |         | MIN | NOM | MAX  | UNIT |
|---------------------------------------|---------|-----|-----|------|------|
| Input voltage, $V_{IN}$               |         | 8.0 |     | 14.5 | V    |
| Operating junction temperature, $T_J$ | UCC1806 | -55 |     | 125  | °C   |
|                                       | UCC2806 | -40 |     | 85   |      |
|                                       | UCC3806 | 0   |     | 70   |      |

## PACKAGE DESCRIPTION

**D, DW, J, M, N OR PW PACKAGE**  
(TOP VIEW)



**Q OR L PACKAGE**  
(TOP VIEW)



N/C - No connection

## ORDERING INFORMATION

| PACKAGED DEVICES |          |        |          | $T_A = T_J$     |                |             |
|------------------|----------|--------|----------|-----------------|----------------|-------------|
| DESIGNATOR       | TYPE     | OPTION | QUANTITY | - 55°C to 125°C | - 40°C to 85°C | 0°C to 70°C |
| D                | SOIC-16  | Tube   | 40       | —               | UCC2806D       | —           |
|                  |          | Reeled | 2,500    | —               | UCC2806DTR     | —           |
| DW               | SOICW-16 | Tube   | 40       | —               | UCC2806DW      | UCC3806DW   |
|                  |          | Reeled | 2,000    | —               | UCC2806DWTR    | UCC3806DWTR |
| J                | CDIP-16  | Tube   | 25       | UCC1806J        | UCC2806J       | UCC3806J    |
| L                | CLCC-20  | Tube   | 55       | UCC1806L        | —              | —           |
| M                | SSOP-16  | Reeled | 2,500    | —               | UCC2806MTR     | —           |
| N                | PDIP-16  | Tube   | 25       | —               | UCC2806N       | UCC3806N    |
| PW               | TSSOP-16 | Tube   | 90       | —               | UCC2806PW      | UCC3806PW   |
|                  |          | Reeled | 2,000    | —               | UCC2806PWTR    | UCC3806PWTR |
| Q                | PLCC-20  | Tube   | 46       | —               | UCC2806Q       | UCC3806Q    |
|                  |          | Reeled | 1,000    | —               | UCC2806QTR     | UCC3806QTR  |

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 12\text{ V}$ ,  $R_T = 33\text{ k}\Omega$ ,  $C_T = 330\text{ pF}$ ,  $C_{BYPASS}$  on  $V_{REF} = 0.01\text{ }\mu\text{F}$ ,  $-55^\circ\text{C} < T_A < 125^\circ\text{C}$  for the UCC1806,  $-40^\circ\text{C} < T_A < 85^\circ\text{C}$  for the UCC2806,  $0^\circ\text{C} < T_A < 70^\circ\text{C}$  for the UCC3806, and  $T_A = T_J$  (unless otherwise noted)

| PARAMETER                                |                            | TEST CONDITIONS    |                                                                                                | MIN  | TYP  | MAX  | UNIT |
|------------------------------------------|----------------------------|--------------------|------------------------------------------------------------------------------------------------|------|------|------|------|
| REFERENCE                                |                            |                    |                                                                                                |      |      |      |      |
| V <sub>REF</sub>                         | Supply, UVLO, turn-on      | UCC1806<br>UCC2806 |                                                                                                | 5.02 | 5.10 | 5.17 | V    |
|                                          |                            | UCC3806            |                                                                                                | 5.00 | 5.10 | 5.20 |      |
| Load regulation                          |                            |                    | 0.2 mA ≤ I <sub>OUT</sub> ≤ 5 mA                                                               | 3    |      | 25   | mV   |
| Total output variation <sup>(1)(2)</sup> |                            |                    | Line, load, temperature                                                                        | -150 |      | 150  |      |
| Output noise voltage <sup>(2)</sup>      |                            |                    | 10 Hz ≤ f <sub>OSC</sub> ≤ 10 kHz, T <sub>J</sub> = 25°C                                       | 70   |      |      | μV   |
| Long term stability <sup>(2)</sup>       |                            |                    | T <sub>A</sub> = 125°C, 1000 hours                                                             | 5    |      | 25   | mV   |
| Output short circuit                     |                            |                    |                                                                                                | -10  |      | -30  | mA   |
| OSCILLATOR                               |                            |                    |                                                                                                |      |      |      |      |
| Initial accuracy                         |                            |                    | T <sub>J</sub> = 25°C                                                                          | 42   | 47   | 52   | kHz  |
| Temperature stability <sup>(2)</sup>     |                            |                    | T(min) ≤ T <sub>A</sub> ≤ T(max)                                                               | 2%   |      |      |      |
| Amplitude                                |                            |                    |                                                                                                | 2.35 |      |      | V    |
| t <sub>DELAY</sub>                       | Delay-to-output time, SYNC | UCC1806<br>UCC2806 | V <sub>CT</sub> = 0 V, V <sub>RT</sub> = V <sub>REF</sub><br>0.8 V ≤ V <sub>SYNC</sub> ≤ 2.0 V | 50   |      | 125  | ns   |
|                                          |                            | UCC3806            | V <sub>CT</sub> = 0 V, V <sub>RT</sub> = V <sub>REF</sub><br>0.8 V ≤ V <sub>SYNC</sub> ≤ 2.0 V | 50   |      | 100  |      |

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 12\text{ V}$ ,  $R_T = 33\text{ k}\Omega$ ,  $C_T = 330\text{ pF}$ ,  $C_{BYPASS}$  on  $V_{REF} = 0.01\text{ }\mu\text{F}$ ,  $-55^\circ\text{C} < T_A < 125^\circ\text{C}$  for the UCC1806,  $-40^\circ\text{C} < T_A < 85^\circ\text{C}$  for the UCC2806,  $0^\circ\text{C} < T_A < 70^\circ\text{C}$  for the UCC3806, and  $T_A = T_J$  (unless otherwise noted)

| PARAMETER                                                                |                                   | TEST CONDITIONS                                                                                                                                       |                                                       | MIN  | TYP                | MAX  | UNIT |    |
|--------------------------------------------------------------------------|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------|------|--------------------|------|------|----|
| OSCILLATOR (continued)                                                   |                                   |                                                                                                                                                       |                                                       |      |                    |      |      |    |
| I <sub>DCHG</sub>                                                        | Discharge current                 | T <sub>J</sub> = 25°C,                                                                                                                                | V <sub>CT</sub> = 2.0 V                               | 2.5  |                    |      | mA   |    |
| V <sub>OL</sub>                                                          | Low-level output voltage, SYNC    | I <sub>OUT</sub> = 1 mA                                                                                                                               |                                                       | 0.4  |                    |      | V    |    |
| V <sub>OH</sub>                                                          | High-level output voltage, SYNC   | I <sub>OUT</sub> = -4 mA                                                                                                                              |                                                       | 2.4  |                    |      |      |    |
| V <sub>IL</sub>                                                          | Low-level input voltage, SYNC     | V <sub>CT</sub> = 0 V,                                                                                                                                | V <sub>RT</sub> = V <sub>REF</sub>                    | 0.8  |                    |      |      |    |
| V <sub>IH</sub>                                                          | High-level input voltage, SYNC    | V <sub>CT</sub> = 0 V,                                                                                                                                | V <sub>RT</sub> = V <sub>REF</sub>                    | 2.0  |                    |      |      |    |
| I <sub>SYNC</sub>                                                        | Input current, SYNC               |                                                                                                                                                       |                                                       | -1   |                    | 1    | μA   |    |
| ERROR AMPLIFIER                                                          |                                   |                                                                                                                                                       |                                                       |      |                    |      |      |    |
| Input offset voltage                                                     |                                   | UCC1806                                                                                                                                               |                                                       | 5    |                    |      | mV   |    |
|                                                                          |                                   | UCC2806                                                                                                                                               |                                                       |      |                    |      |      |    |
|                                                                          |                                   | UCC3806                                                                                                                                               |                                                       | 10   |                    |      |      |    |
| I <sub>BIAS</sub>                                                        | Input bias current                |                                                                                                                                                       |                                                       | -1   |                    |      | μA   |    |
| I <sub>OFFSET</sub>                                                      | Input offset current              |                                                                                                                                                       |                                                       | 500  |                    |      | nA   |    |
| CMR                                                                      | Common mode range <sup>(1)</sup>  |                                                                                                                                                       |                                                       | 0    | V <sub>IN</sub> -2 |      | V    |    |
| A <sub>VOL</sub>                                                         | Open loop gain                    | 1 V ≤ V <sub>OUT</sub> ≤ 4 V                                                                                                                          |                                                       | 80   | 100                |      | dB   |    |
| GBW                                                                      | bandwidth                         |                                                                                                                                                       |                                                       | 1    |                    |      | MHz  |    |
| I <sub>COMP_SINK</sub>                                                   | Output sink current               | V <sub>ID</sub> < -20 mV, V <sub>COMP</sub> = 1 V                                                                                                     |                                                       | 1    |                    |      | mA   |    |
| I <sub>COMP_SRC</sub>                                                    | Output source current             | V <sub>ID</sub> < 20 mV, V <sub>COMP</sub> = 3 V                                                                                                      |                                                       | -80  | -120               |      | μA   |    |
| V <sub>COMP_L</sub>                                                      | Low-level output voltage          | V <sub>ID</sub> = -50 mV                                                                                                                              |                                                       | 0.5  |                    |      | V    |    |
| V <sub>COMP_H</sub>                                                      | High-level output voltage         | V <sub>ID</sub> = -50 mV                                                                                                                              |                                                       | 4.5  |                    |      |      |    |
| CURRENT SENSE AMPLIFIER                                                  |                                   |                                                                                                                                                       |                                                       |      |                    |      |      |    |
| A                                                                        | Amplifier gain <sup>(3)(4)</sup>  | V <sub>CS-</sub> = 0 V, V <sub>CURLIM</sub> = V <sub>REF</sub>                                                                                        |                                                       | 2.75 | 3.00               | 3.35 | V/V  |    |
| Maximum differential input signal (V <sub>CS+</sub> - V <sub>CS-</sub> ) |                                   | V <sub>CURLIM</sub> = V <sub>NI</sub> = V <sub>REF</sub> , V <sub>INV</sub> = 0V                                                                      |                                                       | 1.1  |                    |      | V    |    |
| Input offset voltage                                                     |                                   | UCC1806                                                                                                                                               | V <sub>CURLIM</sub> = 0.5 V, V <sub>COMP</sub> = OPEN | 10   |                    |      | mV   |    |
|                                                                          |                                   | UCC2806                                                                                                                                               |                                                       |      |                    |      |      |    |
|                                                                          |                                   | UCC3806                                                                                                                                               | V <sub>CURLIM</sub> = 0.5 V, V <sub>COMP</sub> = OPEN | 10   |                    |      | 50   | mV |
| CMRR                                                                     | Common mode rejection ratio       | 0 V ≤ V <sub>CM</sub> ≤ (V <sub>IN</sub> - 3.5 V)                                                                                                     |                                                       | 60   |                    |      | dB   |    |
| PSRR                                                                     | Power supply rejection ratio      |                                                                                                                                                       |                                                       | 56   |                    |      | dB   |    |
| I <sub>BIAS</sub>                                                        | Input bias current <sup>(3)</sup> | V <sub>CURLIM</sub> = 0.5 V, V <sub>COMP</sub> = OPEN                                                                                                 |                                                       | -1   |                    |      | μA   |    |
| Input offset current <sup>(3)</sup>                                      |                                   | V <sub>CURLIM</sub> = 0.5 V, V <sub>COMP</sub> = OPEN                                                                                                 |                                                       | 1    |                    |      | μA   |    |
| Delay-to-output time <sup>(5)</sup>                                      |                                   | V <sub>NI</sub> = V <sub>REF</sub> , V <sub>INV</sub> = 0 V, V <sub>CURLIM</sub> = 2.75 V, (V <sub>CS+</sub> - V <sub>CS-</sub> ) = 0 V to 1.5 V step |                                                       | 125  |                    |      | 175  | ns |
| CURRENT LIMIT ADJUST                                                     |                                   |                                                                                                                                                       |                                                       |      |                    |      |      |    |
| Current limit offset                                                     |                                   | V <sub>CS-</sub> = V <sub>CS+</sub> = 0 V, V <sub>COMP</sub> = OPEN                                                                                   |                                                       | 0.4  | 0.5                | 0.6  | V    |    |
| I <sub>BIAS</sub>                                                        | Input bias current                |                                                                                                                                                       |                                                       | 1    |                    |      | μA   |    |
| Minimum latching current                                                 |                                   |                                                                                                                                                       |                                                       | 300  | 200                |      |      |    |
| Maximum non-latching current                                             |                                   |                                                                                                                                                       |                                                       | 200  |                    |      |      | 80 |

<sup>(1)</sup> Line range = 10 V to 15 V, load range = 0.2 mA to 5 mA

<sup>(2)</sup> Ensured by design. Not production tested.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 12\text{ V}$ ,  $R_T = 33\text{ k}\Omega$ ,  $C_T = 330\text{ pF}$ ,  $C_{BYPASS}$  on  $V_{REF} = 0.01\text{ }\mu\text{F}$ ,  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for the UCC1806,  $-40^\circ\text{C} < T_A < 85^\circ\text{C}$  for the UCC2806,  $0^\circ\text{C} < T_A < 70^\circ\text{C}$  for the UCC3806, and  $T_A = T_J$  (unless otherwise noted)

| SHUTDOWN TERMINAL             |                           |                    |                                                    |  |      |                 |      |    |
|-------------------------------|---------------------------|--------------------|----------------------------------------------------|--|------|-----------------|------|----|
| Threshold voltage             |                           | UCC1806            |                                                    |  | 0.94 | 1.00            | 1.06 | V  |
|                               |                           | UCC2806            |                                                    |  |      |                 |      |    |
|                               |                           | UCC3806            |                                                    |  | 0.9  | 1.0             | 1.1  |    |
| Input voltage range           |                           |                    |                                                    |  | 0    | V <sub>IN</sub> |      |    |
| t <sub>DLY</sub>              | Delay-to-output time      |                    | 0 V ≤ V <sub>SHUTDOWN</sub> ≤ 1.3 V                |  | 75   |                 | 150  | ns |
| OUTPUT                        |                           |                    |                                                    |  |      |                 |      |    |
| Output supply voltage         |                           |                    |                                                    |  | 2.5  | 15.0            |      | V  |
| Low-level output voltage      |                           | UCC1806<br>UCC2806 | I <sub>SINK</sub> = 20 mA                          |  | 100  | 300             |      |    |
|                               |                           |                    | I <sub>SINK</sub> = 100 mA                         |  | 0.4  | 1.1             |      |    |
|                               |                           | UCC3806            | I <sub>SINK</sub> = 20 mA                          |  | 100  | 200             |      |    |
|                               |                           |                    | I <sub>SINK</sub> = 100 mA                         |  | 0.4  | 1.1             |      |    |
| High-level output voltage     |                           |                    | I <sub>SRC</sub> = -20 mA                          |  | 11.6 | 11.9            |      |    |
|                               |                           |                    | I <sub>SRC</sub> = -100 mA                         |  | 11.0 | 11.6            |      |    |
| t <sub>RISE</sub>             | Rise time                 |                    | T <sub>J</sub> = 25°C, C <sub>LOAD</sub> = 1000 pF |  | 35   | 65              |      | ns |
| t <sub>FALL</sub>             | Fall time                 |                    | T <sub>J</sub> = 25°C, C <sub>LOAD</sub> = 1000 pF |  | 35   | 65              |      |    |
| UNDERVOLTAGE LOCKOUT (UVLO)   |                           |                    |                                                    |  |      |                 |      |    |
| V <sub>START</sub>            | Startup threshold voltage |                    |                                                    |  | 6.5  | 7.5             | 8.0  | V  |
| Threshold hysteresis          |                           |                    |                                                    |  | 0.75 |                 |      | V  |
| I <sub>START</sub>            | Startup current           |                    | V <sub>IN</sub> < V <sub>START</sub>               |  | 50   | 100             |      | μA |
| I                             | Operating supply current  |                    |                                                    |  | 1.0  | 1.4             |      | mA |
| V <sub>IN</sub> shunt voltage |                           |                    | I <sub>VIN</sub> = 10 mA                           |  | 15.0 | 17.5            |      |    |

- (1) Line range = 10 V to 15 V, load range = 0.2 mA to 5 mA
- (2) Ensured by design. Not production tested.
- (3) Parameters measured at trip point of latch with  $V_{NI} = V_{REF}$ ,  $V_{INV} = 0\text{V}$ .
- (4) Amplifier gain defined as:  $G = \Delta \text{ change at COMP} / \Delta \text{ change forced at CS+ delta voltage at CS+} = 0 \text{ to } 1\text{V}$
- (5) Current-sense amplifier output is slew rate limited to provide noise immunity.

## THERMAL RESISTANCE TABLE

| PACKAGE DESIGNATOR | PACKAGE TYPE | $\theta_{JC}$<br>( $^\circ\text{C/W}$ ) | $\theta_{JA}$<br>( $^\circ\text{C/W}$ ) |
|--------------------|--------------|-----------------------------------------|-----------------------------------------|
| D                  | SOIC-16      | 35                                      | 50 to 120 <sup>(1)</sup>                |
| DW                 | SOICW-16     | 27                                      | 50 to 100 <sup>(1)</sup>                |
| J                  | CDIP-16      | 28                                      | 80 to 120                               |
| L                  | CLCC-20      | 20                                      | 70 to 80                                |
| M                  | SSOP-16      | 38                                      | 144 to 172 <sup>(2)</sup>               |
| N                  | PDIP-16      | 45                                      | 90 <sup>(1)</sup>                       |
| PW                 | TSSOP-16     | 15                                      | 123 to 147 <sup>(2)</sup>               |
| Q                  | PLCC-20      | 34                                      | 43 to 75 <sup>(1)</sup>                 |

- (1) Specified  $\theta_{JA}$  (junction to ambient) is for devices mounted to 5 in<sup>2</sup> FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5 in<sup>2</sup> aluminum PC board. Test PWB was 0.062 in thick and typically used 0.635 mm trace widths for power packages and 1.3 mm trace widths for non-power packages with a 100x100 mil probe land area at the end of each trace.
- (2) Modeled data. If value range given for  $\theta_{JA}$ , the lower value is for 3x3 inch1 oz internal copper ground plane, and the higher value is for 1x1 inch ground plane. All model data assumes only one trace for each non-fused lead.

## TERMINAL FUNCTIONS

| NAME     | TERMINAL<br>PACKAGES |     | I/O | DESCRIPTION                                                                                                   |
|----------|----------------------|-----|-----|---------------------------------------------------------------------------------------------------------------|
|          | D/DW/J/M<br>/N/PW    | L,Q |     |                                                                                                               |
| AOUT     | 11                   | 14  | O   | High-current gate drive for the external MOSFETs                                                              |
| BOUT     | 14                   | 18  |     |                                                                                                               |
| COMP     | 7                    | 9   | O   | Output of the error amplifier                                                                                 |
| CS-      | 3                    | 4   | I   | Inverting input of the 3×, differential current sense amplifier                                               |
| CS+      | 4                    | 5   | I   | Non-inverting input of the 3×, differential current sense amplifier                                           |
| CT       | 8                    | 10  | I   | Oscillator timing capacitor connection point                                                                  |
| CURLIM   | 1                    | 2   | I   | Programs the primary current limit threshold that determines latching or retry after an overcurrent situation |
| GND      | 12                   | 15  | -   | Reference ground and power ground for all functions of this device                                            |
| INV      | 6                    | 8   | I   | Inverting input of the error amplifier.                                                                       |
| NI       | 5                    | 7   | I   | Non-inverting input of the error amplifier.                                                                   |
| RT       | 9                    | 12  | I   | Connection point for the oscillator timing resistor                                                           |
| SHUTDOWN | 16                   | 20  | I   | Provided for enhanced protection. When SHUTDOWN is driven above 1 V, AOUT and BOUT are forced low.            |
| SYNC     | 10                   | 13  | I/O | Allows providing external synchronization with TTL compatible thresholds.                                     |
| VC       | 13                   | 17  | I   | Input supply connection for the FET drive outputs.                                                            |
| VIN      | 15                   | 19  | I   | Input supply connection for this device.                                                                      |
| VREF     | 2                    | 3   | O   | Reference output.                                                                                             |

## DETAILED PIN DESCRIPTIONS

**AOUT and BOUT:** AOUT and BOUT provide alternating high current gate drive for the external MOSFETs. Duty cycle can be varied from 0% to 50% where minimum dead time is a function of CT. Both outputs use MOS transistor switches with inherent anti-parallel body diodes to clamp voltage swings to the supply rails, allowing operation without the use of clamp diodes.

**COMP:** COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier is a low output impedance, 2-MHz operational amplifier which allows sinking or sourcing of current at the COMP pin. The error amplifier is internally current limited, so that zero duty cycle can be commanded by externally forcing COMP to GND.

**CS-:** CS- is the inverting input of the 3× differential current sense amplifier.

**CS+:** CS+ is the non-inverting input of the 3× differential current sense amplifier.

**CT:** CT is the oscillator timing capacitor connection point, which is charged by the current set by RT. CT is discharged to GND through a 2.5-mA current sink. This causes a linear discharge of CT to 0 V which then initiates the next switching cycle. Dead time occurs during the discharge of CT, forcing AOUT and BOUT low. Switching frequency ( $f_s$ ) and dead time ( $t_D$ ) are approximated by:

$$f_s = \frac{1}{1.96 \times R_T \times C_T + t_D} \quad \text{and} \quad t_D = 956 \times C_T \quad (1)$$

## DETAILED PIN DESCRIPTIONS (continued)

**CURLIM:** CURLIM programs the primary current limit threshold and determines whether the device latches off or retries after an overcurrent condition. When a shutdown signal is generated, a 200- $\mu$ A current source to ground pulls down on CURLIM. If the voltage on the pin remains above 350 mV the device remains latched and the power must be cycled to restart. If the voltage on the pin falls below 350 mV, the device attempts a restart. The voltage threshold is typically set by a resistor divider from  $V_{REF}$  to ground. To calculate the current limit adjust voltage threshold the following equations can be used.

Current limit adjust latching mode voltage is calculated in equation (2)

$$V = \frac{V_{REF} - (R1 \times 300 \mu A)}{1 + \left(\frac{R1}{R2}\right)} > 350 \text{ mV} \quad (2)$$

Current limit adjust non-latching mode voltage is calculated in equation (3)

$$V = \frac{V_{REF} - (R1 \times 80 \mu A)}{1 + \left(\frac{R1}{R2}\right)} < 350 \text{ mV} \quad (3)$$

where

- R1 is the resistance from the VREF to CURLIM
- R2 is the resistance from CURLIM to GND

**GND:** GND is the reference ground and power ground for all functions of this part. Bypass and timing capacitors should be connected as close as possible to GND.

**RT:** RT is the connection point for the oscillator timing resistor. It has a low impedance input and is nominally at 1.25 V. The current through RT is mirrored to the timing capacitor pin, CT. This causes a linear charging of CT from 0 V to 2.35 V. Note that the current mirror is limited to a maximum of 100  $\mu$ A so  $R_T$  must be greater than 12.5 k $\Omega$ .

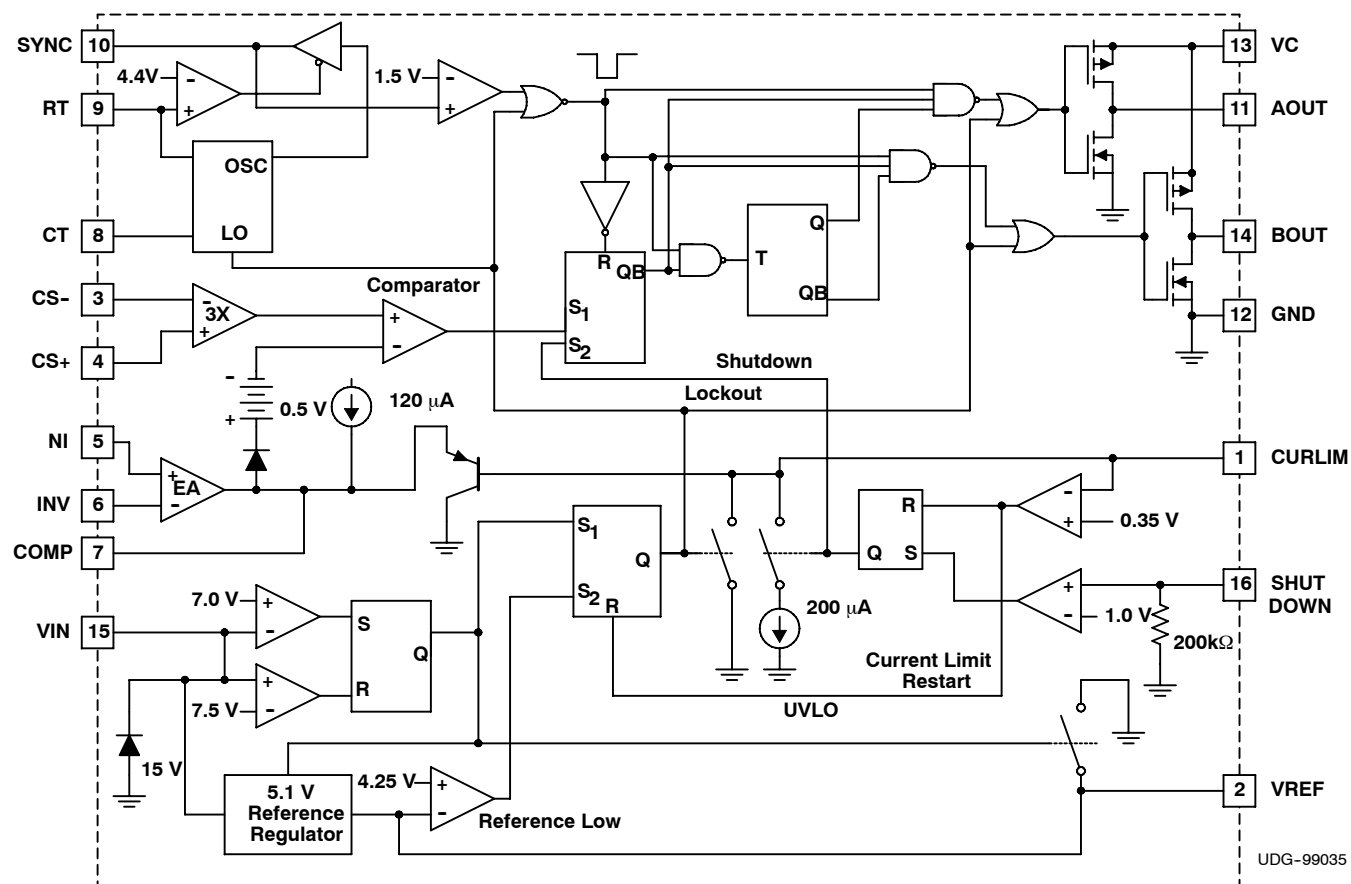
**SYNC:** SYNC is a bi-directional pin, allowing or providing external synchronization with TTL compatible thresholds. In a typical application RT is connected through a timing resistor to GND which allows the internal oscillator to free run. In this mode SYNC outputs a TTL compatible pulse during the oscillator dead time (when CT is being discharged). If RT is forced above 4.4 V, SYNC acts as an input with TTL compatible thresholds and the internal oscillator is disabled. When SYNC is high, greater than 2 V the outputs are held active low. When SYNC returns low, the outputs may be high until the on-time is terminated by the normal peak current signal, a fault seen at SHUTDOWN or the next high assertion of SYNC. Multiple UCC3806s can be synchronized by a single master UCC3806 or external clock.

**VC:** VC is the input supply connection for the FET drive outputs and has an input range from 2.5 V to 15 V. VC should be capacitively bypassed for proper operation.

**VIN:** VIN is the input supply connection for this device. The UCC1806 has a maximum startup threshold of 8 V and internally limited by means of a 15 V shunt regulator. The shunted supply current must be limited to 25 mA. For proper operation, VIN must be bypassed to GND with at least a 0.01- $\mu$ F ceramic capacitor

**VREF:** VREF is a 5.1 V  $\pm 1\%$  trimmed reference output with a 5 mA maximum available current. VREF must be bypassed to GND with at least a 0.1- $\mu$ F ceramic capacitor for proper operation.

## FUNCTIONAL BLOCK DIAGRAM



UDG-99035



TYPICAL CHARACTERISTICS

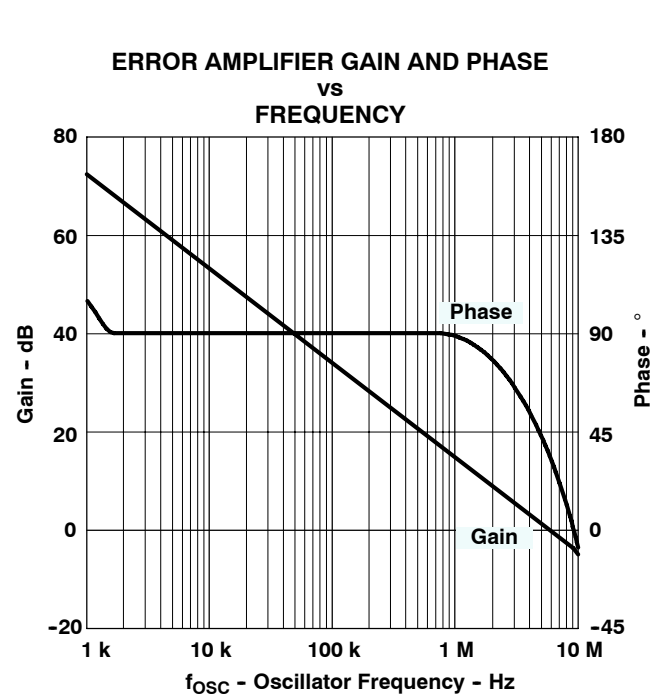


Figure 1.

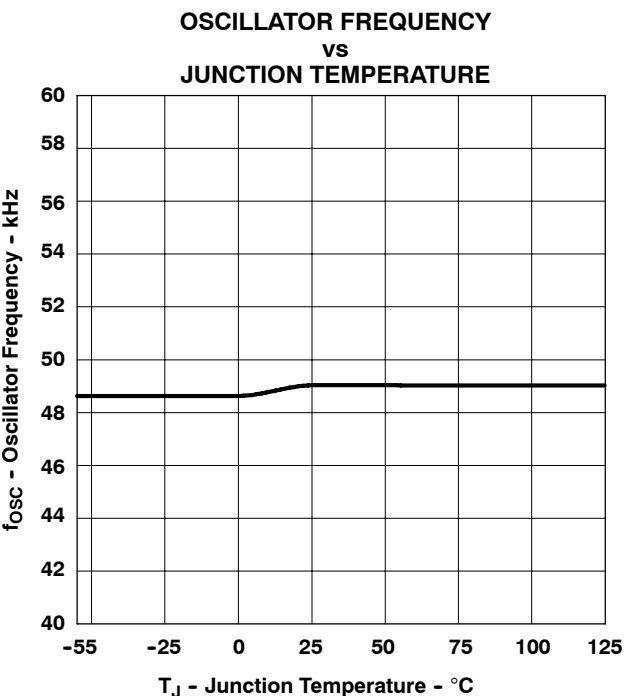


Figure 2.

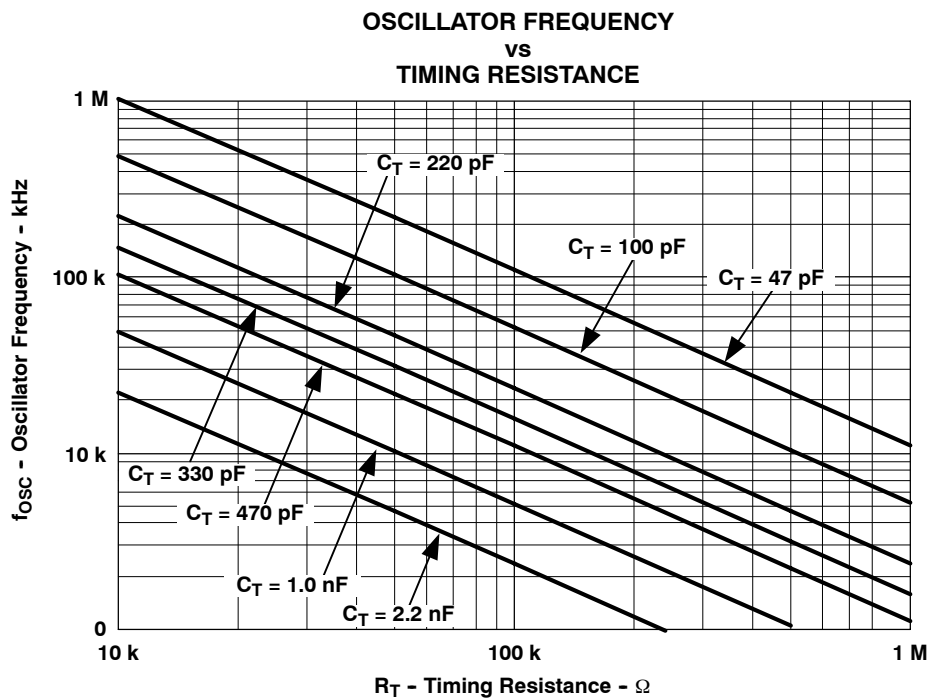


Figure 3.

## REVISION HISTORY

| DATE    | REVISION          | DESCRIPTION                                                                                                                   |
|---------|-------------------|-------------------------------------------------------------------------------------------------------------------------------|
| 3/11/05 | SLUS272D (Rev. D) | Updated Equation 2 and 3 to remove x3 factor.                                                                                 |
| 5/3/05  | SLUS272E (Rev. E) | Adjusted the factors of the switching frequency, Equation 1 and modified the typical discharge current from 2.0 mA to 2.5 mA. |

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type  | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|---------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-9457501MEA  | ACTIVE                | CDIP          | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| 5962-9457501Q2A  | ACTIVE                | LCCC          | FK              | 20   | 1           | TBD                     | POST-PLATE       | N / A for Pkg Type           |
| UCC1806J         | ACTIVE                | CDIP          | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| UCC1806J883B     | ACTIVE                | CDIP          | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| UCC1806L         | ACTIVE                | LCCC          | FK              | 20   | 1           | TBD                     | POST-PLATE       | N / A for Pkg Type           |
| UCC1806L883B     | ACTIVE                | LCCC          | FK              | 20   | 1           | TBD                     | POST-PLATE       | N / A for Pkg Type           |
| UCC2806D         | ACTIVE                | SOIC          | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2806DG4       | ACTIVE                | SOIC          | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2806DTR       | ACTIVE                | SOIC          | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2806DTRG4     | ACTIVE                | SOIC          | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2806DW        | ACTIVE                | SOIC          | DW              | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2806DWG4      | ACTIVE                | SOIC          | DW              | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2806DWTR      | ACTIVE                | SOIC          | DW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2806DWTRG4    | ACTIVE                | SOIC          | DW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2806J         | ACTIVE                | CDIP          | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| UCC2806M         | ACTIVE                | SSOP/<br>QSOP | DBQ             | 16   | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2806MG4       | ACTIVE                | SSOP/<br>QSOP | DBQ             | 16   | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2806MTR       | ACTIVE                | SSOP/<br>QSOP | DBQ             | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2806MTRG4     | ACTIVE                | SSOP/<br>QSOP | DBQ             | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2806N         | ACTIVE                | PDIP          | N               | 16   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | N / A for Pkg Type           |
| UCC2806NG4       | ACTIVE                | PDIP          | N               | 16   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | N / A for Pkg Type           |
| UCC2806PW        | ACTIVE                | TSSOP         | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2806PWG4      | ACTIVE                | TSSOP         | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2806PWTR      | ACTIVE                | TSSOP         | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2806PWTRG4    | ACTIVE                | TSSOP         | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC2806Q         | ACTIVE                | PLCC          | FN              | 20   | 46          | Green (RoHS & no Sb/Br) | CU SN            | Level-2-260C-1 YEAR          |
| UCC2806QG3       | ACTIVE                | PLCC          | FN              | 20   | 46          | Green (RoHS & no Sb/Br) | CU SN            | Level-2-260C-1 YEAR          |
| UCC3806DW        | ACTIVE                | SOIC          | DW              | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| no Sb/Br)        |                       |              |                 |      |             |                         |                  |                              |
| UCC3806DWG4      | ACTIVE                | SOIC         | DW              | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC3806DWTR      | ACTIVE                | SOIC         | DW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC3806DWTRG4    | ACTIVE                | SOIC         | DW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC3806J         | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| UCC3806N         | ACTIVE                | PDIP         | N               | 16   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | N / A for Pkg Type           |
| UCC3806NG4       | ACTIVE                | PDIP         | N               | 16   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | N / A for Pkg Type           |
| UCC3806PW        | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC3806PWG4      | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| UCC3806Q         | ACTIVE                | PLCC         | FN              | 20   | 46          | Green (RoHS & no Sb/Br) | CU SN            | Level-2-260C-1 YEAR          |
| UCC3806QG3       | ACTIVE                | PLCC         | FN              | 20   | 46          | Green (RoHS & no Sb/Br) | CU SN            | Level-2-260C-1 YEAR          |
| UCC3806QTR       | ACTIVE                | PLCC         | FN              | 20   | 1000        | Green (RoHS & no Sb/Br) | CU SN            | Level-2-260C-1 YEAR          |
| UCC3806QTRG3     | ACTIVE                | PLCC         | FN              | 20   | 1000        | Green (RoHS & no Sb/Br) | CU SN            | Level-2-260C-1 YEAR          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF UCC1806, UCC2806, UCC2806M, UCC3806, UCC3806M :**

- Space: [UCC1806-SP](#)

NOTE: Qualified Version Definitions:

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)     | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)                  | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|------------------------------------------|-------------------------|
| 5962-9457501MEA  | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9457501ME<br>A<br>UCC1806J/883B     | <a href="#">Samples</a> |
| 5962-9457501Q2A  | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-<br>9457501Q2A<br>UCC1806L/<br>883B | <a href="#">Samples</a> |
| 5962-9457501V2A  | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-<br>9457501V2A<br>UCC1806L<br>QMLV  | <a href="#">Samples</a> |
| 5962-9457501VEA  | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9457501VE<br>A<br>UCC1806JQMLV      | <a href="#">Samples</a> |
| UCC1806J         | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | UCC1806J                                 | <a href="#">Samples</a> |
| UCC1806J883B     | ACTIVE        | CDIP         | J               | 16   | 1           | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-9457501ME<br>A<br>UCC1806J/883B     | <a href="#">Samples</a> |
| UCC1806L         | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | UCC1806L                                 | <a href="#">Samples</a> |
| UCC1806L883B     | ACTIVE        | LCCC         | FK              | 20   | 1           | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | 5962-<br>9457501Q2A<br>UCC1806L/<br>883B | <a href="#">Samples</a> |
| UCC2806D         | ACTIVE        | SOIC         | D               | 16   | 40          | RoHS & Green        | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | UCC2806D                                 | <a href="#">Samples</a> |
| UCC2806DTR       | ACTIVE        | SOIC         | D               | 16   | 2500        | RoHS & Green        | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | UCC2806D                                 | <a href="#">Samples</a> |
| UCC2806DW        | ACTIVE        | SOIC         | DW              | 16   | 40          | RoHS & Green        | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | UCC2806DW                                | <a href="#">Samples</a> |
| UCC2806DWG4      | ACTIVE        | SOIC         | DW              | 16   | 40          | RoHS & Green        | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | UCC2806DW                                | <a href="#">Samples</a> |
| UCC2806DWTR      | ACTIVE        | SOIC         | DW              | 16   | 2000        | RoHS & Green        | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | UCC2806DW                                | <a href="#">Samples</a> |
| UCC2806DWTRG4    | ACTIVE        | SOIC         | DW              | 16   | 2000        | TBD                 | Call TI                              | Call TI              | -40 to 85    |                                          | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)     | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|---------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| UCC2806J         | ACTIVE        | CDIP         | J                  | 16   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -40 to 85    | UCC2806J                | <a href="#">Samples</a> |
| UCC2806M         | ACTIVE        | SSOP         | DBQ                | 16   | 75             | RoHS & Green        | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | UCC2806M                | <a href="#">Samples</a> |
| UCC2806MTR       | ACTIVE        | SSOP         | DBQ                | 16   | 2500           | RoHS & Green        | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | UCC2806M                | <a href="#">Samples</a> |
| UCC2806N         | ACTIVE        | PDIP         | N                  | 16   | 25             | RoHS & Green        | NIPDAU                               | N / A for Pkg Type   | -40 to 85    | UCC2806N                | <a href="#">Samples</a> |
| UCC2806PW        | ACTIVE        | TSSOP        | PW                 | 16   | 90             | RoHS & Green        | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | 2806                    | <a href="#">Samples</a> |
| UCC2806PWTR      | ACTIVE        | TSSOP        | PW                 | 16   | 2000           | RoHS & Green        | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | 2806                    | <a href="#">Samples</a> |
| UCC2806PWTRG4    | ACTIVE        | TSSOP        | PW                 | 16   | 2000           | RoHS & Green        | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 85    | 2806                    | <a href="#">Samples</a> |
| UCC3806DW        | ACTIVE        | SOIC         | DW                 | 16   | 40             | RoHS & Green        | NIPDAU                               | Level-2-260C-1 YEAR  | 0 to 70      | UCC3806DW               | <a href="#">Samples</a> |
| UCC3806DWG4      | ACTIVE        | SOIC         | DW                 | 16   | 40             | RoHS & Green        | NIPDAU                               | Level-2-260C-1 YEAR  | 0 to 70      | UCC3806DW               | <a href="#">Samples</a> |
| UCC3806DWTR      | ACTIVE        | SOIC         | DW                 | 16   | 2000           | RoHS & Green        | NIPDAU                               | Level-2-260C-1 YEAR  | 0 to 70      | UCC3806DW               | <a href="#">Samples</a> |
| UCC3806J         | ACTIVE        | CDIP         | J                  | 16   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | 0 to 70      | UCC3806J                | <a href="#">Samples</a> |
| UCC3806N         | ACTIVE        | PDIP         | N                  | 16   | 25             | RoHS & Green        | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | UCC3806N                | <a href="#">Samples</a> |
| UCC3806NG4       | ACTIVE        | PDIP         | N                  | 16   | 25             | RoHS & Green        | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | UCC3806N                | <a href="#">Samples</a> |
| UCC3806PW        | ACTIVE        | TSSOP        | PW                 | 16   | 90             | RoHS & Green        | NIPDAU                               | Level-2-260C-1 YEAR  |              | 3806                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF UCC1806, UCC1806-SP, UCC2806, UCC2806M, UCC3806, UCC3806M :**

- Catalog : [UCC3806](#), [UCC1806](#), [UCC2806](#), [UCC3806M](#), [UCC3806](#)
- Military : [UCC2806M](#), [UCC1806](#), [UCC1806](#)
- Space : [UCC1806-SP](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| UCC2806DTR  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| UCC2806DWTR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| UCC2806MTR  | SSOP         | DBQ             | 16   | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| UCC2806PWTR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| UCC3806DWTR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |

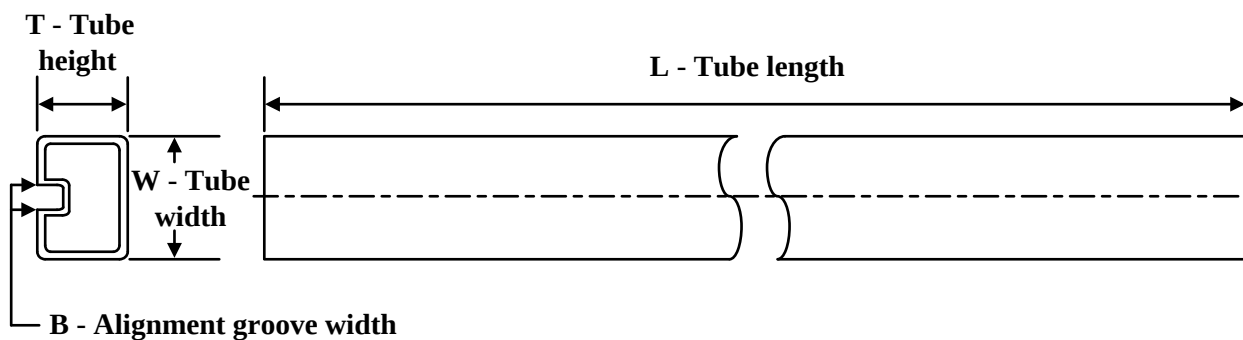
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| UCC2806DTR  | SOIC         | D               | 16   | 2500 | 356.0       | 356.0      | 35.0        |
| UCC2806DWTR | SOIC         | DW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| UCC2806MTR  | SSOP         | DBQ             | 16   | 2500 | 356.0       | 356.0      | 35.0        |
| UCC2806PWTR | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| UCC3806DWTR | SOIC         | DW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |

## TUBE



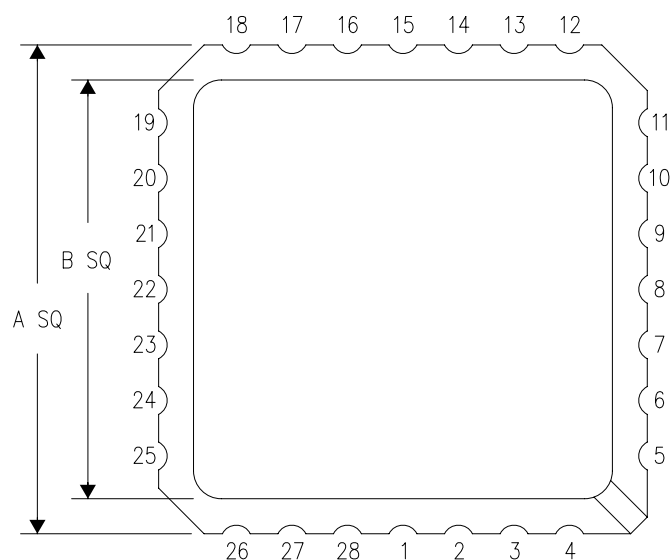
\*All dimensions are nominal

| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9457501Q2A | FK           | LCCC         | 20   | 1   | 506.98 | 12.06  | 2030   | NA     |
| 5962-9457501V2A | FK           | LCCC         | 20   | 1   | 506.98 | 12.06  | 2030   | NA     |
| UCC1806L        | FK           | LCCC         | 20   | 1   | 506.98 | 12.06  | 2030   | NA     |
| UCC1806L883B    | FK           | LCCC         | 20   | 1   | 506.98 | 12.06  | 2030   | NA     |
| UCC2806D        | D            | SOIC         | 16   | 40  | 506.6  | 8      | 3940   | 4.32   |
| UCC2806DW       | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UCC2806DWG4     | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UCC2806M        | DBQ          | SSOP         | 16   | 75  | 506.6  | 8      | 3940   | 4.32   |
| UCC2806N        | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UCC2806PW       | PW           | TSSOP        | 16   | 90  | 508    | 8.5    | 3250   | 2.8    |
| UCC3806DW       | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UCC3806DWG4     | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UCC3806N        | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UCC3806NG4      | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UCC3806PW       | PW           | TSSOP        | 16   | 90  | 530    | 10.2   | 3600   | 3.5    |

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF<br>TERMINALS<br>** | A                |                  | B                |                  |
|---------------------------|------------------|------------------|------------------|------------------|
|                           | MIN              | MAX              | MIN              | MAX              |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                        | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                        | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

D (R-PDSO-G16)

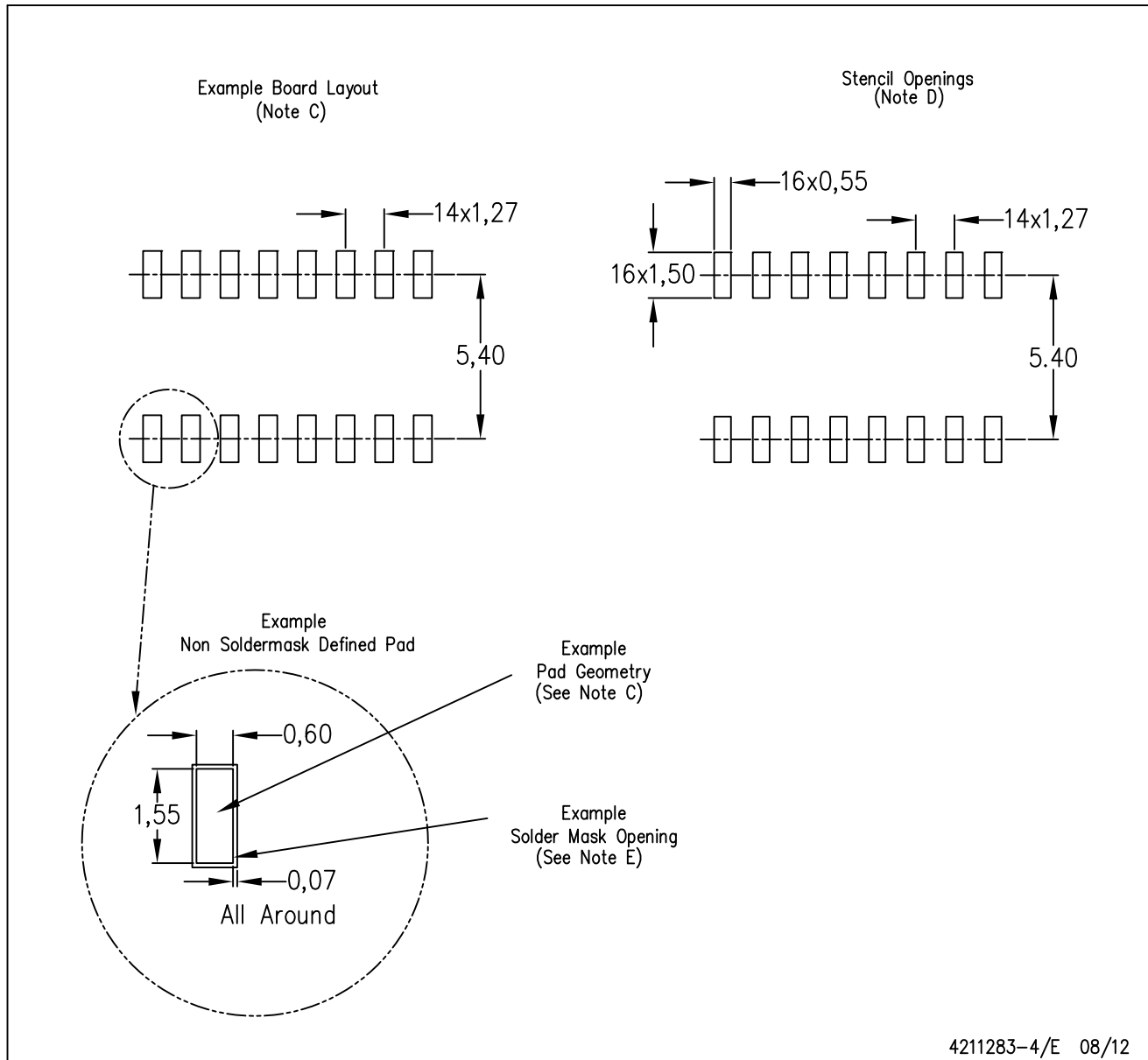
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

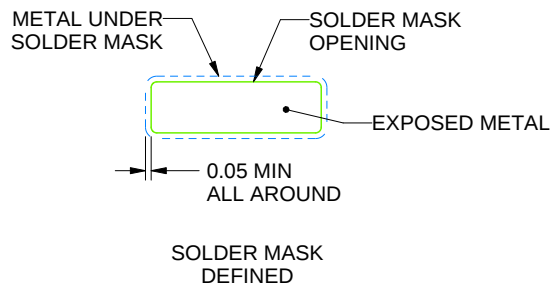
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

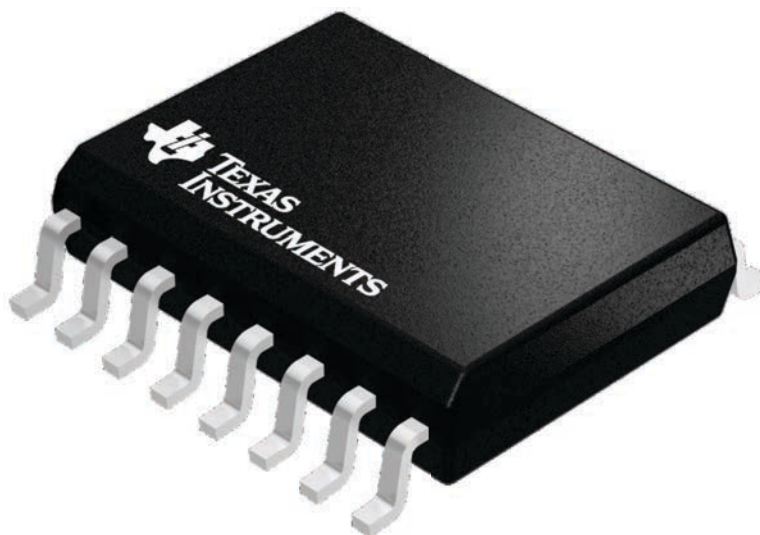
**DW 16**

**SOIC - 2.65 mm max height**

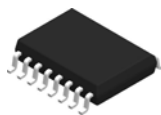
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A

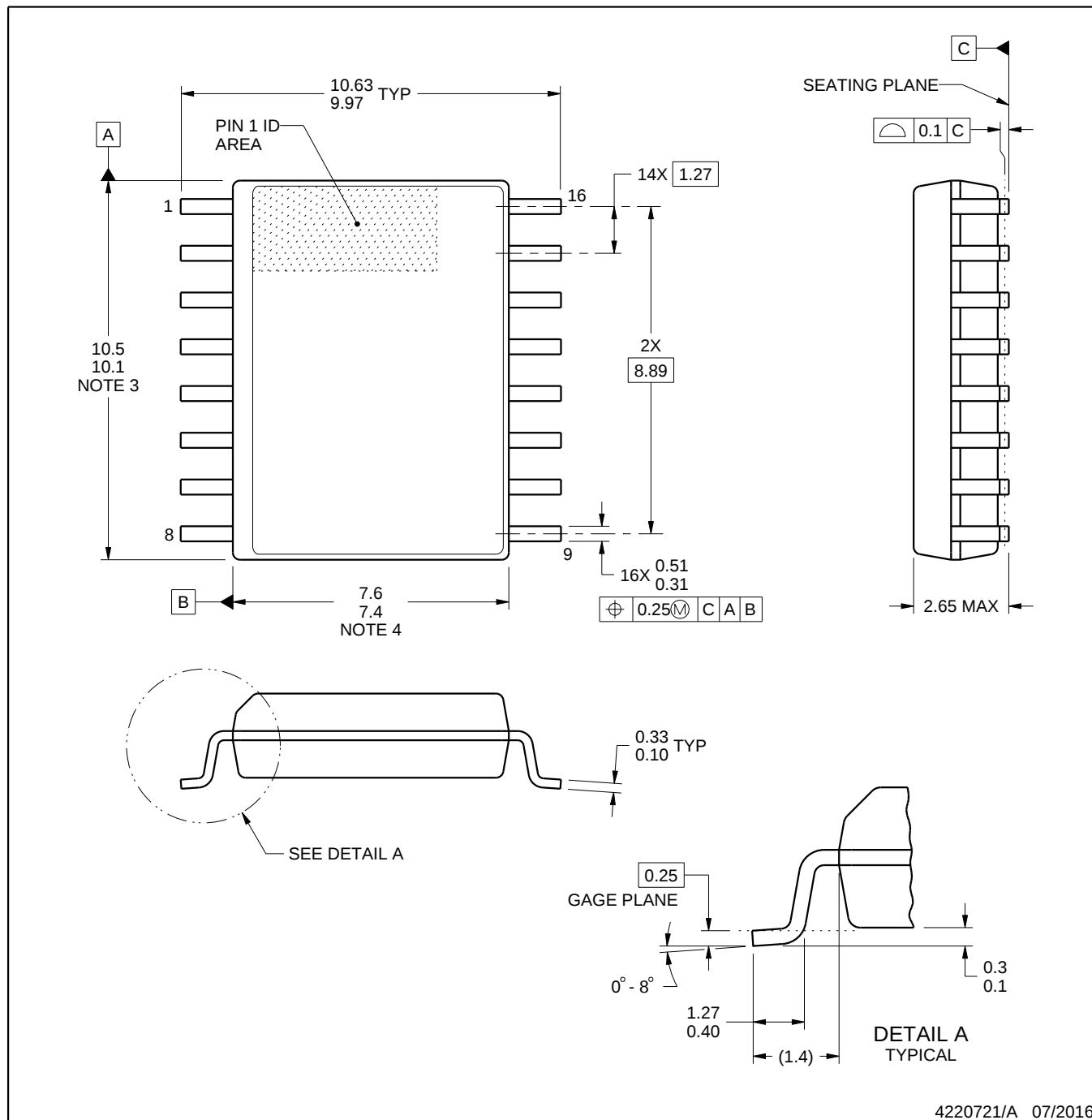


DW0016A

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

### NOTES:

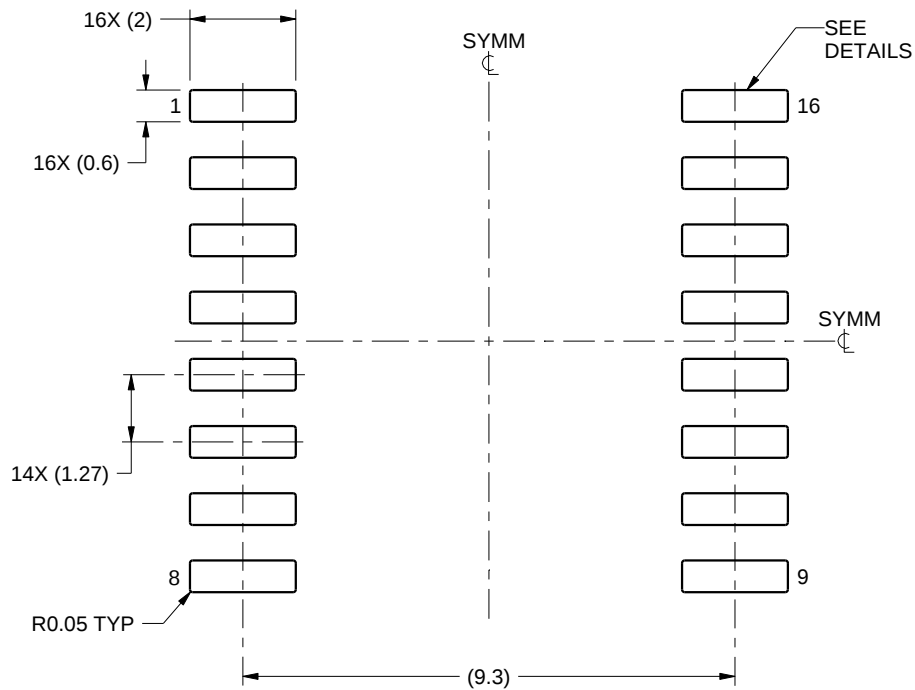
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

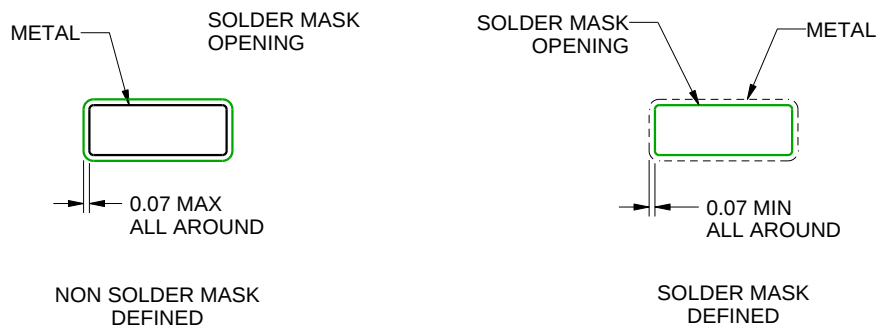
DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

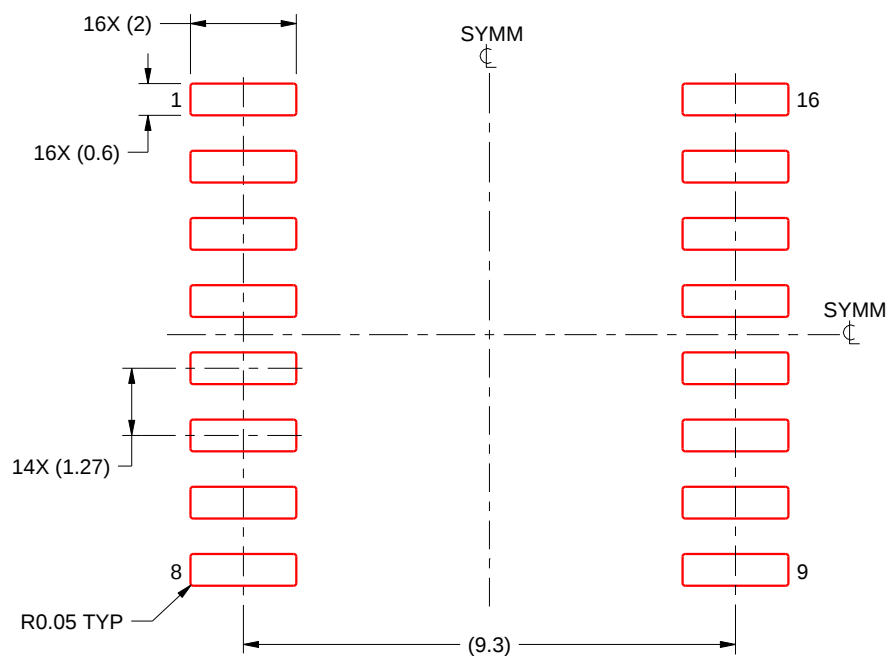
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

4220721/A 07/2016

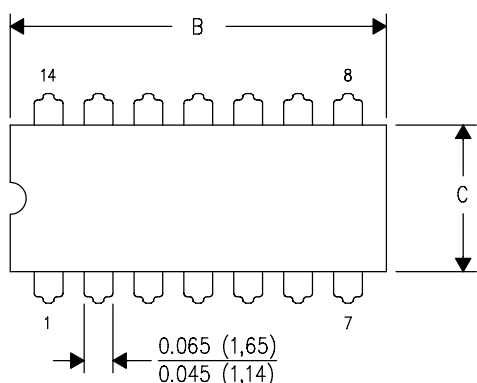
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

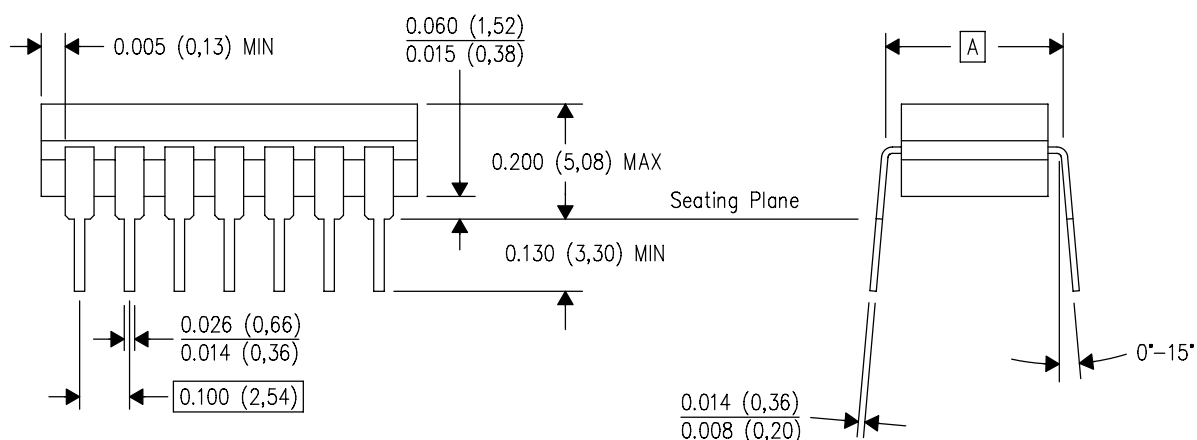
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE

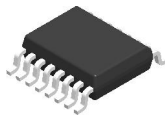


| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

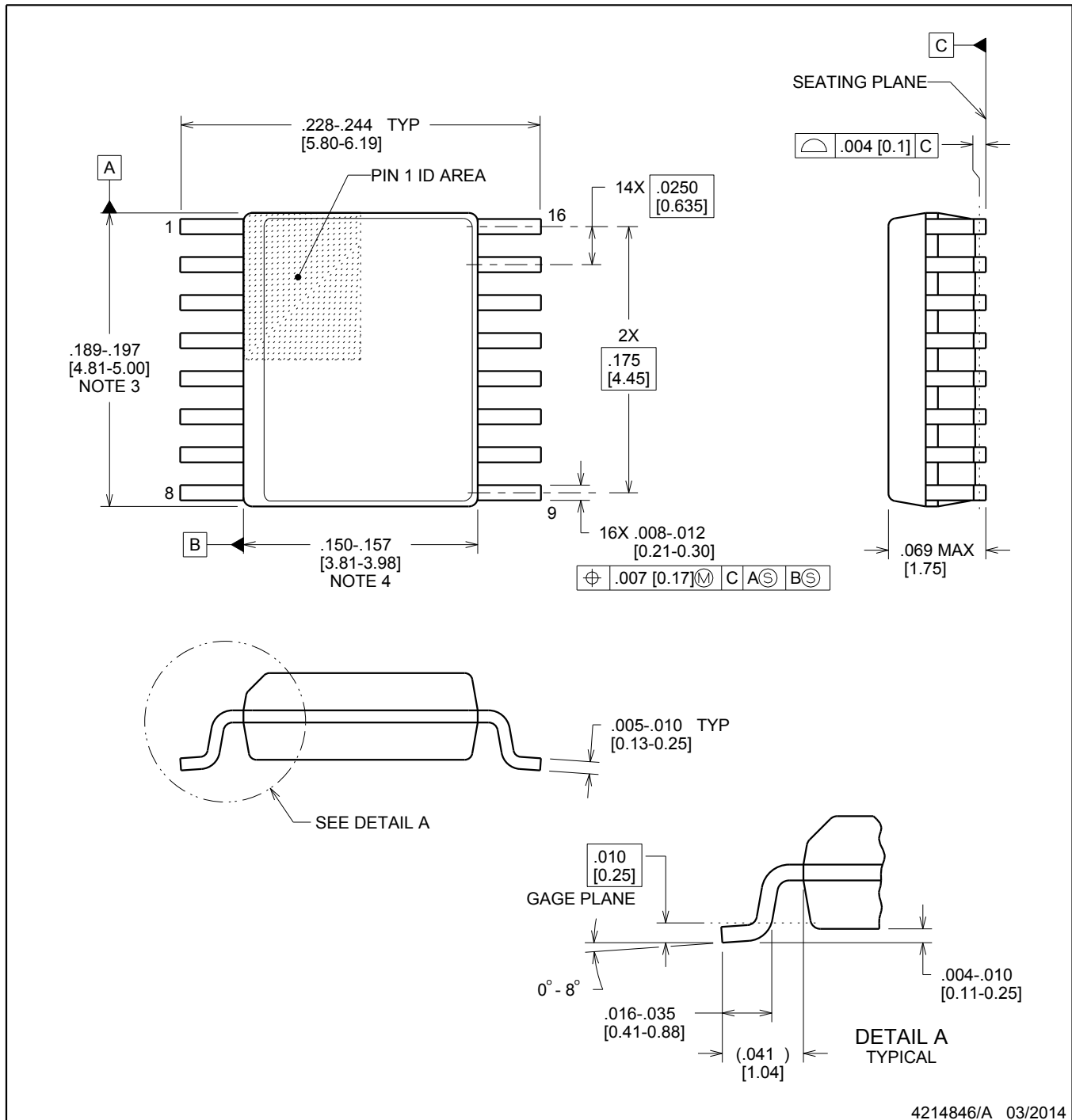


**DBQ0016A**

## PACKAGE OUTLINE

**SSOP - 1.75 mm max height**

SHRINK SMALL-OUTLINE PACKAGE



4214846/A 03/2014

### NOTES:

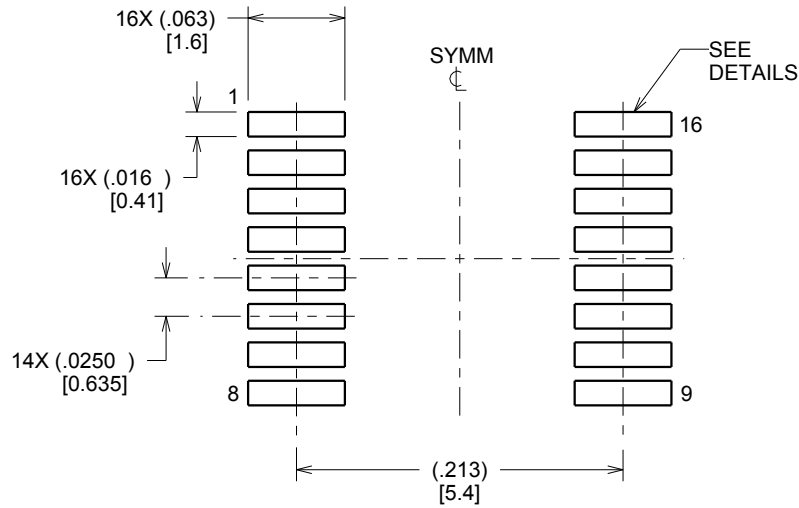
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MO-137, variation AB.

# EXAMPLE BOARD LAYOUT

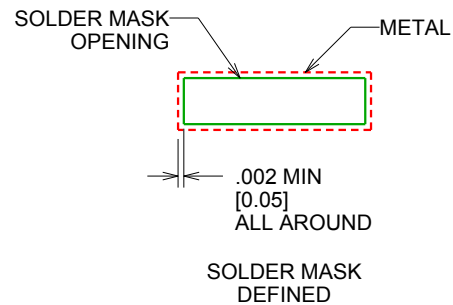
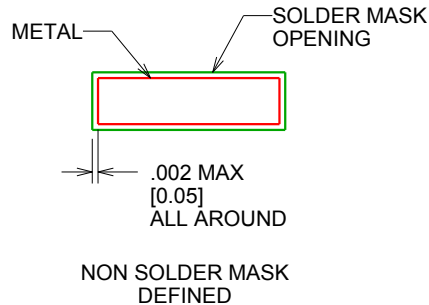
DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

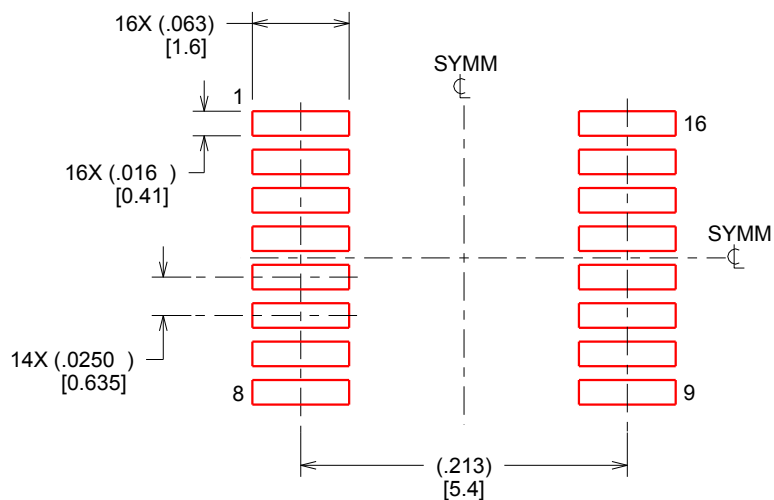
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.127 MM] THICK STENCIL  
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

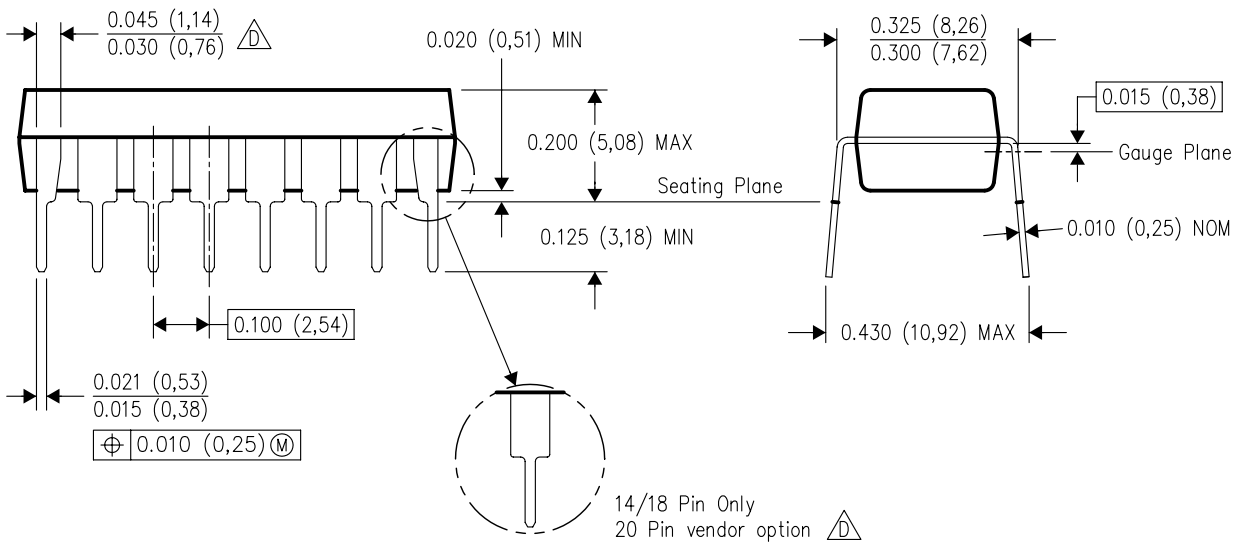
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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