THVD24xxV 具有灵活的 I/O 电源和 IEC ESD 保护功能的 ±70V 故障保护、3V 至 5.5V RS-485 收发器

1 特性

- 符合或超出 TIA/EIA-485A 和 TIA/EIA-422B 标准的要求
- 3V 至 5.5V RS-485 电源电压
- 差分输出超过 2.1V，在 5V 电源下与 PROFIBUS 兼容
- 用于逻辑信号接口的 1.65V 至 5.5V 电源
- SLR 引脚可选数据速率：
  - THVD2410V、THVD2412V：250kbps 和 1Mbps
  - THVD2450V、THVD2452V：20Mbps 和 50Mbps
- 总线 I/O 保护
  - ±70V 直流总线故障
  - ±16kV HBM ESD
  - 半双工器件：±15kV IEC 61000-4-2 接触放电和空气间隙放电
  - 全双工器件：±8kV IEC 61000-4-2 接触放电和空气间隙放电
  - ±4kV IEC 61000-4-4 快速瞬变脉冲
- 提供两种速度等级的半双工和全双工器件
- 更宽泛的工作环境温度范围： -40°C 至 125°C
- 扩展的运行共模电压范围：±25V
- 增强型接收器迟滞，可获得抗噪能力
- 低功耗
  - 低待机电源电流：< 5µA
  - 运行期间静态电流：< 5.3mA
- 适用于热插拔功能的无干扰上电/断电
- 开路、短路和空闲总线失效防护
- 热关断
- 1/8 单位负载（多达 256 个总线节点）（在 -7V 至 12V 的共模范围内）
- 小型 3mm x 3mm VSON 封装（可节省布板空间）或 14-SOIC 封装（可方便插接）

2 应用

- 电机驱动器
- 工厂自动化和控制
- HVAC 系统
- 楼宇自动化
- 电网基础设施
- 电表
- 过程分析
- 视频监控

3 说明

THVD24xxV 是具有 ±70V 故障保护功能的半双工和全双工 RS-422/RS-485 收发器，对逻辑信号接口使用 1.65V 至 5.5V 电源，对总线侧使用 3V 至 5.5V 电源。这些器件具有压摆率选择功能，因此可在两种最大速度（根据 SLR 引脚设置）下使用。

这些器件具有集成式 IEC ESD 保护，无需外部系统级保护组件。在更长的电缆敷设长度和/或存在大接地环路电压的情况下，扩展的 ±25V 输入共模范围可实现可靠的数据通信。增强型 250mV 接收器迟滞可提供高噪声抑制。此外，当输入同时开路或短路时，接收器失效防护功能可确保逻辑高电平。

封装信息

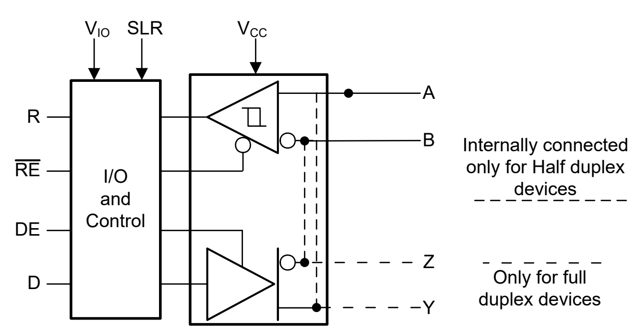
器件型号	封装[(1)]	封装尺寸（标称值）
THVD2450V THVD2410V	VSON (10)	3.00mm × 3.00mm
THVD2412V[(2)] THVD2452V[(2)]	SOIC (14)	8.65mm × 3.91mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 产品预发布

表 3-1. 器件信息

器件型号	双工	最大数据速率
THVD2410V	半双工	SLR = 高电平，250kbps SLR = 低电平，1Mbps
THVD2412V	全双工	
THVD2450V	半双工	SLR = 高电平，20Mbps SLR = 低电平，50Mbps
THVD2452V	全双工	



简化版原理图

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4 Revision History

Changes from Revision * (December 2022) to Revision A (February 2023)	**Page**
• 删除了*封装信息* 表中 THVD2410V 的“产品预发布”说明	1

5 Pin Configuration and Functions

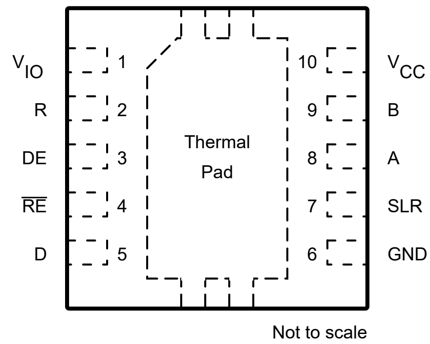


图 5-1. THVD2410V, THVD2450V 10-Pin DRC Package (VSON) Top View

表 5-1. Pin Functions

NO.	NAME	TYPE	DESCRIPTION
1	V_{IO}	Logic Supply	Supply for logic I/O signals (R, $\overline{RE}$, D, DE, and SLR)
2	R	Digital Output	Receive data output
3	DE	Digital Input	Driver enable input; integrated pull-down
4	$\overline{RE}$	Digital Input	Receiver enable input; integrated pull-up
5	D	Digital Input	Transmission data input; integrated pull-up
6	GND	Reference Potential	Local device ground
7	SLR	Digital Input	Slew rate select. For THVD2410V: Low = 1 Mbps, High = 250 kbps. Defaults to 1 Mbps if SLR is left floating. For THVD2450V: Low = 50 Mbps, High = 20 Mbps. Defaults to 50 Mbps if left floating.
8	A	Bus I/O	RS 485 bus I/O, A
9	B	Bus I/O	RS 485 bus I/O, B
10	V_{CC}	Bus Supply	Bus supply
	Thermal Pad	--	Connect to GND for optimal thermal performance

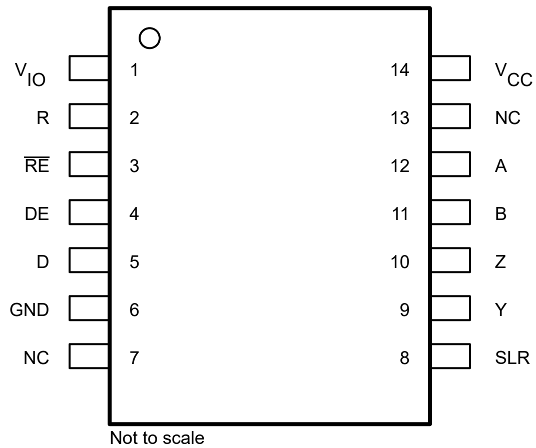


图 5-2. THVD2412V, THVD2452V 14-Pin SOIC Package (D) Top View

表 5-2. Pin functions

NO.	NAME	TYPE	DESCRIPTION
1	V_{IO}	Logic supply	1.65 V to 5.5 V supply for logic I/O signals (R, $\overline{RE}$, D, DE and SLR)
2	R	Digital output	Receive data output
3	$\overline{RE}$	Digital input	Receiver enable input; integrated pull-up
4	DE	Digital input	Driver enable input; integrated pull-down
5	D	Digital input	Transmission data input; integrated pull-up
6	GND	Reference potential	Local device ground
7	NC	No connect	Not connected internally
8	SLR	Digital input	Slew rate select. For THVD2412V: Low = 1 Mbps, High = 250 kbps. Defaults to 1 Mbps if SLR is left floating. For THVD2452V: Low = 50 Mbps, High = 20 Mbps. Defaults to 50 Mbps if left floating.
9	Y	Bus output	RS 485 driver non-inverting output
10	Z	Bus output	RS 485 driver inverting output
11	B	Bus input	RS 485 receiver inverting input
12	A	Bus input	RS 485 receiver non-inverting input
13	NC	No connect	Not connected internally
14	V_{CC}	Bus supply	3 V to 5.5 V bus supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)(2)]

		MIN	MAX	UNIT
Logic supply voltage	V_{IO}	–0.5	V_{CC} + 0.2	V
Bus supply voltage	V_{CC}	–0.5	6.5	V
Bus voltage	Range at any bus pin as differential or common-mode with respect to GND	–70	70	V
Input voltage	Range at any logic pin (D, DE, SLR or $\overline{RE}$)	–0.3	V_{IO} + 0.2	V
Receiver output current	I_O	–24	24	mA
Storage temperature	T_{stg}	–65	170	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	Bus terminals and GND	±16,000	V
			All pins except bus terminals and GND	±4,000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]		±1,500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings [IEC]

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge, Half duplex devices THVD2410V/2450V [(1)]	Contact discharge, per IEC 61000-4-2	Bus terminals and GND	±15,000	V
		Air-gap discharge, per IEC 61000-4-2	Bus terminals and GND	±15,000	
$V_{(ESD)}$	Electrostatic discharge, Full duplex devices THVD2412V/2452V	Contact discharge, per IEC 61000-4-2	Bus terminals and GND	±8,000	V
		Air-gap discharge, per IEC 61000-4-2	Bus terminals and GND	±8,000	
$V_{(EFT)}$	Electrical fast transient	Per IEC 61000-4-4	Bus terminals	±4,000	V

(1) For optimised IEC ESD performance, it is recommended to have series resistor (⩾ 50 Ω) on all logic inputs to minimize transient currents going into or out of the logic pins.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
V_{IO}	I/O supply voltage		1.65		V_{CC}	V
V_I	Input voltage at any bus terminal (separately or common mode)(1)		–25		25	V
V_{IH}	High-level input voltage (driver, driver enable, receiver enable and slew rate select inputs)		0.7*V_{IO}		V_{IO}	V
V_{IL}	Low-level input voltage (driver, driver enable, receiver enable and slew rate select inputs)		0		0.3*V_{IO}	V
V_{ID}	Differential input voltage bus pins		–25		25	V
I_O	Output current, driver		–60		60	mA
I_{OR}	Output current, receiver	V_{IO} = 1.8 V or 2.5 V	–4		4	mA
I_{OR}	Output current, receiver	V_{IO} = 3.3 V or 5 V	–8		8	mA
R_L	Differential load resistance		54	60		Ω
$1/t_{UI}$	Signaling rate	THVD2410V, THVD2412V with SLR = V_{IO}			250	kbps
		THVD2410V, THVD2412V with SLR = GND or floating			1	Mbps
		THVD2450V, THVD2452V with SLR = V_{IO}			20	Mbps
		THVD2450V, THVD2452V with SLR = GND or floating			50	Mbps
T_A	Operating ambient temperature		-40		125	°C
T_J	Junction temperature		-40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

6.5 Thermal Information

THERMAL METRIC(1)		THVD2410V THVD2450V	THVD2412V THVD2452V	UNIT
		DRC (VSON)	D (SOIC)	
		10 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.7	87.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.7	41.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.1	43.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	8.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.1	43.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.6	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Power Dissipation

PARAMETER		TEST CONDITIONS			VALUE	UNIT
P_D	Driver and receiver enabled, loopback for full duplex devices (A connected to Y, B connected to Z) V_{CC} = 5.5 V, T_A = 125 °C, square wave at 50% duty cycle	Unterminated R_L = 300 Ω, C_L = 50 pF (driver)	THVD2410V, THVD2412V	250 kbps	160	mW
			THVD2410V, THVD2412V	1Mbps	250	
			THVD2450V, THVD2452V	20Mbps	310	
			THVD2450V, THVD2452V	50 Mbps	630	
		RS-422 load R_L = 100 Ω, C_L = 50 pF (driver)	THVD2410V, THVD2412V	250 kbps	170	mW
			THVD2410V, THVD2412V	1Mbps	250	
			THVD2450V, THVD2452V	20Mbps	290	
			THVD2450V, THVD2452V	50 Mbps	570	
		RS-485 load R_L = 54 Ω, C_L = 50 pF (driver)	THVD2410V, THVD2412V	250 kbps	220	mW
			THVD2410V, THVD2412V	1Mbps	280	
			THVD2450V, THVD2452V	20Mbps	325	
			THVD2450V, THVD2452V	50 Mbps	560	

6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V , unless otherwise noted. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
$\lvert V_{OD}\rvert$	Driver differential output voltage magnitude	R_L = 60 Ω, –25 V ≤ V_{test} ≤ 25 V (See 图 7-1)		1.5	3.3		V
		R_L = 60 Ω, –25 V ≤ V_{test} ≤ 25 V, 4.5 V ≤ V_{CC} ≤ 5.5 V (See 图 7-1)		2.1	3.3		V
		R_L = 100 Ω (See 图 7-2)		2	4		V
		R_L = 54 Ω (See 图 7-2)		1.5	3.5		V
$\Delta\lvert V_{OD}\rvert$	Change in differential output voltage	R_L = 54 Ω or 100 Ω (See 图 7-2)		–50		50	mV
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω (See 图 7-2)		1	$V_{CC}/2$	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	R_L = 54 Ω or 100 Ω (See 图 7-2)		–50		50	mV
I_{OS}	Short-circuit output current	DE = V_{IO}, -70 V ≤ (V_A or V_B) ≤ 70 V, or A shorted to B (A,B are driver terminals for half duplex, Y/Z are for full duplex)		–250		250	mA
Receiver							
I_I	Bus input current	DE = 0 V, V_{CC} and V_{IO} = 0 V or 5.5 V	V_I = 12 V		90	125	μA
			V_I = 25 V		200	250	μA
			V_I = –7 V	–100	–80		μA
			V_I = –25 V	–350	–220		μA
V_{TH+}	Positive-going input threshold voltage (2)	Over common-mode range of ± 25 V		40	125	200	mV
V_{TH-}	Negative-going input threshold voltage (2)			–200	–125	-40	mV
V_{HYS}	Input hysteresis				250		mV
V_{TH_FSH}	Input fail-safe threshold			–40		40	mV
$C_{A,B}$	Input differential capacitance	Measured between A and B, f = 1 MHz			50		pF
V_{OH}	Output high voltage	I_{OH} = –8 mA, V_{IO} = 3 to 3.6 V or 4.5 V to 5.5 V		V_{IO} – 0.4	V_{IO} – 0.2		V
V_{OL}	Output low voltage	I_{OL} = 8 mA, V_{IO} = 3 to 3.6 V or 4.5 V to 5.5 V			0.2	0.4	V
V_{OH}	Output high voltage	I_{OH} = –4 mA, V_{IO} = 1.65 to 1.95 V or 2.25 V to 2.75 V		V_{IO} – 0.4	V_{IO} – 0.2		V
V_{OL}	Output low voltage	I_{OL} = 4 mA, V_{IO} = 1.65 to 1.95 V or 2.25 V to 2.75 V			0.2	0.4	V
I_{OZ}	Output high-impedance current, R pin	V_O = 0 V or V_{IO}, $\overline{RE}$ = V_{IO}		–1		1	µA
Logic							
I_{IN}	Input current (DE , SLR)	1.65 V ≤ V_{IO} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{IO}				5	µA
I_{IN}	Input current (D, $\overline{RE}$)	1.65 V ≤ V_{IO} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{IO}		–5			µA
Thermal Protection							
T_{SHDN}	Thermal shutdown threshold	Temperature rising		150	180		°C
T_{HYS}	Thermal shutdown hysteresis				10		°C
Supply							
UV_{VCC} (rising)	Rising under-voltage threshold on V_{CC}				2.3	2.6	V
UV_{VCC} (falling)	Falling under-voltage threshold on V_{CC}			1.95	2.2		V
$UV_{VCC(hys)}$	Hysteresis on under-voltage of V_{CC}				170		mV
UV_{VIO} (rising)	Rising under-voltage threshold on V_{IO}				1.4	1.6	V

6.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V , unless otherwise noted. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
UV_{VIO} (falling)	Falling under-voltage threshold on V_{IO}			1.2	1.3		V
$UV_{VIO(hys)}$	Hysteresis on under-voltage of V_{IO}				120		mV
I_{CC}	Supply current (quiescent), V_{CC} = 4.5 V to 5.5 V	Driver and receiver enabled	$\overline{RE}$ = 0 V, DE = V_{IO}, No load		3.5	5.3	mA
		Driver enabled, receiver disabled	$\overline{RE}$ = V_{IO}, DE = V_{IO}, No load		2.5	4.2	mA
		Driver disabled, receiver enabled	$\overline{RE}$ = 0 V, DE = 0 V, No load		1.8	2.4	mA
		Driver and receiver disabled	$\overline{RE}$ = V_{IO}, DE = 0 V, D = open, No load		0.1	1.2	μA
I_{CC}	Supply current (quiescent), V_{CC} = 3 V to 3.6 V	Driver and receiver enabled	$\overline{RE}$ = 0 V, DE = V_{IO}, No load		3	4.1	mA
		Driver enabled, receiver disabled	$\overline{RE}$ = V_{IO}, DE = V_{IO}, No load		2	3	mA
		Driver disabled, receiver enabled	$\overline{RE}$ = 0 V, DE = 0 V, No load		1.6	2.2	mA
		Driver and receiver disabled	$\overline{RE}$ = V_{IO}, DE = 0 V, D = open, No load		0.1	1	μA
I_{IO}	Logic supply current (quiescent), V_{IO} = 3 to 3.6 V	Driver disabled, Receiver enabled, SLR = GND	DE = 0 V, $\overline{RE}$ = 0 V, No load		4.5	8.4	μA
		Driver disabled, Receiver enabled, SLR = V_{IO}	DE = 0 V, $\overline{RE}$ = 0 V, No load		3.3	8.4	μA
		Driver disabled, Receiver disabled, SLR = GND	DE = 0 V, $\overline{RE}$ = V_{IO}, No load		0.1	1	μA
		Driver disabled, Receiver disabled, SLR = V_{IO}	DE = 0 V, $\overline{RE}$ = V_{IO}, No load		1.8	4	μA

(1) A, B are driver output and receiver input terminals for Half duplex devices; A/B are Receiver input, Y/Z are driver output terminals for Full duplex devices
(2) Under any specific conditions, V_{TH+} is assured to be at least V_{HYS} higher than V_{TH-} .

6.8 Switching Characteristics_250 kbps

250-kbps (THVD2410V, THVD2412V with SLR = V_{IO}) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V , V_{IO} = 3.3 V, unless otherwise noted. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF See 图 7-3	V_{CC} = 3 to 3.6 V, Typical at 3.3V	450	560	1200	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V	500	625	1200	ns
t_{PHL}, t_{PLH}	Propagation delay		V_{CC} = 3 to 3.6 V, Typical at 3.3V		500	720	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		540	770	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$		V_{CC} = 3 to 3.6 V, Typical at 3.3V		10	70	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		10	70	ns
t_{PHZ}, t_{PLZ}	Disable time	$\overline{RE}$ = X	See 图 7-4 and 图 7-5		40	75	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V			70	280	ns
		$\overline{RE}$ = V_{IO}			2.5	4.5	μs
t_{SHDN}	Time to shutdown	$\overline{RE}$ = V_{IO}		50		500	ns
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15 pF	See 图 7-6		7	20	ns
t_{PHL}, t_{PLH}	Propagation delay				800	1270	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$				5	45	ns
t_{PHZ}, t_{PLZ}	Disable time	DE = X			30	40	ns
$t_{PZH(1)}$	Enable time	V_{IO} = 3 V to 3.6 V; DE = V_{IO}	See 图 7-7		90	120	ns
		V_{IO} = 1.65 V to 1.95 V, DE = V_{IO}			100	130	ns
$t_{PZL(1)}$		V_{IO} = 3 V to 3.6 V; DE = V_{IO}			900	1320	ns
		V_{IO} = 1.65 V to 1.95 V; DE = V_{IO}			900	1320	ns
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time	DE = 0 V	See 图 7-8		3.3	5.4	μs
$t_{D(OFS)}$	Delay to enter fail-safe operation	C_L = 15 pF	See 图 7-9	7	11	18	μs
$t_{D(FSO)}$	Delay to exit fail-safe operation			540	800	1260	ns
t_{SHDN}	Time to shutdown	DE = 0 V	See 图 7-8	50		500	ns

(1) A, B are driver output and receiver input terminals for Half duplex devices; A/B are Receiver input, Y/Z are driver output terminals for Full duplex device

6.9 Switching Characteristics_1 Mbps

1Mbps (THVD2410V, THVD2412V with SLR = 0) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V , V_{IO} = 3.3 V, unless otherwise noted. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF See 图 7-3	V_{CC} = 3 to 3.6 V, Typical at 3.3 V	125	150	300	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V	130	160	300	ns
t_{PHL}, t_{PLH}	Propagation delay		V_{CC} = 3 to 3.6 V, Typical at 3.3 V		160	240	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		185	280	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$		V_{CC} = 3 to 3.6 V, Typical at 3.3 V		2	20	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		2	15	ns
t_{PHZ}, t_{PLZ}	Disable time	$\overline{RE}$ = X	See 图 7-4 and 图 7-5		40	95	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V			90	275	ns
		$\overline{RE}$ = V_{IO}			3	4.6	μs
t_{SHDN}	Time to shutdown	$\overline{RE}$ = V_{IO}		50		500	ns
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15 pF	See 图 7-6		7	15	ns
t_{PHL}, t_{PLH}	Propagation delay				50	85	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$				4	12.5	ns
t_{PHZ}, t_{PLZ}	Disable time	DE = X			30	40	ns
$t_{PZH(1)}$, $t_{PZL(1)}$	Enable time	V_{IO} = 3 V to 3.6 V; DE = V_{IO}	See 图 7-7		90	120	ns
		V_{IO} = 1.65 V to 1.95 V; DE = V_{IO}			90	130	ns
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time	DE = 0 V	See 图 7-8		3	4.5	μs
$t_{D(OFS)}$	Delay to enter fail-safe operation	C_L = 15 pF	See 图 7-9	7	10	18	μs
$t_{D(FSO)}$	Delay to exit fail-safe operation			27	40	60	ns
t_{SHDN}	Time to shutdown	DE = 0 V	See 图 7-8	50		500	ns

(1) A, B are driver output and receiver input terminals for Half duplex devices; A/B are Receiver input, Y/Z are driver output terminals for Full duplex device

6.10 Switching Characteristics_20 Mbps

20-Mbps (THVD2450V, THVD2452V with SLR = V_{IO}) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF See 图 7-3	V_{CC} = 3 to 3.6 V, Typical at 3.3 V	4	8	15	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V	4	7	15	ns
t_{PHL}, t_{PLH}	Propagation delay		V_{CC} = 3 to 3.6 V, Typical at 3.3 V	6	12	30	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V	4	9	26	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$		V_{CC} = 3 to 3.6 V, Typical at 3.3 V		1	3	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		1	3	ns
t_{PHZ}, t_{PLZ}	Disable time	$\overline{RE}$ = X	See 图 7-4 and 图 7-5		17	35	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V			14	39	ns
		$\overline{RE}$ = V_{IO}			3	4.5	μs
t_{SHDN}	Time to shutdown	$\overline{RE}$ = V_{IO}		50		500	ns
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15 pF	See 图 7-6		1.5	6	ns
t_{PHL}, t_{PLH}	Propagation delay	V_{IO} = 3 V to 3.6 V		25	33	58	ns
		V_{IO} = 1.65 V to 1.95 V		25	35	60	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$	C_L = 15 pF			0.5	5	ns
t_{PHZ}, t_{PLZ}	Disable time	DE = X			12	25	ns
$t_{PZH(1)}$, $t_{PZL(1)}$	Enable time	DE = V_{IO}	See 图 7-7		50	82	ns
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time	DE = 0 V	See 图 7-8		2.8	5	μs
$t_{D(OFS)}$	Delay to enter fail-safe operation	C_L = 15 pF	See 图 7-9	7	10	18	μs
$t_{D(FSO)}$	Delay to exit fail-safe operation			19	32	50	ns
t_{SHDN}	Time to shutdown	DE = 0 V	See 图 7-8	50		500	ns

(1) A, B are driver output and receiver input terminals for Half duplex devices; A/B are Receiver input, Y/Z are driver output terminals for Full duplex device

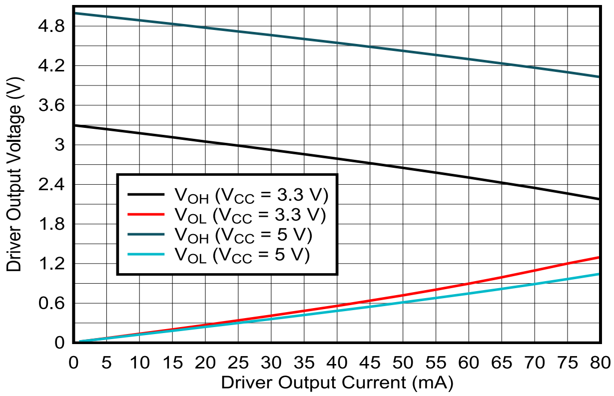
6.11 Switching Characteristics_50 Mbps

50-Mbps (THVD2450V, THVD2452V with SLR = 0) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V, unless otherwise noted. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF See 图 7-3	V_{CC} = 3 to 3.6 V, Typical at 3.3 V	1	5	7	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V	1	5	6	ns
t_{PHL}, t_{PLH}	Propagation delay		V_{IO} = 3 V to 3.6 V, V_{CC} = 3 to 3.6 V, Typical at 3.3 V	5	11	19	ns
			V_{IO} = 1.65 V to 1.95 V, V_{CC} = 3 to 3.6 V, Typical at 3.3 V	7	12	22	ns
			V_{IO} = 3 V to 3.6 V, V_{CC} = 4.5 to 5.5 V, Typical at 5 V	4	8	15	ns
			V_{IO} = 1.65 V to 1.95 V, V_{CC} = 4.5 to 5.5 V, Typical at 5 V	6	10	19	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} – t_{PLH}\|$		V_{CC} = 3 to 3.6 V, Typical at 3.3 V		1	3	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		1	3	ns
t_{PHZ}, t_{PLZ}	Disable time	$\overline{RE}$ = X	See 图 7-4 and 图 7-5		14	30	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V ; V_{IO} = 1.65 V to 1.95 V, 2.25 V to 2.75 V			20	35	ns
		$\overline{RE}$ = 0 V ; V_{IO} = 3 V to V_{CC} V			15	32	ns
		$\overline{RE}$ = V_{IO}			2.5	4.5	μs
t_{SHDN}	Time to shutdown	$\overline{RE}$ = V_{IO}		50		500	ns
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15 pF	See 图 7-6		1.5	6	ns
t_{PHL}, t_{PLH}	Propagation delay		V_{IO} = 3 V to 3.6 V, See 图 7-6	25	33	58	ns
t_{PHL}, t_{PLH}	Propagation delay		V_{IO} = 1.65 V to 1.95 V, See 图 7-6	25	35	60	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} – t_{PLH}\|$	C_L = 15 pF	See 图 7-6		0.5	5	ns
t_{PHZ}, t_{PLZ}	Disable time	DE = X			12	25	ns
$t_{PZH(1)}$, $t_{PZL(1)}$	Enable time	DE = V_{IO}	V_{IO} = 1.65 V to 1.95 V, See 图 7-7		50	82	ns
			V_{IO} = 3 V to 3.6 V, See 图 7-7		50	75	ns
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time	DE = 0 V	See 图 7-8		2.8	5	μs
$t_{D(OFS)}$	Delay to enter fail-safe operation	C_L = 15 pF	See 图 7-9	7	10	18	μs
$t_{D(FSO)}$	Delay to exit fail-safe operation			19	32	50	ns
t_{SHDN}	Time to shutdown	DE = 0 V	See 图 7-8	50		500	ns

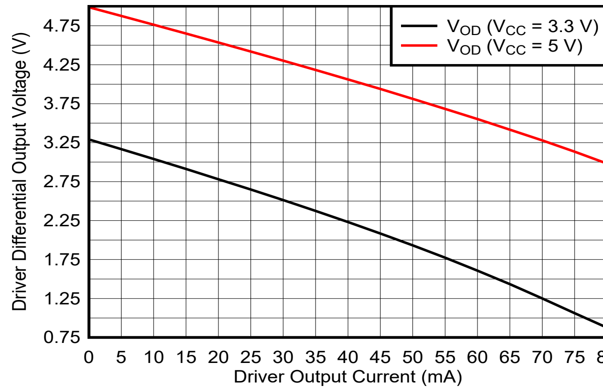
(1) A, B are driver output and receiver input terminals for Half duplex devices; A/B are Receiver input, Y/Z are driver output terminals for Full duplex device

6.12 Typical Characteristics



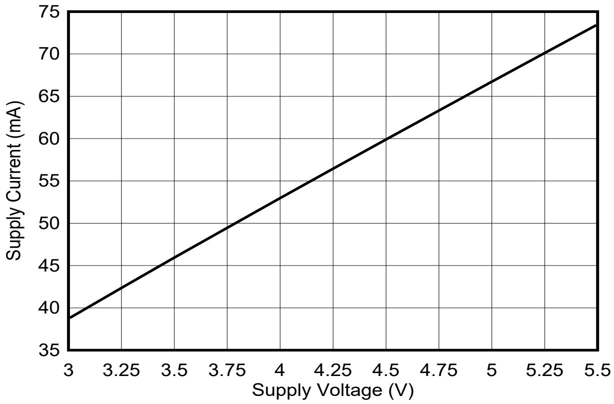
DE = V_{IO} D = GND T_A = 27 °C

图 6-1. Driver Output Voltage vs Driver Output Current



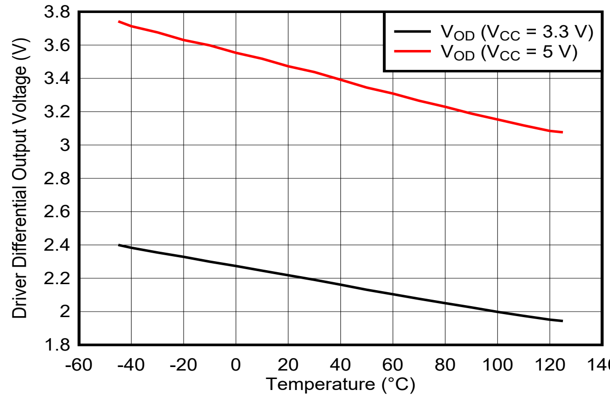
DE = V_{IO} D = GND T_A = 27 °C

图 6-2. Driver Differential Output voltage vs Driver Output Current



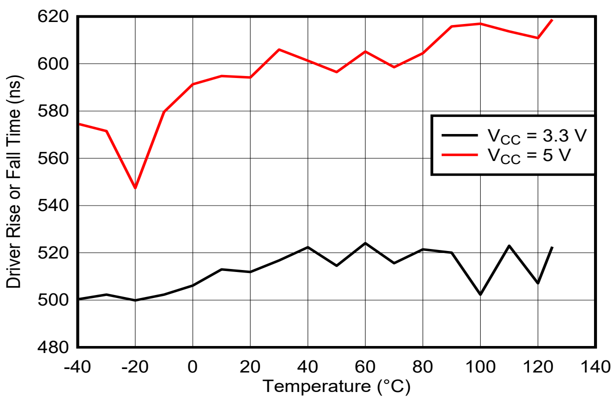
DE = D = V_{IO} R_L = 54 Ω T_A = 27 °C

图 6-3. Supply Current vs Supply Voltage



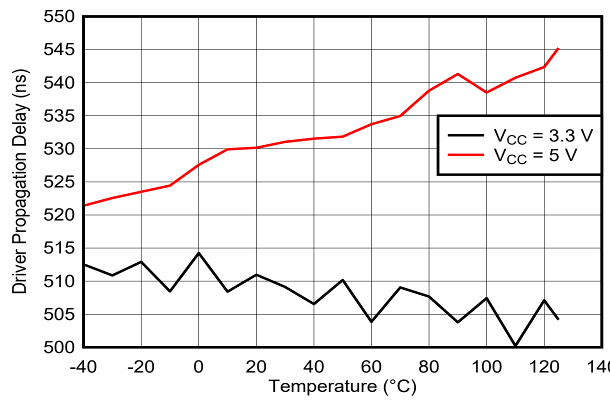
DE = D = V_{IO} R_L = 54 Ω

图 6-4. Driver differential output voltage vs Temperature



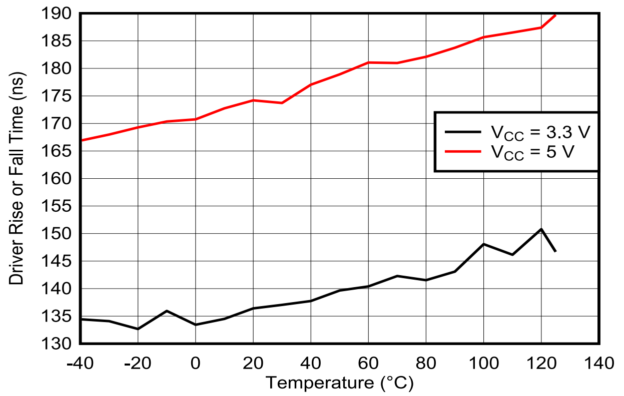
DE = V_{IO} R_L = 54 Ω C_L = 50 pF

图 6-5. THVD2410V 250kbps Driver rise or fall time vs Temperature



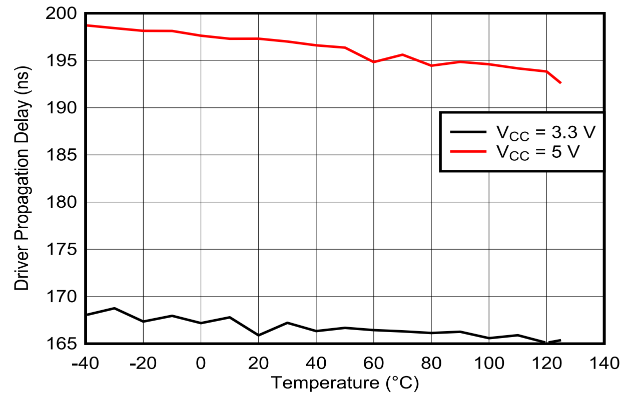
DE = V_{IO} R_L = 54 Ω C_L = 50 pF

图 6-6. THVD2410V 250kbps Driver propagation delay vs Temperature



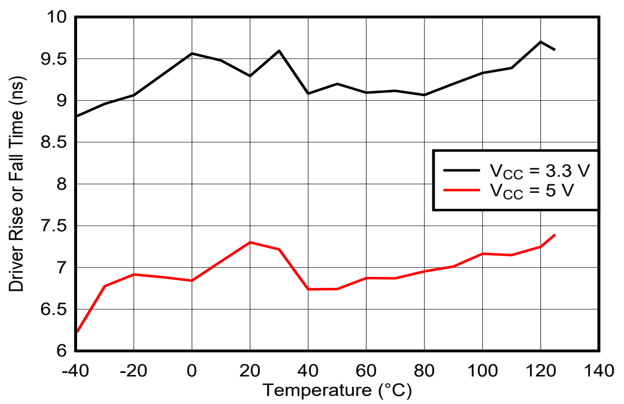
DE = V_{IO} R_L = 54 Ω C_L = 50 pF

图 6-7. THVD2410V 1Mbps Driver rise or fall time vs Temperature



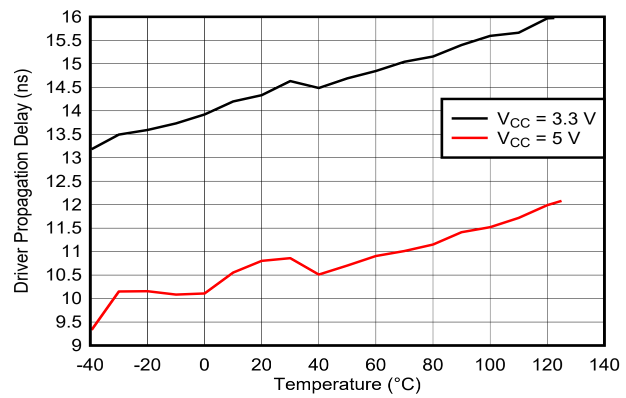
DE = V_{IO} R_L = 54 Ω C_L = 50 pF

图 6-8. THVD2410V 1Mbps Driver propagation delay vs Temperature



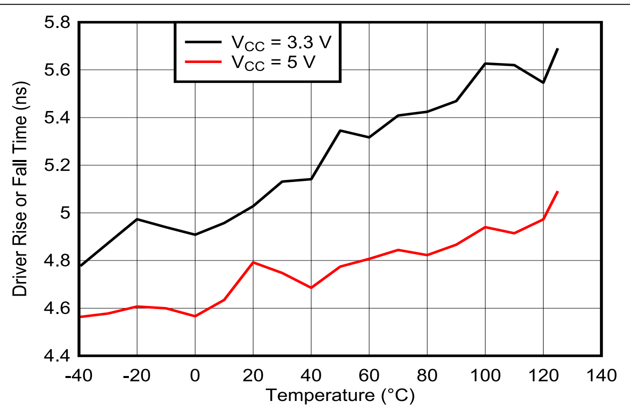
DE = V_{IO} R_L = 54 Ω C_L = 50 pF

图 6-9. THVD2450V 20Mbps Driver rise or fall time vs Temperature



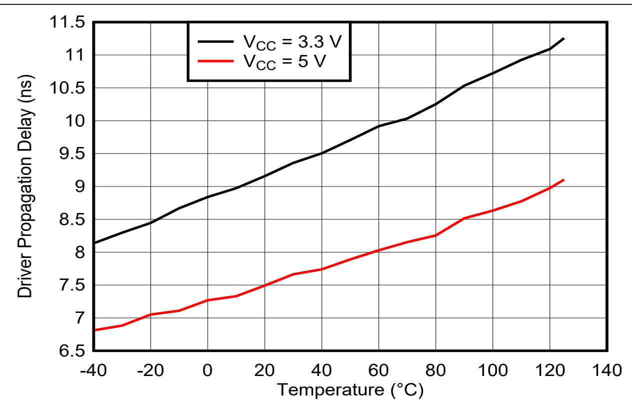
DE = V_{IO} R_L = 54 Ω C_L = 50 pF

图 6-10. THVD2450V 20Mbps Driver propagation delay vs Temperature



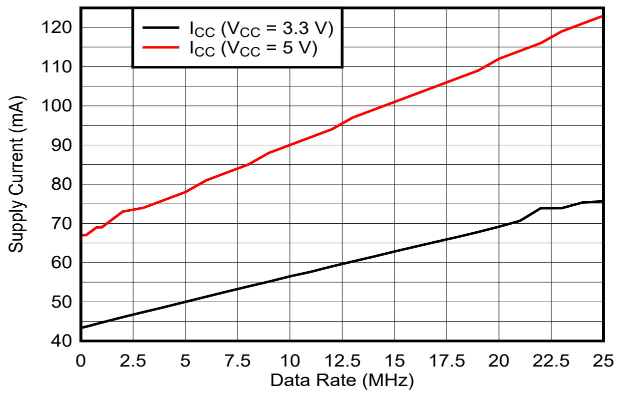
DE = V_{IO} R_L = 54 Ω C_L = 50 pF

图 6-11. THVD2450V 50Mbps Driver rise or fall time vs Temperature



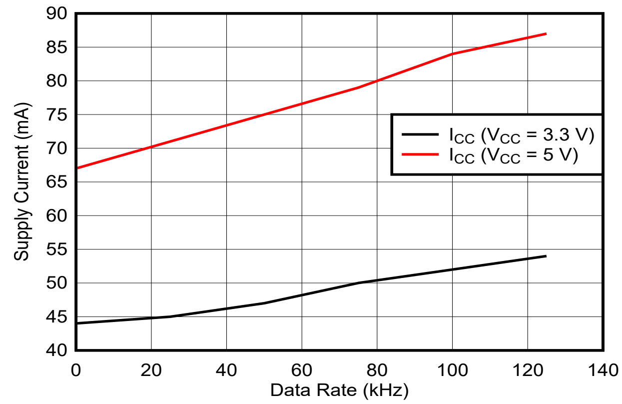
DE = V_{IO} R_L = 54 Ω C_L = 50 pF

图 6-12. THVD2450V 50Mbps Driver propagation delay vs Temperature



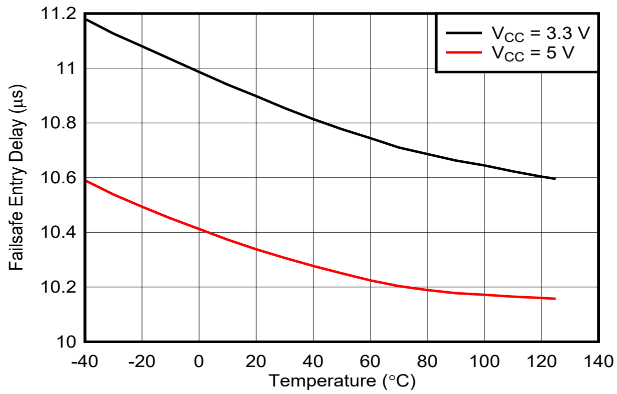
DE = V_{IO} R_L = 54 Ω T_A = 27 °C

图 6-13. THVD2450V Supply Current vs Signal Rate



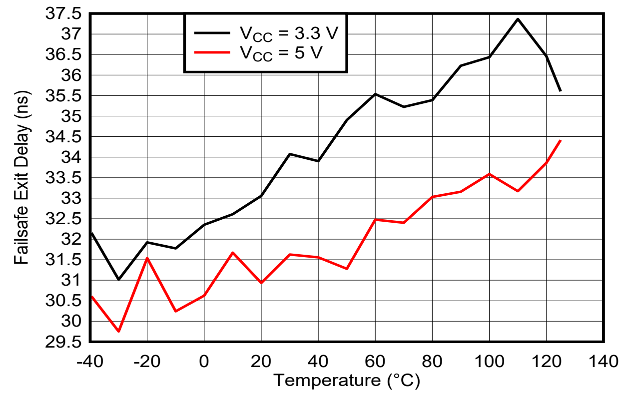
DE = V_{IO} R_L = 54 Ω T_A = 27 °C

图 6-14. THVD2410V Supply Current vs Signal Rate



SLR = GND $\overline{RE}$ = GND $C_{L(RXD)}$ = 15 pF

图 6-15. Failsafe entry delay vs Temperature



SLR = GND $\overline{RE}$ = GND $C_{L(RXD)}$ = 15 pF

图 6-16. Failsafe exit delay vs Temperature

7 Parameter Measurement Information

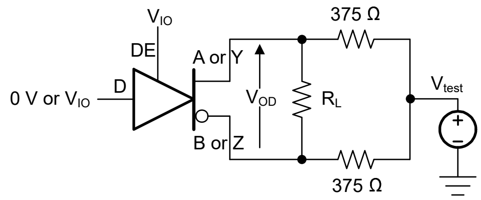


图 7-1. Measurement of Driver Differential Output Voltage With Common-Mode Load

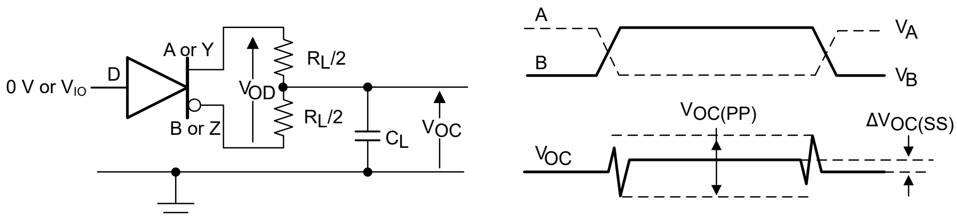


图 7-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

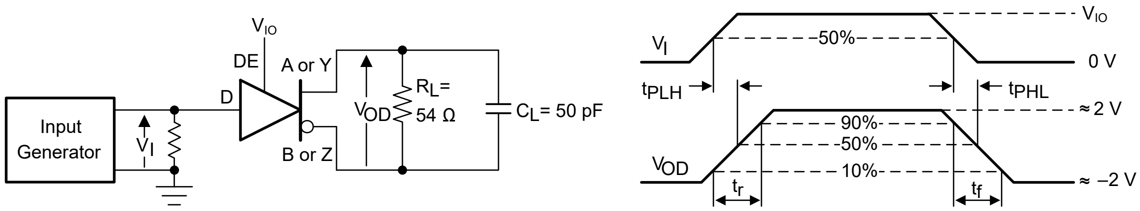


图 7-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

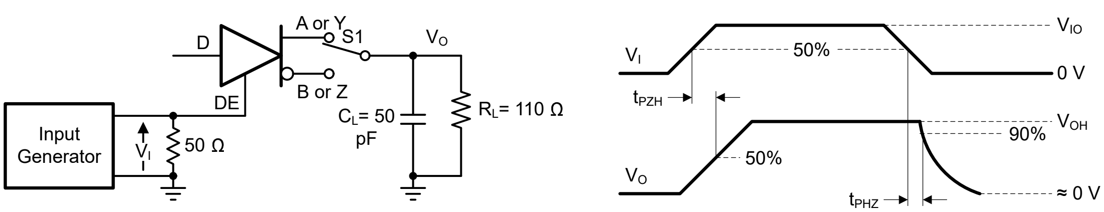


图 7-4. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

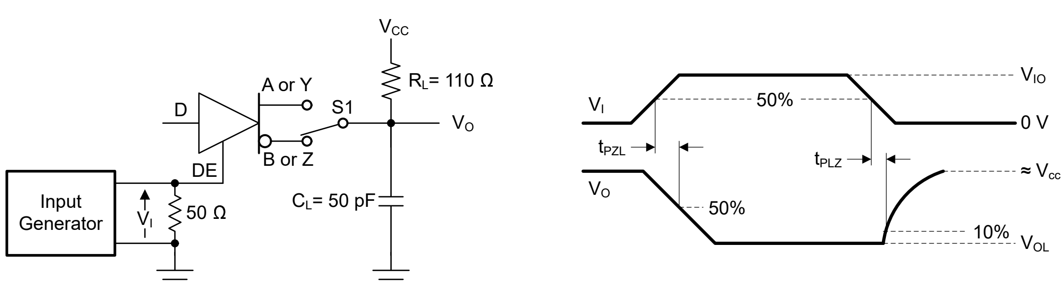


图 7-5. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

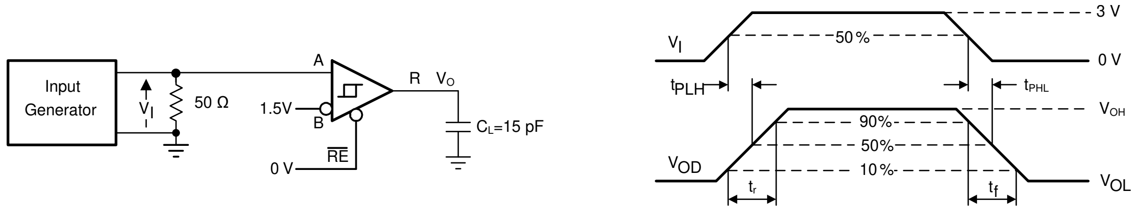


图 7-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

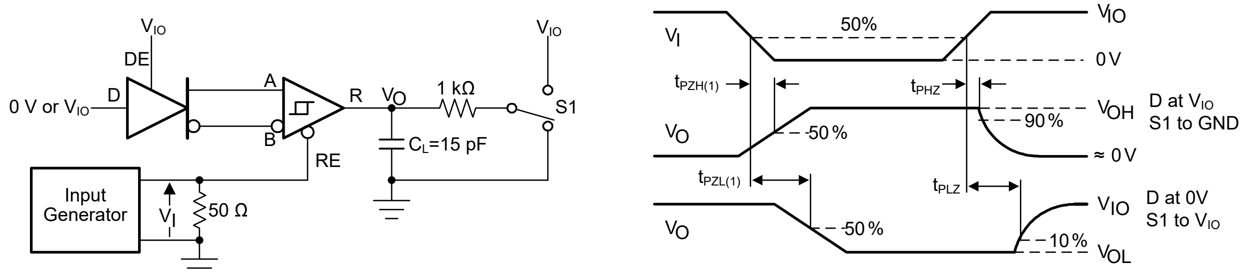


图 7-7. Measurement of Receiver Enable/Disable Times With Driver Enabled

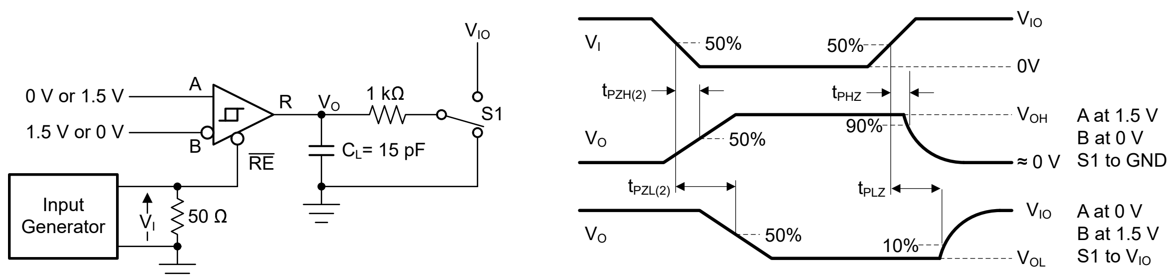


图 7-8. Measurement of Receiver Enable Times With Driver Disabled

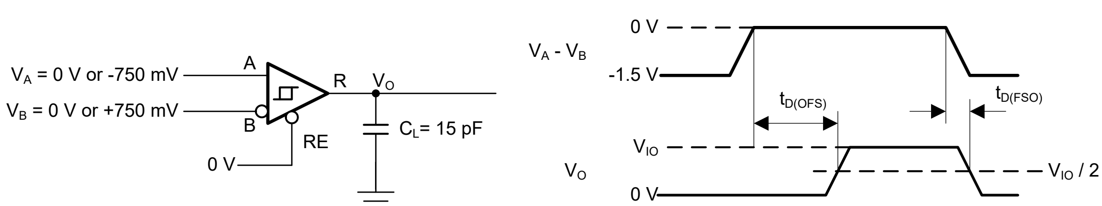


图 7-9. Measurement of Fail-Safe Delay

8 Detailed Description

8.1 Overview

THVD24xxV are ±70 V bus fault-protected, ±25V common-mode voltage range capable half and full-duplex RS-485 transceivers. The devices have active-high driver enable and active-low receiver enable logic. Each device has SLR pin which allows it to be used for two different maximum speed settings. This is beneficial as customers can qualify one device and use it in two different end-applications. The devices also have flexible I/O supply pin V_{IO} which enables digital interface voltage range, from 1.65 V to 5.5 V, different from bus voltage supply 3 V to 5.5 V.

8.2 Functional Block Diagrams

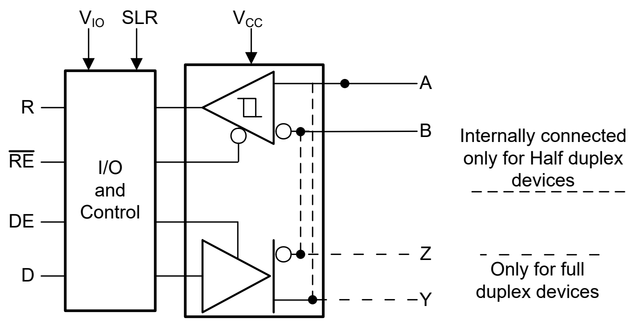


图 8-1. THVD2410 and THVD2450 Block Diagram

8.3 Feature Description

8.3.1 ±70 V Fault Protection

THVD24xxV transceivers have extended bus fault protection compared to standard RS-485 devices. Transceivers that operate in rugged industrial environments are often exposed to voltage transients greater than the -7 V to +12 V defined by the TIA/EIA-485A standard. To protect against such conditions, the generic RS-485 devices with lower absolute maximum ratings requires expensive external protection components. To simplify system design and reduce overall system cost, THVD24xxV devices are protected up to ±70 V without the need for any external components.

8.3.2 Integrated IEC ESD and EFT Protection

Internal ESD protection circuits protect the transceivers against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to ±15 kV contact and air discharge (for half-duplex devices) and up to ±8 kV contact and air discharge (for full-duplex devices). Bus structures also protect against electrical fast transients (EFT) according to IEC 61000-4-4 for up to ±4 kV. With careful system design, integrated bus structures can enable EFT Criterion A at the system level (minimum to no data loss when transient noise is present).

8.3.3 Driver Overvoltage and Overcurrent Protection

The THVD24xxV drivers are protected against any DC supply shorts in the range of -70 V to +70 V. The devices internally limit the short circuit current to ±250 mA in order to comply with the TIA/EIA-485A standard. In addition, a fold-back current limiting circuit further reduces the driver short circuit current to less than ±5 mA if the output fault voltage exceeds |±25 V|.

All devices feature thermal shutdown protection that disables the driver and the receiver if the junction temperature exceeds the T_{SHDN} threshold due to excessive power dissipation.

8.3.4 Enhanced Receiver Noise Immunity

The differential receivers of THVD24xxV feature fully symmetric thresholds to maintain duty cycle of the signal even with small input amplitudes. In addition, 250 mV (typical) hysteresis provides noise immunity. When the device is in slew rate limited mode of 250 kbps, typical 700 ns of glitch filter in receiver signal chain prevents high frequency noise pulses from the bus to appear on R pin.

8.3.5 Receiver Fail-Safe Operation

The receivers are fail-safe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the receiver outputs a fail-safe logic high state if the input amplitude stays for longer than $t_{D(OFS)}$ at less than $|V_{TH\_FSH}|$.

8.3.6 Low-Power Shutdown Mode

Driving DE low and $\overline{RE}$ high for longer than 500 ns puts the devices into the shutdown mode. If either DE goes high or $\overline{RE}$ goes low, the counters reset. The devices does not enter the shutdown mode if the enable pins are in disable state for less than 50 ns. This feature prevents the devices from accidentally going into shutdown mode due to skew between DE and $\overline{RE}$.

8.4 Device Functional Modes

When the driver enable pin, DE, is logic high (H), the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low (L), the output states reverse: B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant (X). The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (Z= high-impedance) by default. The D pin has an internal pull-up resistor to V_{IO}, thus, when left open while the driver is enabled, output A turns high and B turns low.

表 8-1. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-}, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

表 8-2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

表 8-3 shows SLR (slew rate select) pin functionality. SLR has intergated pull-down, so the device remains in higher speed mode until SLR is pulled high which limits the slew rate and puts the device in slower speed mode.

表 8-3. SLR pin control

Device	Functionality w.r.t SLR pin
THVD2410V, THVD2412V	SLR = Low or floating: Both transmitter (TX) and receiver (RX) maximum speed is 1 Mbps SLR = High: Both TX and RX maximum speed is limited to 250 kbps
THVD2450V, THVD2452V	SLR = Low or floating: Both transmitter (TX) and receiver (RX) maximum speed is 50 Mbps SLR = High: Both TX and RX maximum speed is limited to 20 Mbps

Table shows the device behavior in undervoltage scenarios:

表 8-4. Supply Function Table

V_{CC}	V_{IO}	Driver Output	Receiver Output
> $UV_{VCC(rising)}$	> $UV_{VIO(rising)}$	Determined by DE and D inputs	Determined by $\overline{RE}$ and A-B
< $UV_{VCC(falling)}$	> $UV_{VIO(rising)}$	High impedance	High impedance
> $UV_{VCC(rising)}$	< $UV_{VIO(falling)}$	High impedance	High impedance
< $UV_{VCC(falling)}$	< $UV_{VIO(falling)}$	High impedance	High impedance

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI' s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

THVD24xxV are fault-protected, half- and full-duplex RS-485 transceivers commonly used for asynchronous data transmissions. For these devices, the driver and receiver enable pins allow for the configuration of different operating modes.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

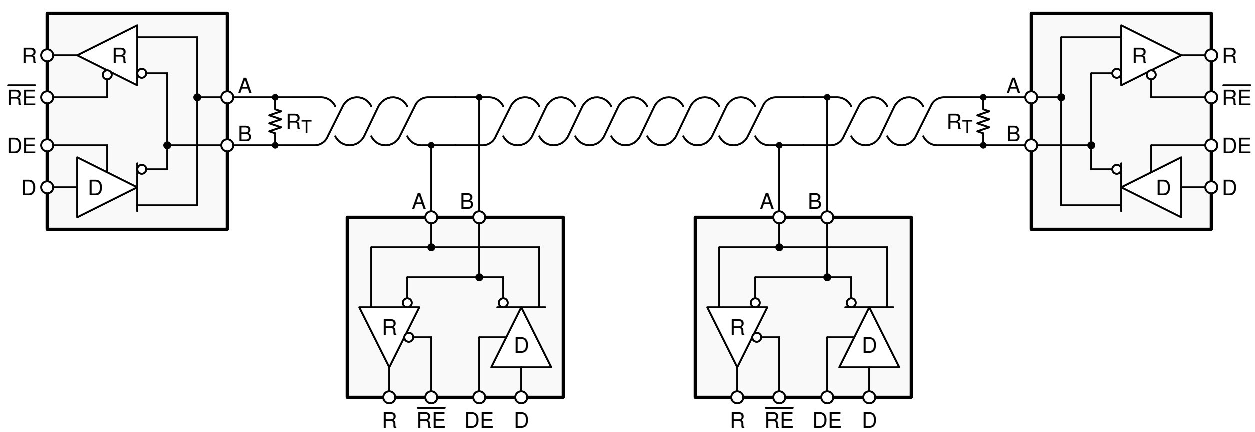


图 9-1. Typical RS-485 Network With Half-Duplex Transceivers

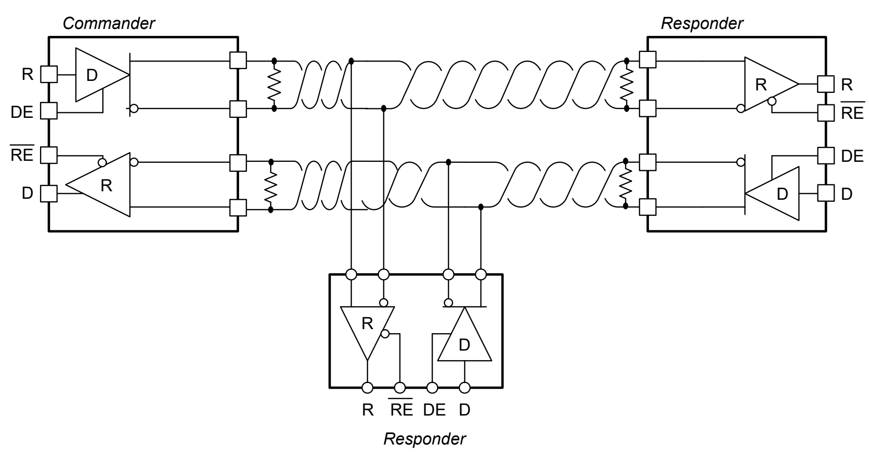


图 9-2. Typical RS-485 Network with Full-Duplex transceivers

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the short the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

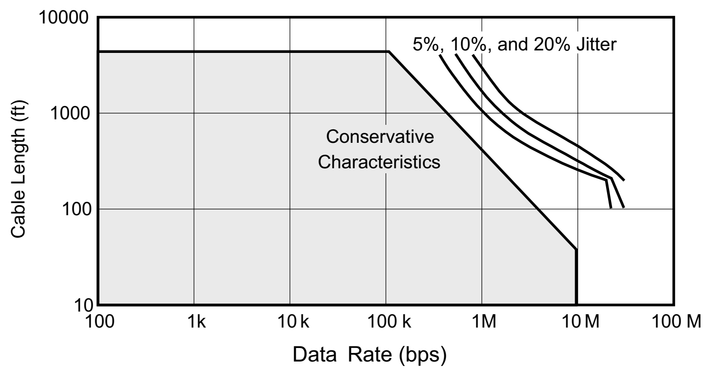


图 9-3. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (that is, 50 Mbps for the THVD24xxV) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections of varying phase as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 方程式 1.

$$L_{(STUB)} \leqslant 0.1 \times t_r \times v \times c \qquad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the THVD24xxV devices consist of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible for a limited common mode range of - 7 V to 12 V.

9.2.1.4 Transient Protection

The bus pins of the THVD24xxV transceivers include on-chip ESD protection against ±16-kV HBM and ±15-kV IEC 61000-4-2 contact discharge for half-duplex devices ±8-kV for full-duplex devices. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method.

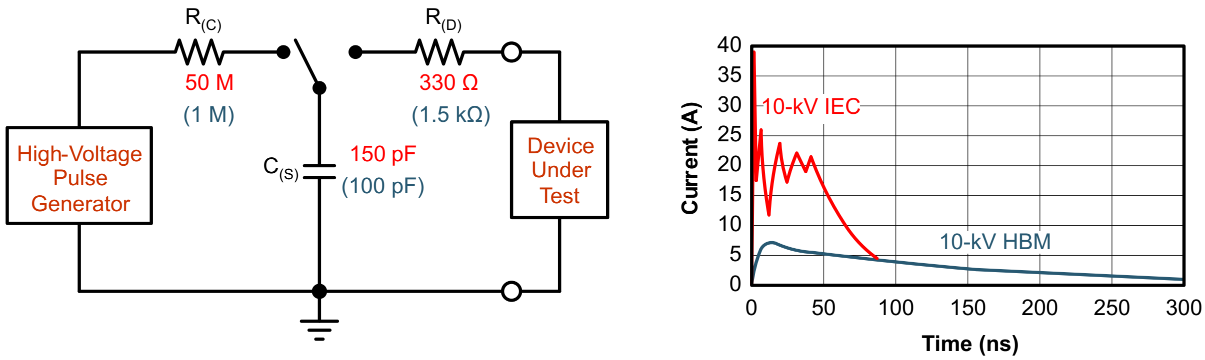


图 9-4. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

图 9-5 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left side of the diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which exceeds the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right side of the diagram shows the pulse power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are may occur in power generation and power-grid systems.

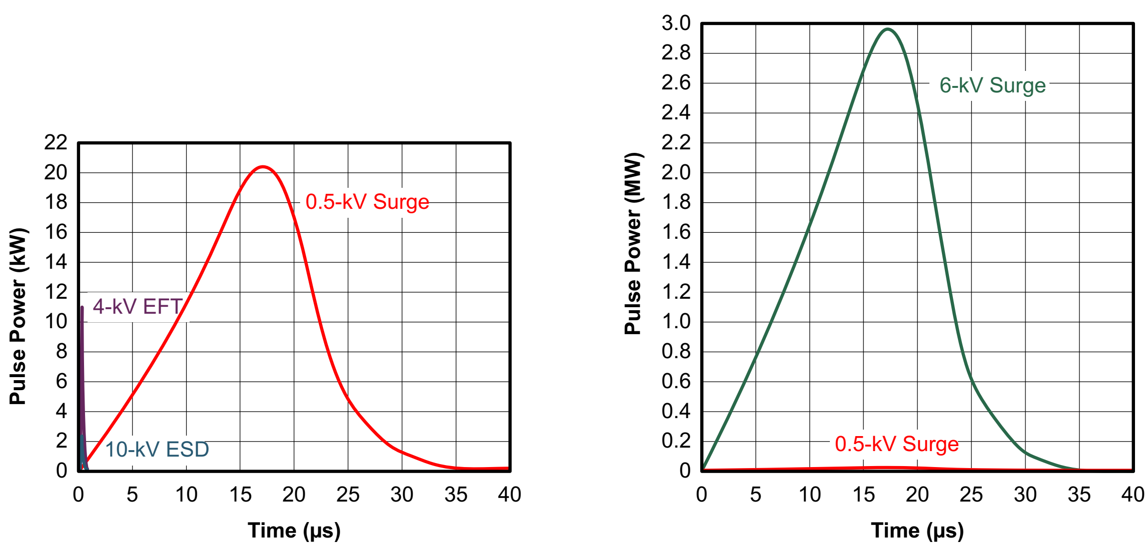


图 9-5. Power Comparison of ESD, EFT, and Surge Transients

For surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. 图 9-6 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

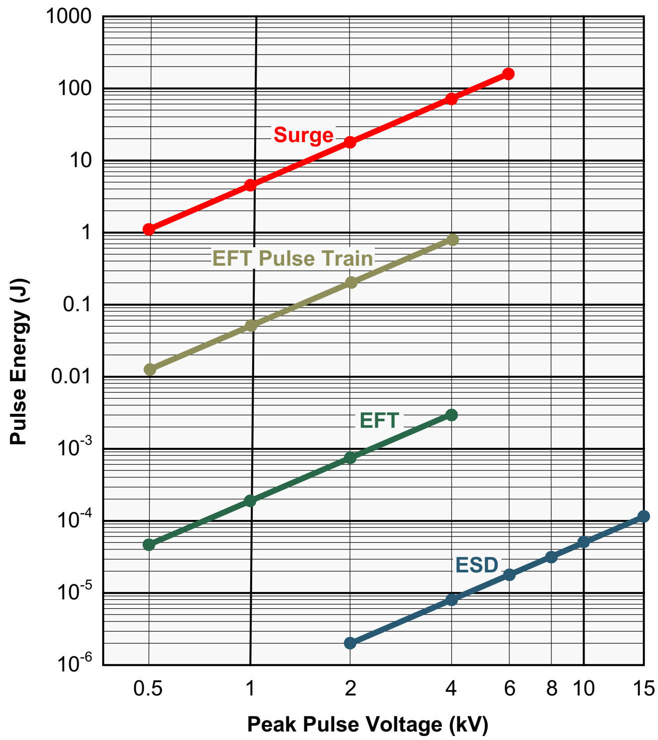


图 9-6. Comparison of Transient Energies

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9.2.2 Detailed Design Procedure

图 9-7 suggests a protection circuit against 1 kV surge (IEC 61000-4-5) transients. 表 9-1 shows the associated bill of materials. SMAJ30CA TVS diodes are rated to operate up to 30 V. This makes sure the protection diodes do not conduct if a direct RS-485 bus shorts to 24-V DC industrial power rail.

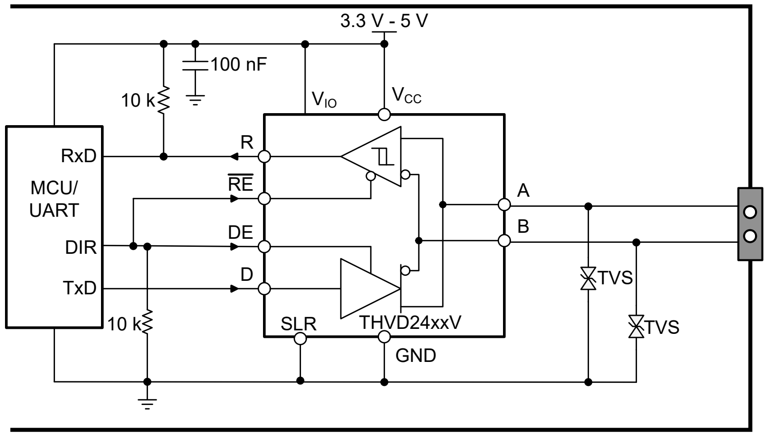


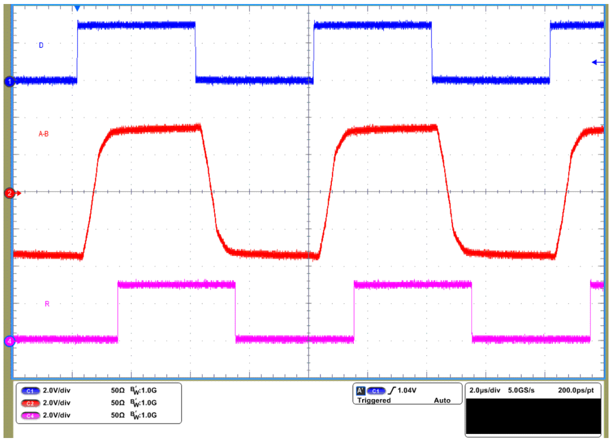
图 9-7. Transient Protection Against Surge Transients for Half-Duplex Devices

表 9-1. Components List

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER(1)
XCVR	RS-485 transceiver	THVD2410V or THVD2450V	TI
TVS	Bidirectional 400-W transient suppressor	SMAJ30CA	Littelfuse

(1) See 节 10.1

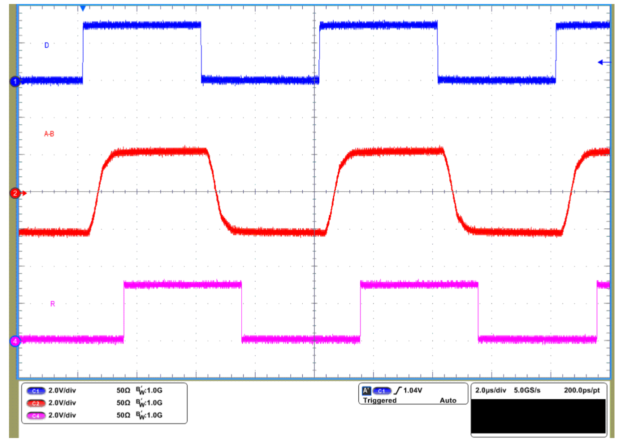
9.2.3 Application Curves



50% duty square wave on D pin at 250 kbps

SLR = V_{IO} R_L = 54 Ω DE = V_{IO}

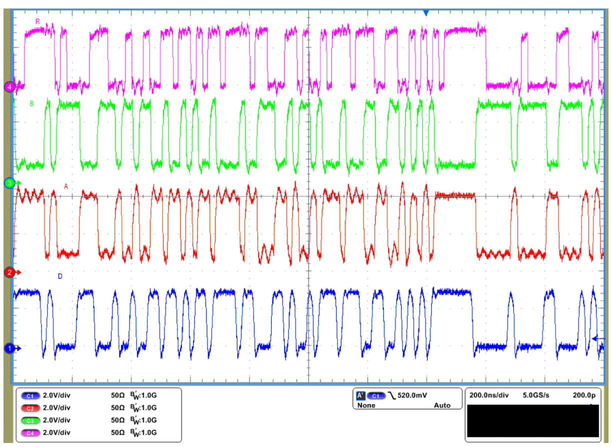
图 9-8. THVD2410V Waveforms at V_{CC} = 5 V



50% duty square wave on D pin at 250 kbps

SLR = V_{IO} R_L = 54 Ω DE = V_{IO}

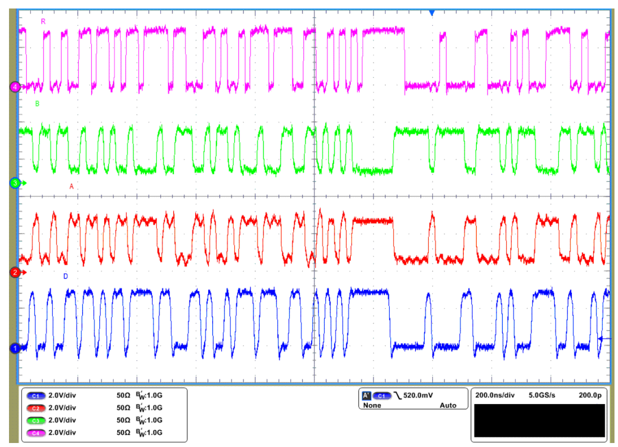
图 9-9. THVD2410V Waveforms at V_{CC} = 3.3 V



Random (PRBS7) data on D pin at 50 Mbps

SLR = GND R_L = 54 Ω DE = V_{IO}

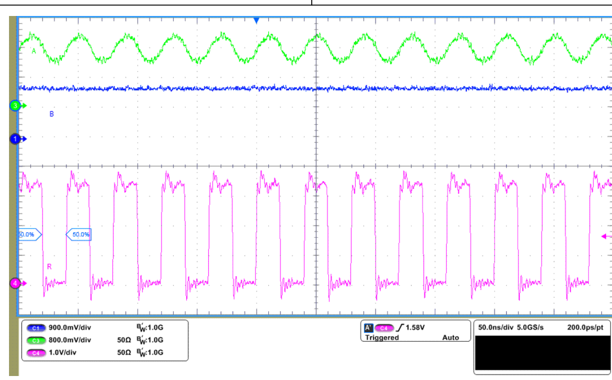
图 9-10. THVD2450V Waveforms at V_{CC} = 5 V



Random (PRBS7) data on D pin at 50 Mbps

SLR = GND R_L = 54 Ω DE = V_{IO}

图 9-11. THVD2450V Waveforms at V_{CC} = 3.3 V



A pin given ±200mV V_{ID} with DC offset of 1.5 V

$\overline{RE}$ = GND B pin at 1.5 V

图 9-12. THVD2450V Receiver Waveform with ±200 mV V_{ID}

9.3 Power Supply Recommendations

For reliable operation at all data rates and supply voltages, each supply should be decoupled with a minimum of 100 nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

9.4 Layout

9.4.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF decoupling capacitors as close as possible to the V_{CC} and V_{IO} pins of transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1-kΩ to 10-kΩ pull-up and pull-down resistors for enable/SLR lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof resistors into the A/Y and B/Z bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.

9.4.2 Layout Example

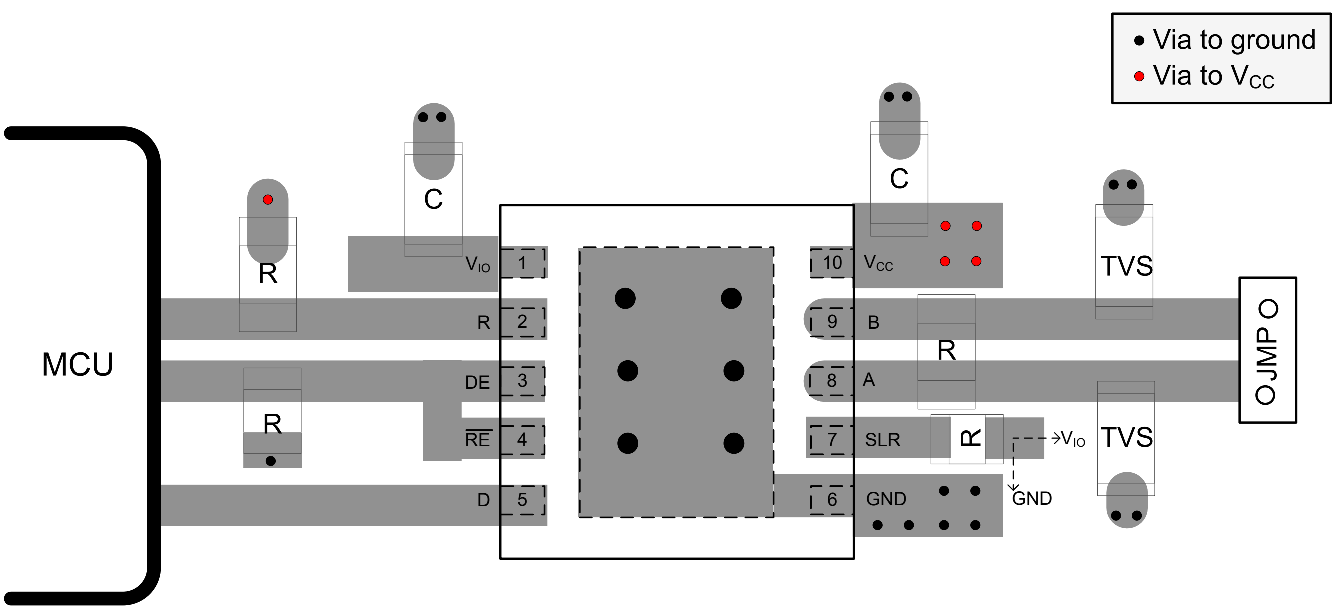


图 9-13. Half-Duplex Layout Example

10 Device and Documentation Support

10.1 Device Support

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTHVD2412VDR	ACTIVE	SOIC	D	14	250	TBD	Call TI	Call TI	-40 to 125		Samples
PTHVD2452VDR	ACTIVE	SOIC	D	14	250	TBD	Call TI	Call TI	-40 to 125		Samples
THVD2410VDRCR	ACTIVE	VSON	DRC	10	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2410	Samples
THVD2450VDRCR	ACTIVE	VSON	DRC	10	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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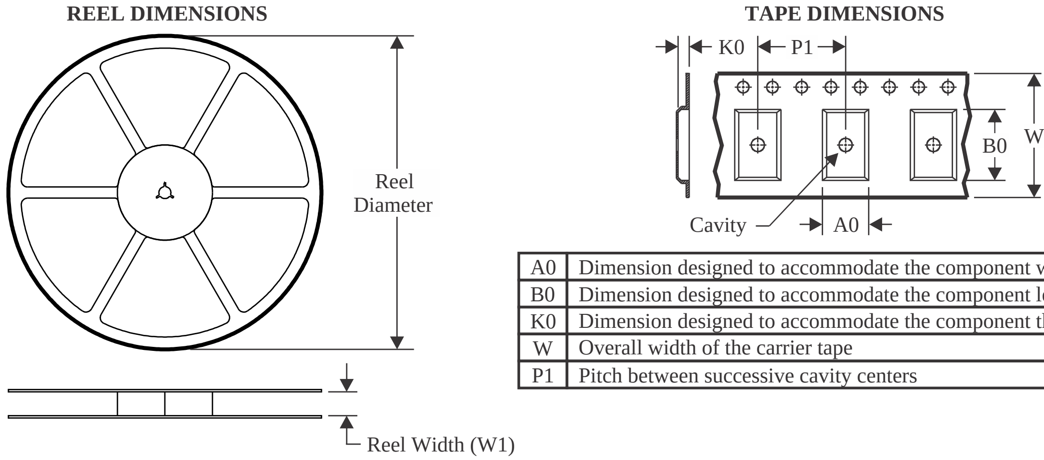
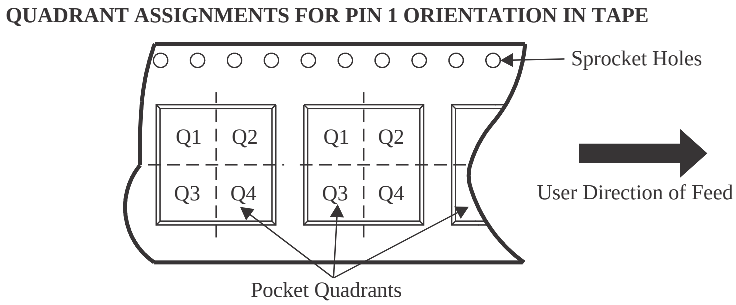


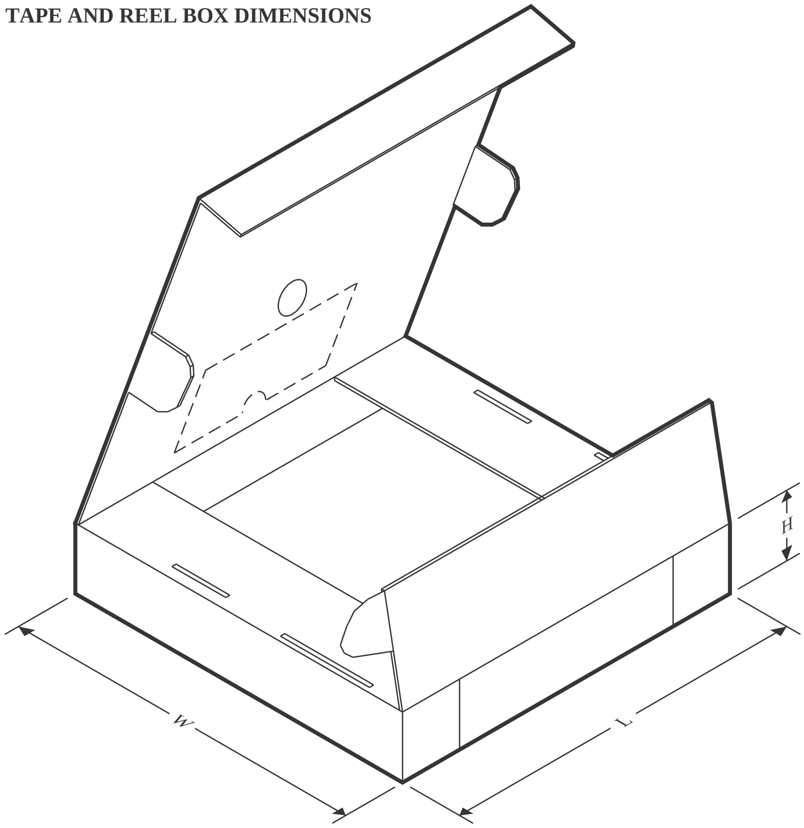
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD2410VDRCR	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THVD2450VDRCR	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

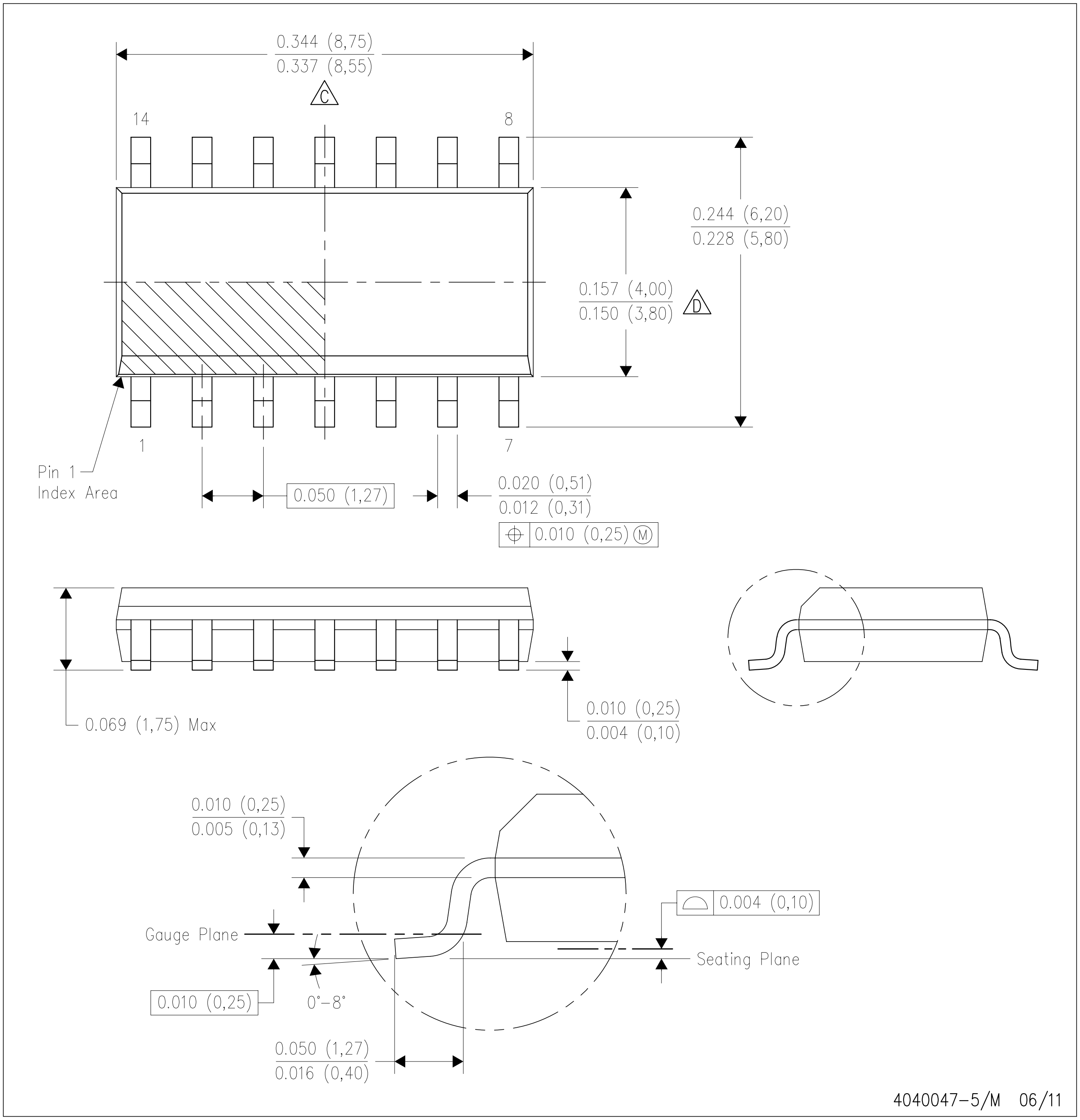
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD2410VDRCR	VSON	DRC	10	5000	367.0	367.0	35.0
THVD2450VDRCR	VSON	DRC	10	5000	367.0	367.0	35.0

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

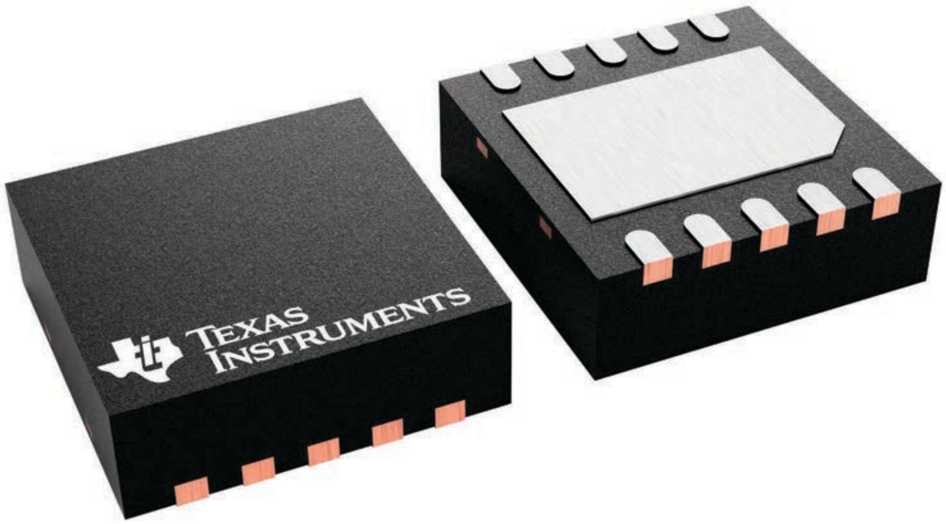
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

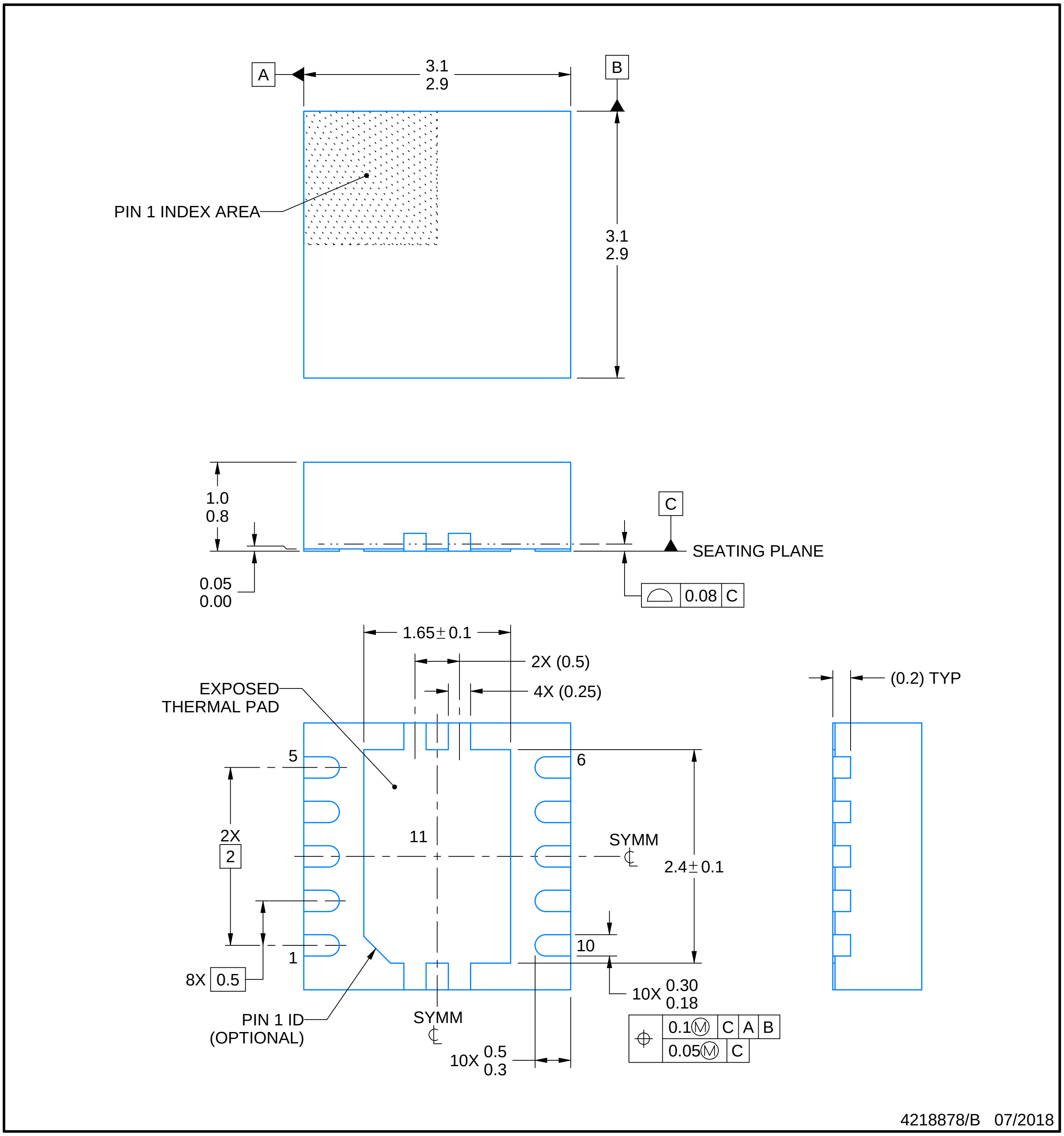


PACKAGE OUTLINE

DRC0010J

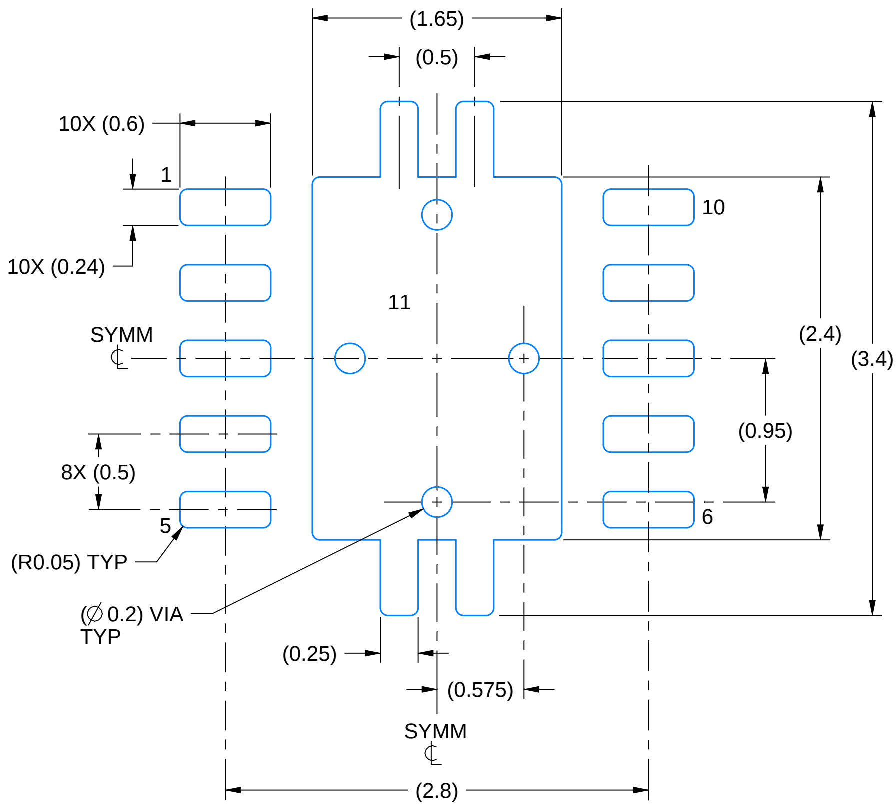
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

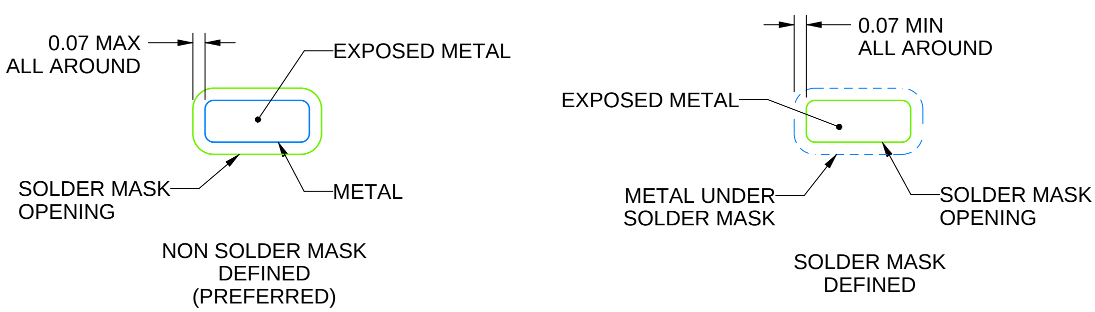


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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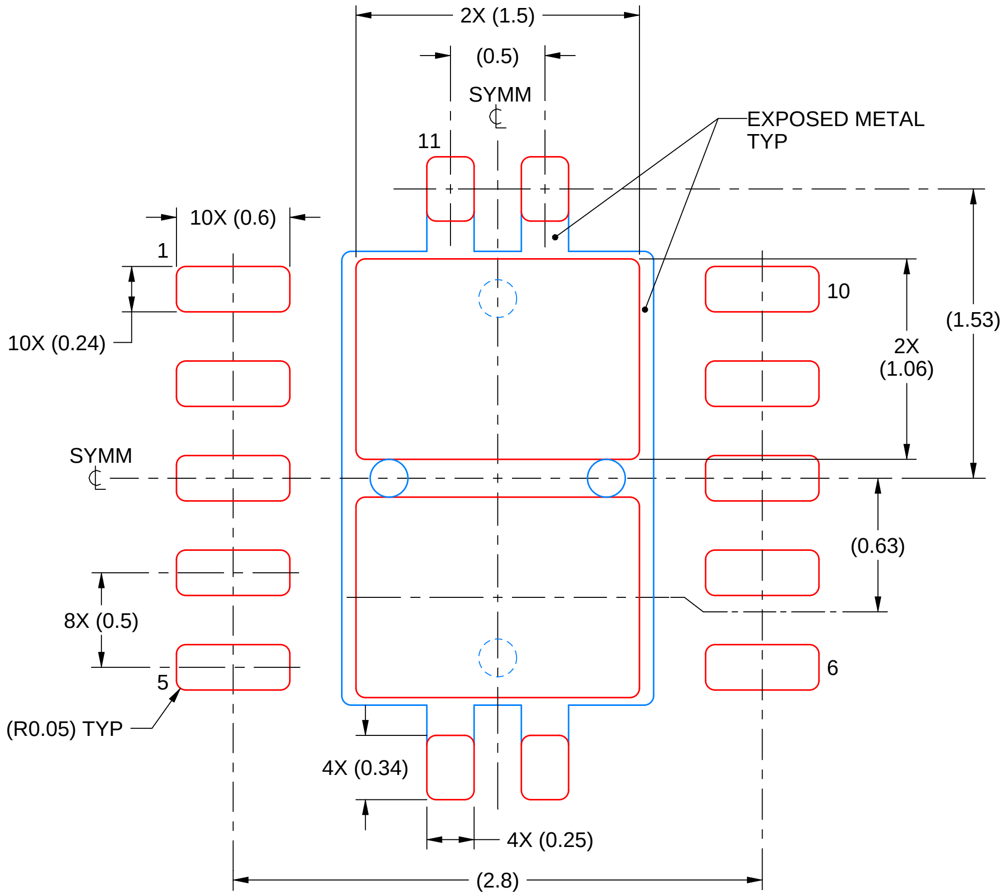
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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