TLV3801-Q1 具有 LVDS 输出的 225ps 高速比较器

1 特性

- 低传播延迟：225 ps
- 低过驱动分散：5 ps
- 静态电流：20mA
- 高切换频率：3GHz/6Gbps
- 窄脉宽检测功能：240ps
- LVDS 输出
- 分离输入和输出接地基准
- 单电源电压：2.7V 至 5.25V
- 低输入失调电压：±0.5mV
- 内部迟滞：2mV
- 封装：TLV3801（8 引脚 WSON）

2 应用

- 激光雷达中的距离感测
- 飞行时间传感器
- 示波器和逻辑分析仪中的高速触发器功能
- 高速差分线路接收器
- 无人机视觉

3 说明

TLV3801-Q1 是具有宽电源电压范围和 3GHz 超高切换频率的 225ps 高速比较器。这些器件具有 2.7V 至 5.25V 的单电源工作电压范围和 2.7V 至 5.25V 的双电源工作电压范围，采用业界通用的小型封装承载所有特性，是激光雷达、差分线路接收器应用以及测试和测量系统的理想选择。

TLV3801-Q1 具有 5ps 的强大输入过驱性能，并且能够检测仅 240ps 的窄脉冲宽度。这些器件具有输入过驱可实现较小传播延迟变化，并且能够检测窄脉冲，是飞行时间 (ToF) 应用（例如工厂自动化和无人机视觉）的理想选择。

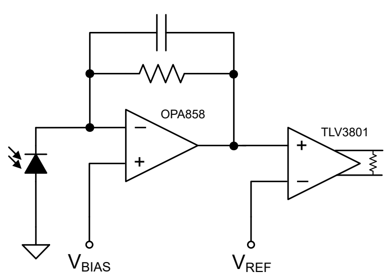
TLV3801-Q1 的低压差分信号 (LVDS) 输出有助于提高数据吞吐量并优化功耗。同样，互补输出有助于通过抑制每个输出上的共模噪声来降低 EMI。LVDS 输出旨在驱动和直接连接可接受标准 LVDS 输入（例如大多数 FPGA 和 CPU）的其他应用下游器件。

TLV3801-Q1 采用 8 引脚 WSON 封装，因此非常适合空间敏感型应用，例如光学传感器模块。

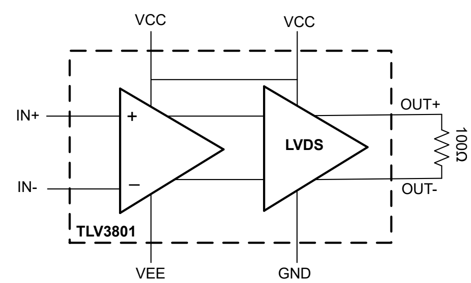
器件信息

器件型号	封装 (1)	封装尺寸（标称值）
TLV3801-Q1	WSON (8)	2.00mm × 2.00mm

1.如需了解所有可订购封装，请参阅数据表末尾的可订购产品附录。



TLV3801 光学接收器电路



功能方框图

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
October 2022	*	Initial Release

5 Pin Configuration and Functions

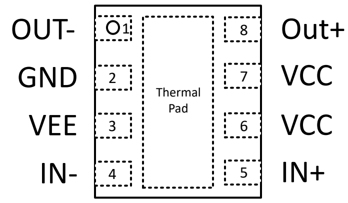


图 5-1. WSON Package 8-Pin DSG Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	TLV3801		
IN+	5	I	Non-inverting input
IN –	4	I	Inverting input
OUT+	8	O	Non-inverting output
OUT –	1	O	Inverting output
V_{EE}	3	I	Negative power supply (If using single supply, connect to GND)
V_{CC}	6, 7	I	Positive power supply
GND	2	I	Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

	MIN	MAX	UNIT
Supply voltage: (V_{CC} – V_{EE}) and (V_{CC} – GND) [(2)]	–0.3	5.5	V
Input pins (IN+, IN–) from V_{EE} [(3)]	V_{EE} – 0.3	V_{CC} + 0.3	V
Current into input pins (IN+, IN–)	–10	10	mA
Output (OUT+, OUT–)	GND	V_{CC}	V
OUT+ to OUT–	–0.5	+0.5	V
Current into output pins (OUT+, OUT–)		10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) VEE less than or equal to GND
(3) Input terminals are diode-clamped to V_{EE} and V_{CC}

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), , per AEC Q100-002[(1)]	±2000	V
		Charged-device model (CDM), per AEC Q100-0111	±1000	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Thermal Information

THERMAL METRIC[(1)]		TLV3801-Q1 DSG (WSON) 8-pin	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	69.4	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	95.7	°C/W
R_{qJB}	Junction-to-board thermal resistance	36.2	°C/W
y_{JT}	Junction-to-top characterization parameter	3.5	°C/W
y_{JB}	Junction-to-board characterization parameter	36.0	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	9.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Single supply operation: V_{CC} – V_{EE} with V_{EE} = GND	2.7	5.25	V
Split supply operation: V_{CC} – V_{EE} with V_{EE} < GND	2.7	5.25	V
Split supply operation: V_{CC} – GND with V_{EE} < GND	2.4	5.25	V
Input voltage range	V_{EE} + 1.5	V_{CC} + 0.1	V
Differential Input voltage range	–1.5	+1.5	V
Ambient temperature, T_A	–40	125	°C

6.5 Electrical Characteristics

For V_{CC} = 3.3 V, V_{EE} = GND = 0, V_{CM} = 2.5 V at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Input Characteristics						
V_{OS}	Input offset voltage	T_A = –40°C to +125°C	–5[1]	±0.5	+5[1]	mV
V_{HYS}	Input hysteresis voltage			2		mV
$V_{CM\text{-}Range}$	Common-mode voltage range	Single Supply: V_{EE} = GND V_{CC} – V_{EE} = 2.7 V to 5.25 V T_A = –40 °C to +125°C	V_{EE} + 1.5		V_{CC}	V
$V_{CM\text{-}Range}$	Common-mode voltage range	Split Supply: V_{EE} < GND V_{CC} – V_{EE} = 2.7 V to 5.25 V and V_{CC} – GND = 2.4 V to 5.25 V T_A = –40 °C to +125°C	V_{EE} + 1.5		V_{CC}	V
CMRR	Common mode rejection ratio	V_{CM} = V_{EE} + 1.5V to V_{CC}		80		dB
PSRR	Power supply rejection ratio	Single Supply: V_{EE} = GND V_{CC} – V_{EE} = 2.7 V to 5.25 V		80		dB
PSRR	Power supply rejection ratio	Split Supply: V_{EE} < GND V_{CC} – V_{EE} = 2.7 V to 5.25 V and V_{CC} – GND = 2.4 V to 5.25 V		80		dB
I_B	Input bias current	T_A = –40 °C to +125 °C	–10	±1	10	μA
I_{OS}	Input offset current	T_A = –40 °C to +125 °C	–4	±0.1	4	μA
C_{IC}	Input capacitance, common mode			1		pF
DC Output Characteristics						
V_{OCM}	Output common mode voltage	V_{CC} - GND ⩾ 2.6 V T_A = –40℃ to +125℃	1.125	1.25	1.375	V
	Output common mode voltage	V_{CC} - GND < 2.6 V T_A = –40℃ to +125℃	0.92	1.2	1.29	V
ΔV_{OCM}	Output common mode voltage mismatch	T_A = –40℃ to +125℃	–30		30	mV
V_{OCM_PP}	Peak-to-Peak output common mode voltage			50		mVpp
V_{OD}	Differential output voltage	T_A = –40℃ to +125℃	250	350	450	mV
ΔV_{OD}	Differential output voltage mismatch	T_A = –40℃ to +125℃			30	mV
Power Supply						
I_Q	Quiescent current per comparator	T_A = –40°C to +125°C		20	26.6	mA
AC Characteristics						
t_{PD}	Propagation delay	$V_{OVERDRIVE}$ = 50 mV, $V_{UNDERDRIVE}$ = 50 mV, 50 MHz Squarewave		225		ps
Tempco of t_{PD}	Temperature Coefficient of propagation delay			±0.2		ps/℃
t_{PD_SKEW}	Propagation delay skew	$V_{OVERDRIVE}$ = 50mV, $V_{UNDERDRIVE}$ = 50 mV, 50 MHz Squarewave		±2.5		ps
$t_{CM\_DISPERSION}$	Common mode dispersion	V_{CM} varied from V_{CM} (min) to V_{CM} (max)		2		ps

6.5 Electrical Characteristics (continued)

For V_{CC} = 3.3 V, V_{EE} = GND = 0, V_{CM} = 2.5 V at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{OD\_DISPERSION}$	Overdrive dispersion	Overdrive varied from 20 mV to 100 mV		5		ps
$t_{OD\_DISPERSION}$	Overdrive dispersion	Overdrive varied from 10 mV to 1 V		15		ps
$t_{UD\_DISPERSION}$	Underdrive dispersion	Overdrive varied from 20 mV to 100 mV		7		ps
$t_{UD\_DISPERSION}$	Underdrive dispersion	Overdrive varied from 10 mV to 1 V		10		ps
t_R	Rise time	20% to 80%		135		ps
t_F	Fall time	80% to 20%		135		ps
f_{TOGGLE}	Input toggle frequency	V_{IN} = 200 mV_{PP} Sine Wave, V_{OD} = 550 mV		2.3		GHz
f_{TOGGLE}	Input toggle frequency	V_{IN} = 200 mV_{PP} Sine Wave, 50% Output swing		3		GHz
TR	Toggle Rate	V_{IN} = 200 mV_{PP} Sine Wave, V_{OD} = 550 mV		4.6		Gbps
TR	Toggle Rate	V_{IN} = 200 mV_{PP} Sine Wave, 50% Output swing		6		Gbps
PulseWidth	Minimum allowed input pulse width	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV PW_{OUT} = 90% of PW_{IN}		240		ps

(1) Ensured by charaterization

6.6 Timing Diagrams

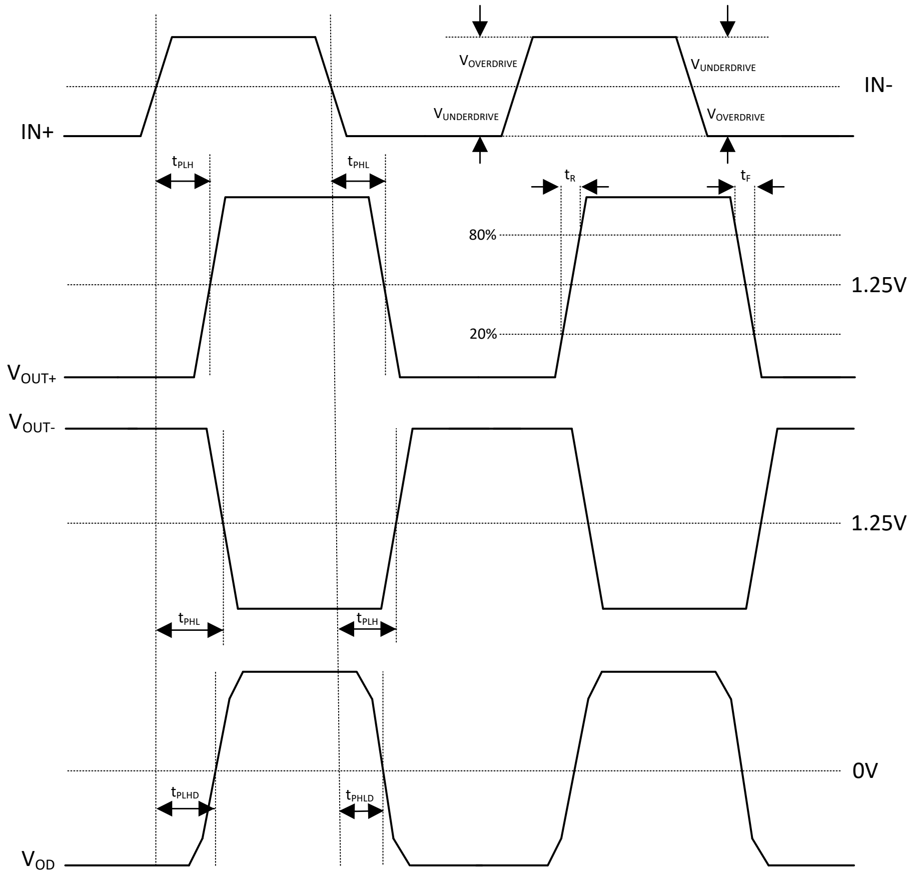


图 6-1. General Timing Diagram

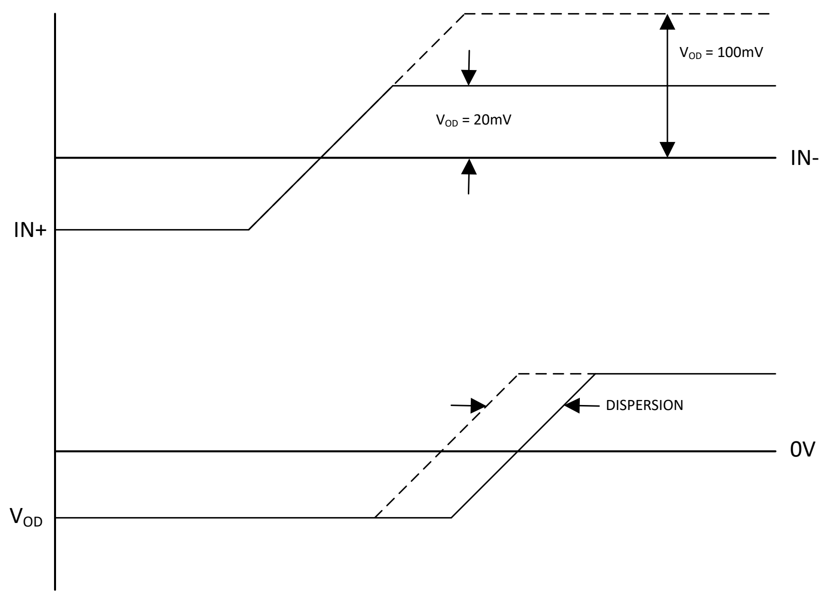


图 6-2. Overdrive Dispersion

6.7 Typical Characteristics

At T_A = 25°C, V_{CC} - V_{EE} = 3.3 V to 5 V while V_{EE} = GND = 0, V_{CM} = 2.5 V, and input overdrive/underdrive = 50 mV, unless otherwise noted.

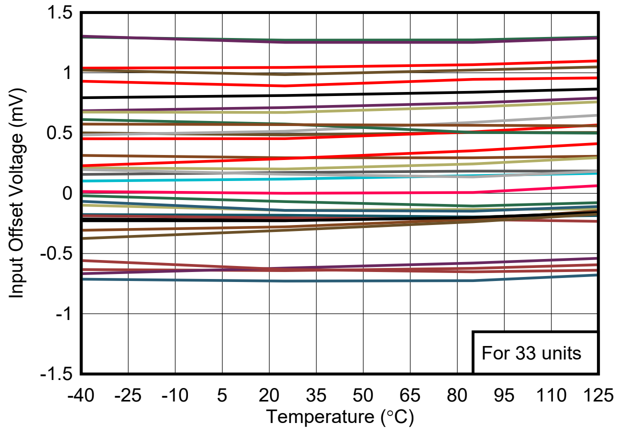


图 6-3. Offset vs. Temperature

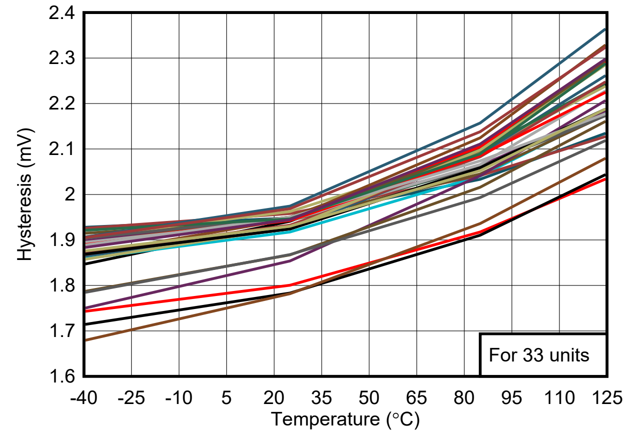


图 6-4. Hysteresis vs. Temperature

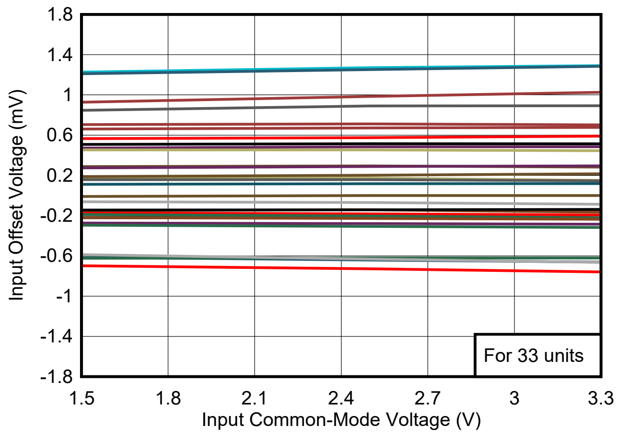


图 6-5. Offset vs. Common-Mode, 3.3 V

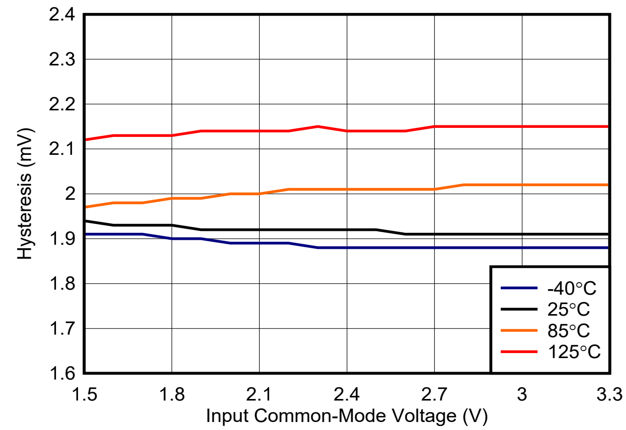


图 6-6. Hysteresis vs. Common-Mode, 3.3 V

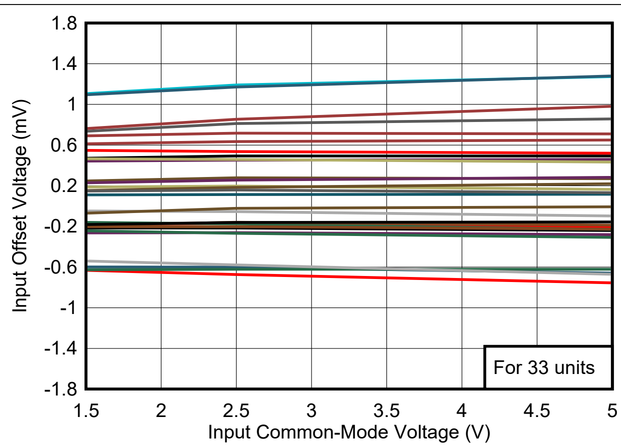


图 6-7. Offset vs. Common-Mode, 5 V

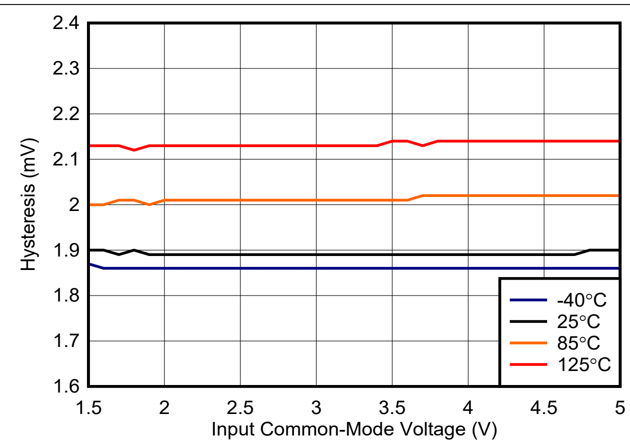


图 6-8. Hysteresis vs. Common-Mode, 5 V

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 3.3 V to 5 V while V_{EE} = GND = 0, V_{CM} = 2.5 V, and input overdrive/underdrive = 50 mV, unless otherwise noted.

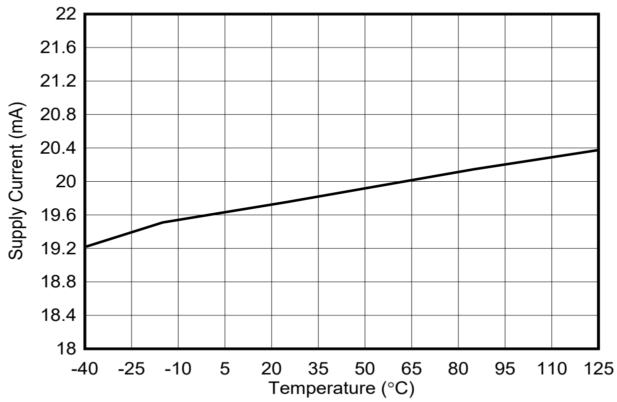


图 6-9. Supply Current vs. Temperature, Output Low

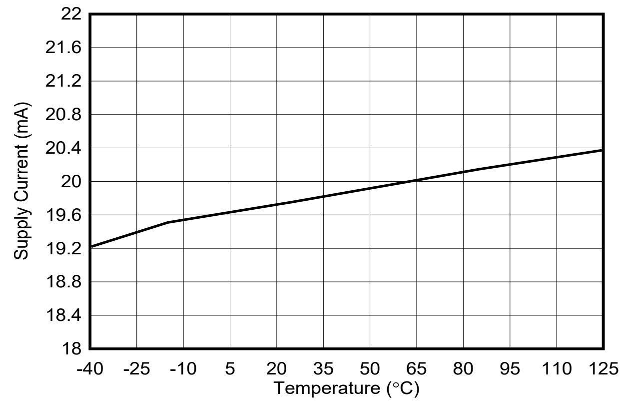


图 6-10. Supply Current vs. Temperature, Output High

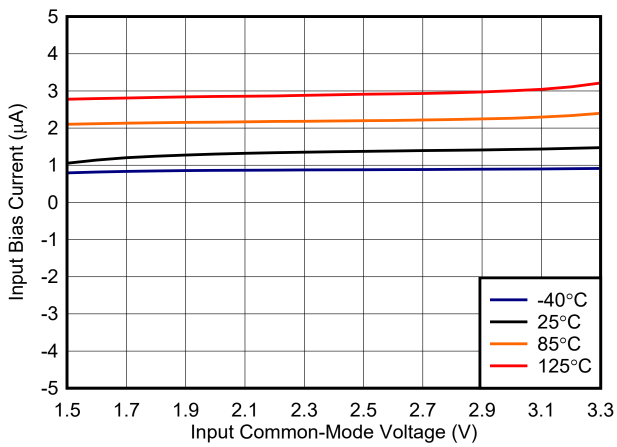


图 6-11. Bias Current vs. Common-Mode, 3.3 V

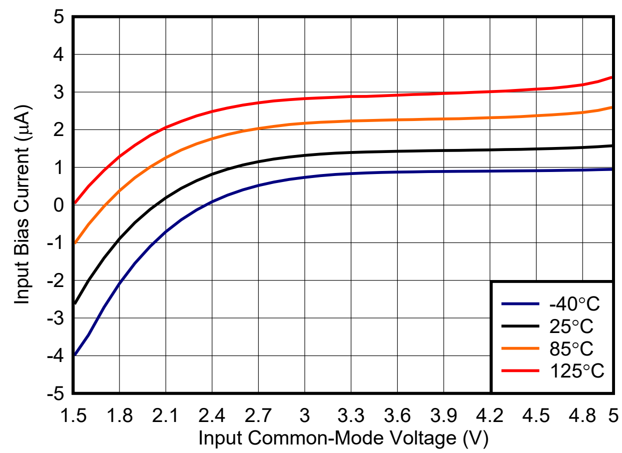


图 6-12. Bias Current vs. Common-Mode, 5 V

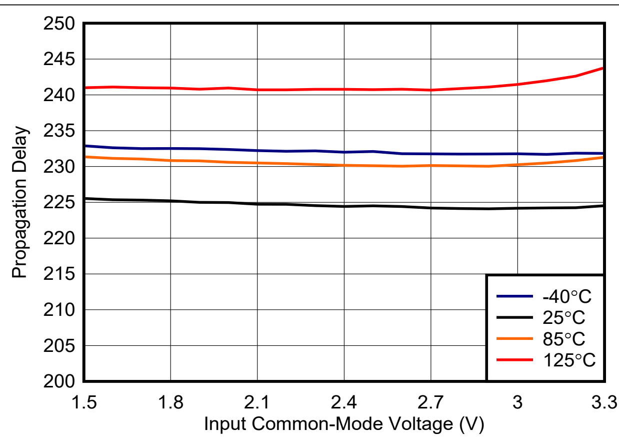


图 6-13. Propagation Delay vs. Common-Mode, 3.3 V

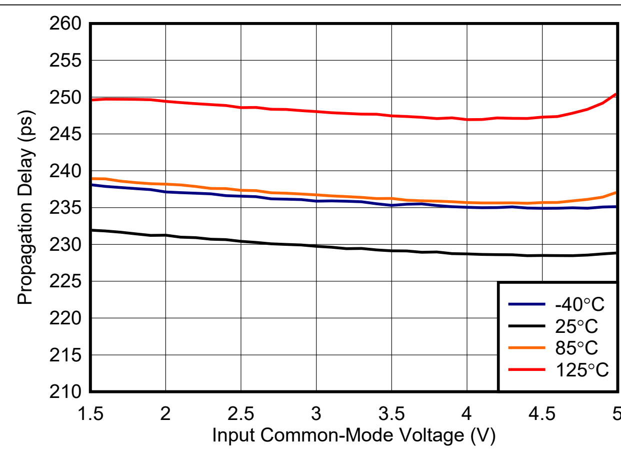


图 6-14. Propagation Delay vs. Common-Mode, 5 V

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 3.3 V to 5 V while V_{EE} = GND = 0, V_{CM} = 2.5 V, and input overdrive/underdrive = 50 mV, unless otherwise noted.

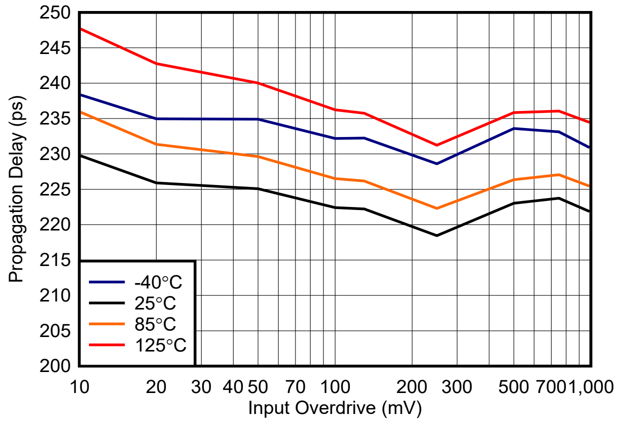


图 6-15. Propagation Delay vs. Overdrive, 3.3 V

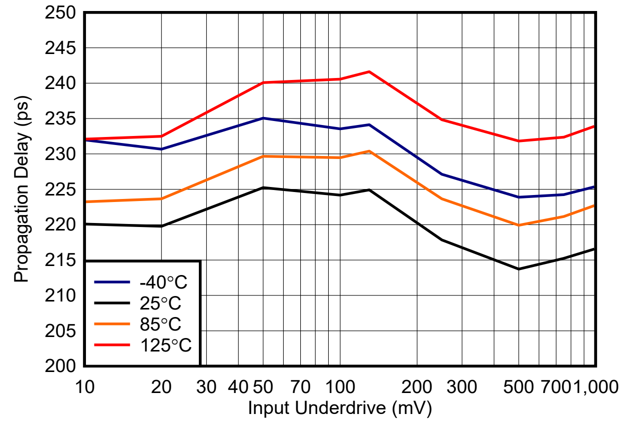


图 6-16. Propagation Delay vs. Underdrive, 3.3 V

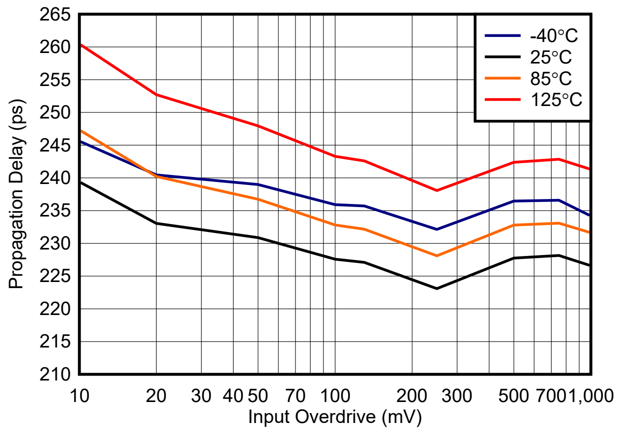


图 6-17. Propagation Delay vs. Overdrive, 5 V

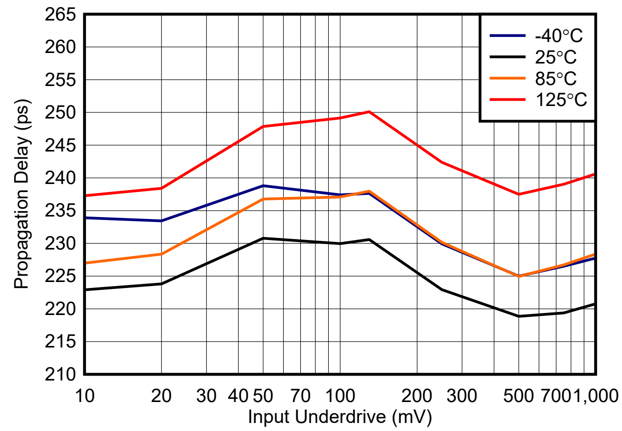


图 6-18. Propagation Delay vs. Underdrive, 5 V

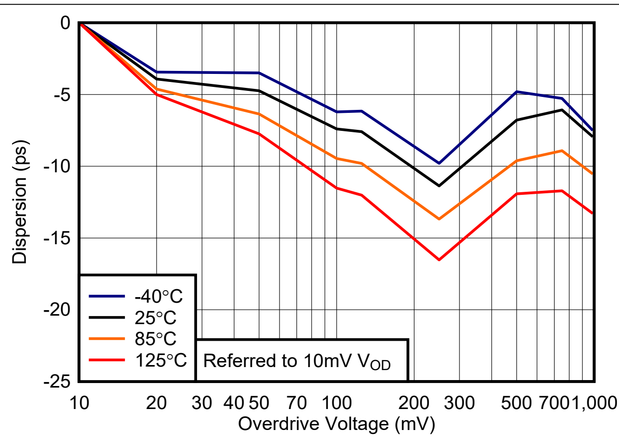


图 6-19. Dispersion vs. Overdrive, 3.3 V

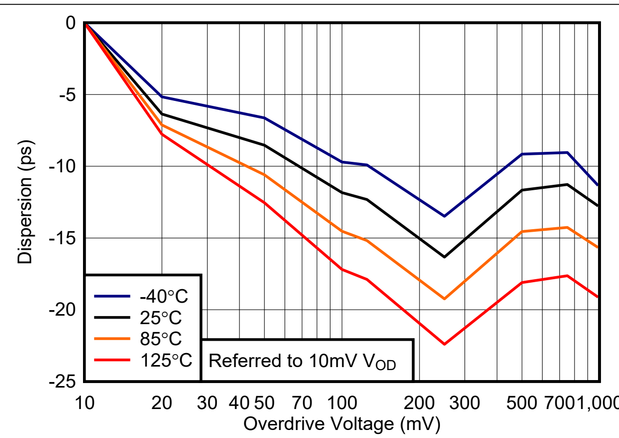


图 6-20. Dispersion vs. Overdrive, 5 V

6.7 Typical Characteristics (continued)

At T_A = 25°C, V_{CC} - V_{EE} = 3.3 V to 5 V while V_{EE} = GND = 0, V_{CM} = 2.5 V, and input overdrive/underdrive = 50 mV, unless otherwise noted.

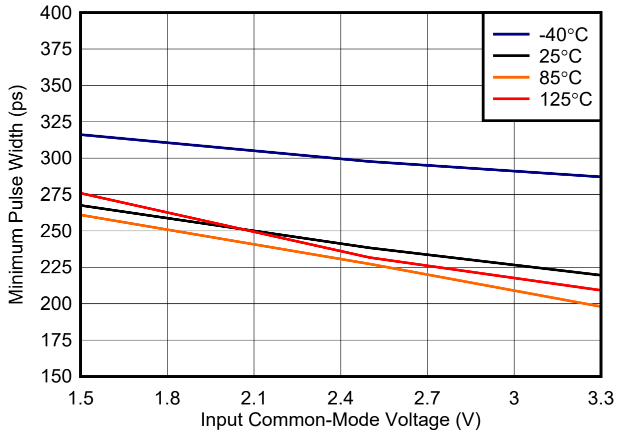


图 6-21. Minimum Pulse Width vs. Common-Mode, 3.3 V

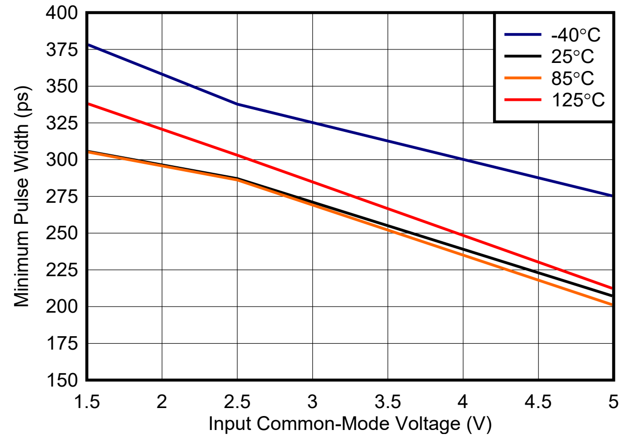


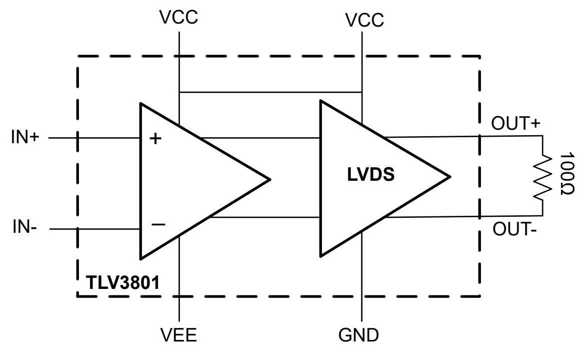
图 6-22. Minimum Pulse Width vs. Common-Mode, 5 V

7 Detailed Description

7.1 Overview

The TLV3801-Q1 is a high-speed comparator with LVDS output. The fast response time of these comparators make them well suited for applications that require narrow pulse width detection or high toggle frequencies. The TLV3801-Q1 is available in the 8-pin DSG package.

7.2 Functional Block Diagram



7.3 Feature Description

The TLV3801-Q1 is a single channel, high-speed comparator with a typical propagation delay of 225 ps and LVDS output. The minimum pulse width detection capability is 240 ps and the typical toggle frequency is 3 GHz (6 Gbps). These comparators are well suited for distance sensing for LIDAR and time-of-flight applications as well as for high-speed test and measurement systems. The TLV3801-Q1 has two separate power rails for the input and the output; this allows the input to be referenced from either single or split supply (VCC and VEE) while the output is referenced from ground (VCC and GND).

7.4 Device Functional Modes

The TLV3801-Q1 has a single functional mode and is operational on the condition that both the input supply voltage (VCC - VEE) is greater than or equal to 2.7 V and the output supply voltage (VCC - GND) is greater than or equal to 2.4 V.

7.4.1 Inputs

The TLV3801-Q1 features an input stage, capable of operating between 1.5 V above VEE and 0.1 V above VCC, with an internal ESD protection circuit that includes two pairs of front-to-back diodes between IN+ and IN- as well as two 50 Ω resistors, as shown in 图 7-1. This prevents damage to the input stage by limiting the differential input voltage to be no more than twice the diode's forward-voltage drop 2 × V_F (2 × 0.7 V).

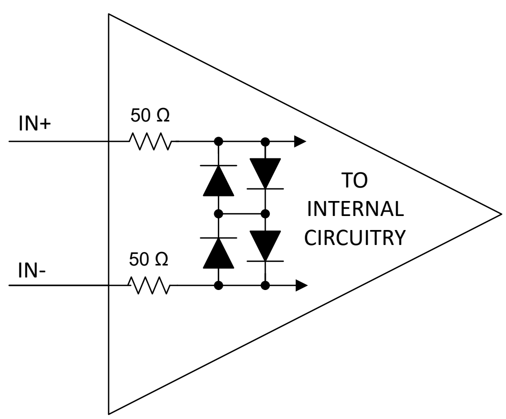


图 7-1. Input Stage Circuitry

When the differential input voltage exceeds 2 × V_F, the input bias current increases at the input pins IN+ and IN-, as shown in 方程式 1.

$$\text{Input Current} = [(V_{IN+} - V_{IN-}) - 2 \times V_F] / (2 \times 50) \tag{1}$$

To avoid damaging the inputs when exceeding the recommended input voltage range, an external resistor should be used to limit the current. The current should be limited to less than 10 mA.

7.4.2 LVDS Output

The TLV3801-Q1 outputs are LVDS compliant. When the input of the downstream device is terminated with a 100 Ω resistor, the comparators provide a ±350 mV differential swing at an output common-mode voltage of 1.25 V above GND. Fully differential outputs enable fast digital toggling and reduce EMI compared to single-ended output standards.

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Capacitive Loads

Under reasonable capacitive loads, the device maintains specified propagation delay. However, excessive capacitive loading under high switching frequencies may increase supply current, propagation delay, or induce decreased slew rate.

8.1.2 Hysteresis

As a result of a comparator's high open loop gain, there is a small band of input differential voltage where the comparator may produce "chatter" which causes the output to toggle back and forth between a “logic high” and a “logic low”. This can cause design challenges for inputs with slow rise and fall times or systems with excessive noise. These challenges can be prevented by adding external hysteresis to the comparator.

Since the TLV3801-Q1 only have a minimal amount of internal hysteresis, external hysteresis can be applied in the form of a positive feedback loop that adjusts the trip point of the comparator depending on its current output state. See the Non-Inverting Comparator With Hysteresis section for more details.

8.2 Typical Application

8.2.1 Optical Receiver

The TLV3801-Q1 can be used in conjunction with a high performance amplifier such as the OPA858 to create an optical receiver as shown in the 图 8-1. The photodiode operates in photoconductive mode: exposure to light will cause a reverse current through the photodiode. A bias voltage is applied to the op amp's non-inverting input to prevent saturation at the negative power supply. The OPA858 takes the current conducting through the diode and translates it into a voltage for a high speed comparator to detect. The TLV3801-Q1 will then output the proper LVDS signal according to the threshold set (V_{REF}).

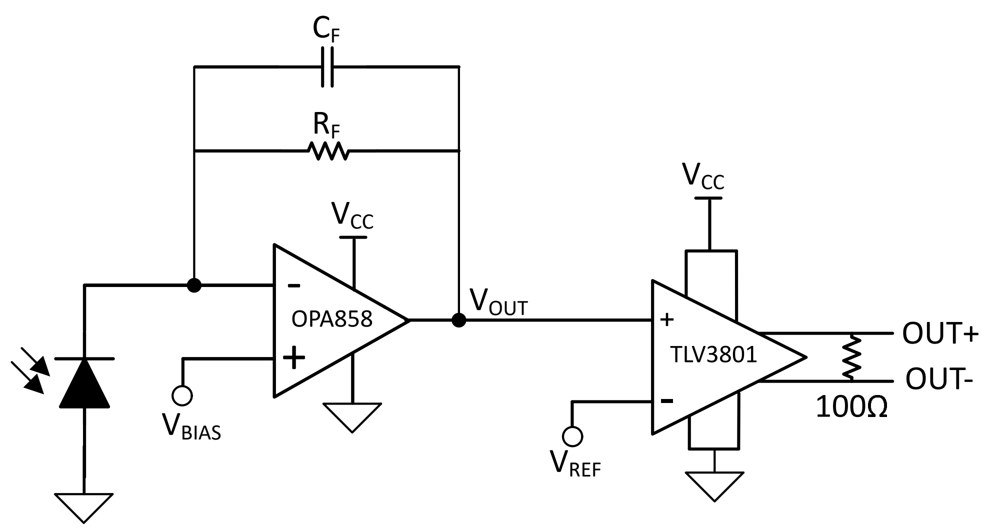


图 8-1. Optical Receiver

8.2.1.1 Design Requirements

表 8-1. Design Parameters

PARAMETER	VALUE
V_{CC}	+5 V
V_{EE}	0 V
$V_{OUT, SWING}$	100 mV
I_{DIODE}	100 µA
f_p	159 MHz

8.2.1.2 Detailed Design Procedure

Set V_{BIAS} to be in the recommended common-mode voltage range of the OPA858. This is also the minimum output voltage of the op amp $V_{OUT, MIN}$ as the op amp will attempt to settle at the voltage applied to the non-inverting input.

The maximum output voltage of the op amp $V_{OUT, MAX}$ can be calculated from the desired output voltage swing $V_{OUT, SWING}$ and $V_{OUT, MIN}$, as shown in 方程式 2.

$$V_{OUT, MAX} = V_{OUT, SWING} + V_{OUT, MIN} \tag{2}$$

The gain resistor R_F is determined by the desired $V_{OUT, MAX}$ and $V_{OUT, MIN}$ and the maximum current I_{DIODE} through the diode, as shown in 方程式 2.

$$R_F = (V_{OUT, MAX} - V_{OUT, MIN}) / I_{DIODE} \tag{3}$$

The feedback capacitor, in combinaton with the gain resistor, forms a pole in the frequency response of the amplifier. The feedback capacitor can be determined by the gain resistor and the desired pole frequency f_p, as shown in 方程式 2.

$$C_F = 1 / (2 \times \pi \times R_F \times f_p) \tag{4}$$

Set V_{REF} to be the switching threshold voltage between $V_{OUT, MAX}$ and $V_{OUT, MIN}$.

Select values for V_{BIAS} and V_{REF}. Plug in given values for $V_{OUT, MAX,}$ I_{DIODE}, and f_p. For the given example, V_{BIAS} = 1.5 V, V_{REF} = 1.55 V, and $R_{F,}$ C_F is solved as 1 kΩ and 1 pF, respectively.

For more information, please refer to the op amp tutorials for stability analysis on the transimpedance amplifier Spice Stability Analysis and Op Amp Stability. See application note SBOA268A Transimpedance Amplifier Circuit for more detailed procedures.

8.2.1.3 Application Performance Plots

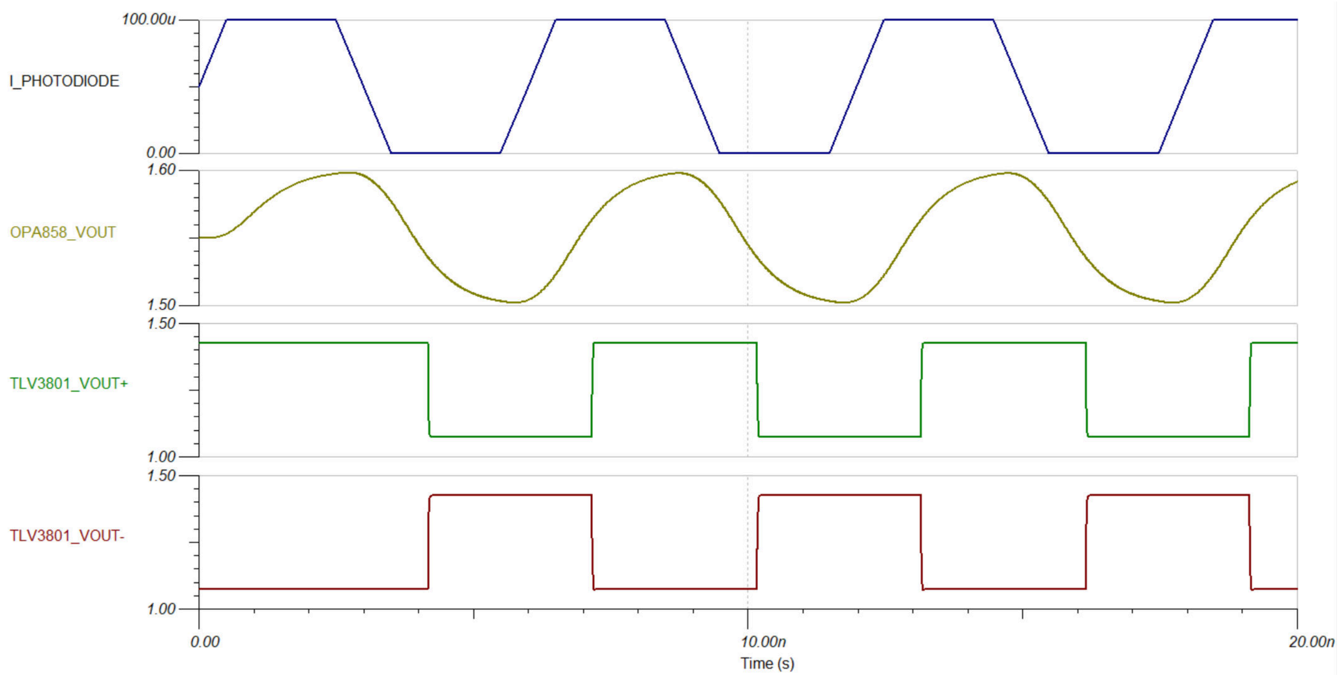


图 8-2.

8.2.2 Non-Inverting Comparator With Hysteresis

A way to implement external hysteresis to the TLV3801-Q1 is to add two resistors to the circuit: one in series between the reference voltage and the inverting pin, and another from the inverting pin to one of the differential output pins.

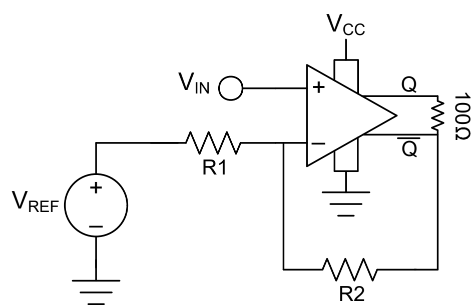


图 8-3. Non-Inverting Comparator with Hysteresis Circuit

8.2.2.1 Design Requirements

表 8-2. Design Parameters

PARAMETER	VALUE
V_{HYS}	50 mV
V_{REF}	2.5 V
V_{T1}	2.34 V
V_{T2}	2.29 V
Q	1.425 V
$\overline{Q}$	1.075 V

8.2.2.2 Detailed Design Procedure

First, create an equation for V_T that covers both output voltages when the output is high or low.

$$V_{T1} = \frac{V_{REF}R_2}{R_1+R_2} + \frac{QR_1}{R_1+R_2} \quad (5)$$

$$V_{T2} = \frac{V_{REF}R_2}{R_1+R_2} + \frac{\overline{Q}R_1}{R_1+R_2} \quad (6)$$

The hysteresis voltage in this network is equal to the difference in the two threshold voltage equations.

$$V_{HYS} = V_{T1} - V_{T2} \quad (7)$$

$$V_{HYS} = \frac{V_{REF}R_2}{R_1+R_2} + \frac{QR_1}{R_1+R_2} - \frac{V_{REF}R_2}{R_1+R_2} - \frac{\overline{Q}R_1}{R_1+R_2} \quad (8)$$

$$V_{HYS} = \frac{(Q-\overline{Q})R_1}{R_1+R_2} \quad (9)$$

$$V_{HYS} = \frac{V_{OD}R_1}{R_1+R_2} \quad (10)$$

Note that these equations do not take into account the effects of the internal hysteresis and offset voltage of the comparator. Design parameters will need to be adjusted accordingly.

Select a value for R2. Plug in given values for V_{REF}, V_{T1}, V_{T2}, Q, and $\overline{Q}$, and solve for R1. For the given example, R2 = 50 kΩ, and R1 is solved as = 8.33 kΩ.

8.2.2.3 Application Performance Plots

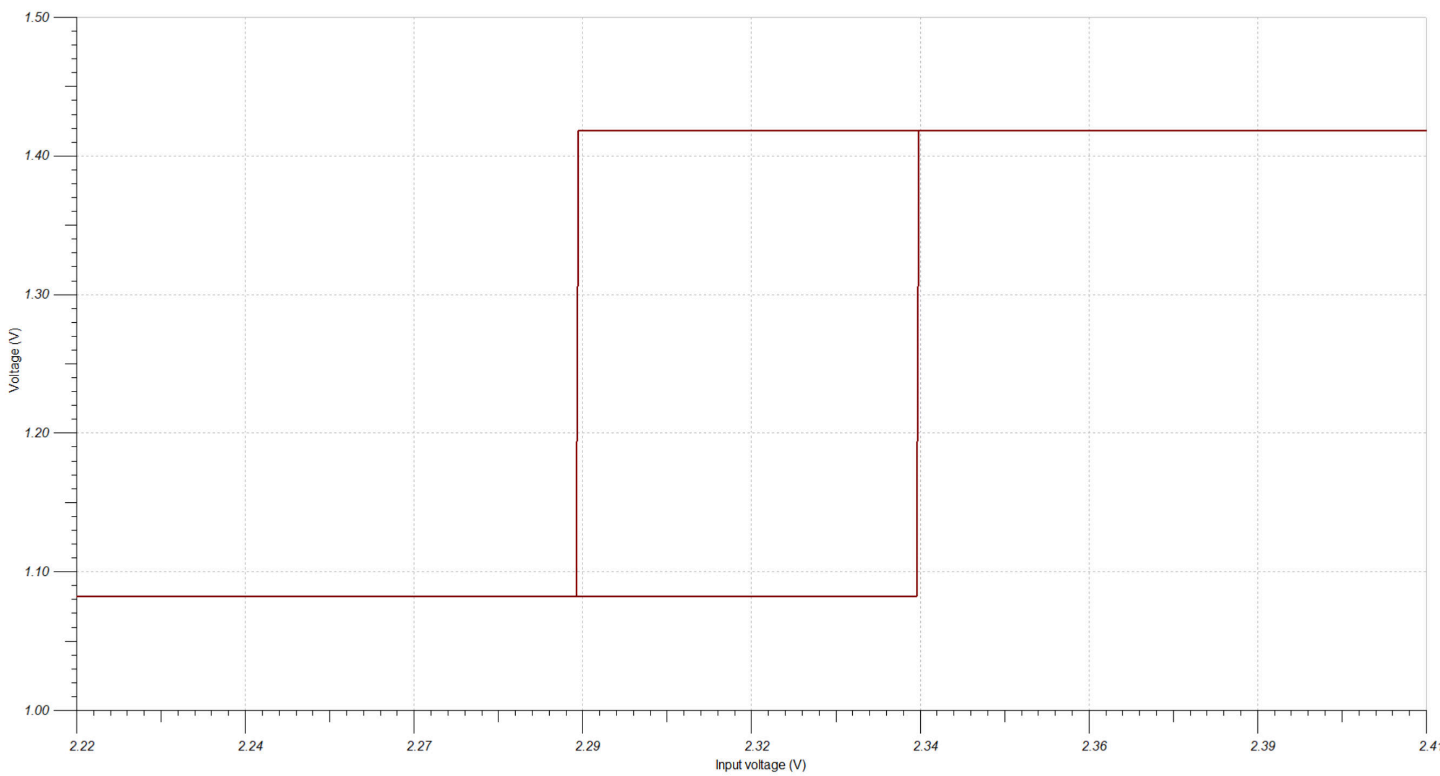


图 8-4. Hysteresis Curve for LVDS Comparator

8.2.3 Logic Clock Source to LVDS Transceiver

The 图 8-5 shows a logic clock source being terminated and driven with the TLV3801-Q1 across a CAT6 Cable to receive an equivalent LVDS clock signal at the receiver end.

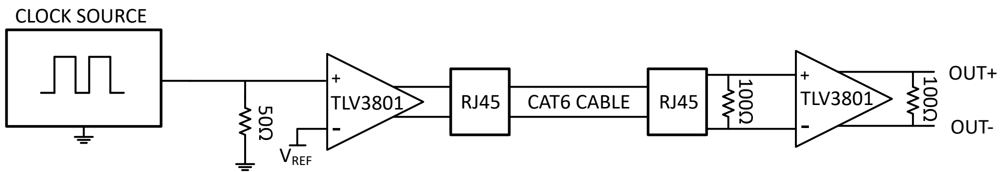


图 8-5. LVDS Clock Transceiver

8.2.4 External Trigger Function for Oscilloscopes

图 8-6 is a typical configuration for creating an external trigger on oscilliscopes. The user adjusts the trigger level, and a DAC converts this trigger level to a voltage the TLV3801-Q1 can use as a reference. The input voltage from an oscilloscope channel is then compared to the trigger reference voltage, and the TLV3801-Q1 sends an LVDS signal to a downstream FPGA to begin a capture. It is common to see bipolar inputs in test and measurement systems such as oscilloscopes; therefore, the TLV3801-Q1 can be configured in split supply so that the inputs are in the allowable input voltage range.

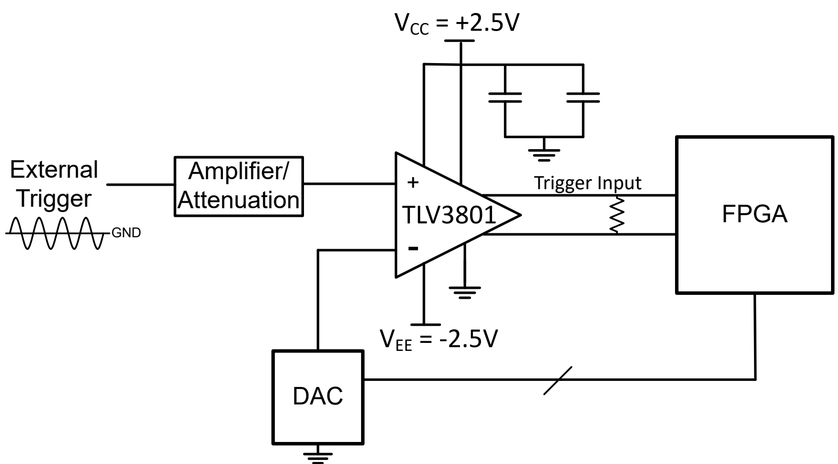


图 8-6. External Trigger Function

8.3 Power Supply Recommendations

The TLV3801-Q1 has two seperate power rails: VCC - VEE for the input stage and VCC - GND for the output stage. This allows for both single and split supply capabilities for the input stage with a seperate ground reference for the LVDS output stage. Split supply operation allows users to apply both positive and negative (bipolar) voltages to the input pins.

When operating from a single supply, the supply voltage range for both the input and output stage is 2.7 V to 5.25 V. When operating from split supply rails, the supply voltage range for the input stage (VCC - VEE) is 2.7 V to 5.25 V, and the supply voltage range for the output stage (VCC - GND) is 2.4 V to 5.25 V. The output logic level is independent of the VCC and VEE levels.

Regardless of single supply or split supply operation, proper decoupling capacitors are required. It is recommended to use a scheme of multiple, low-ESR ceramic capacitors from the supply pins to the ground plane for optimum performance. A good combination would be 100 pF, 10 nF, and 1 uF with the lowest value capacitor closest to the comparator.

8.4 Layout

8.4.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, adhere to the following layout guidelines.

1. Use a printed-circuit-board (PCB) with a good, unbroken, low-inductance ground plane. Proper grounding (use of a ground plane) helps maintain specified device performance.
2. To minimize supply noise for single and split supply, place decoupling capacitor arrays as close as possible to V_{CC}.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.
5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when impedance is low. The topside ground plane runs between the output and inputs.
6. Use a 100 Ω termination resistor across the device's LVDS output.
7. Use higher performance substrate materials such as Rogers.

8.4.2 Layout Example

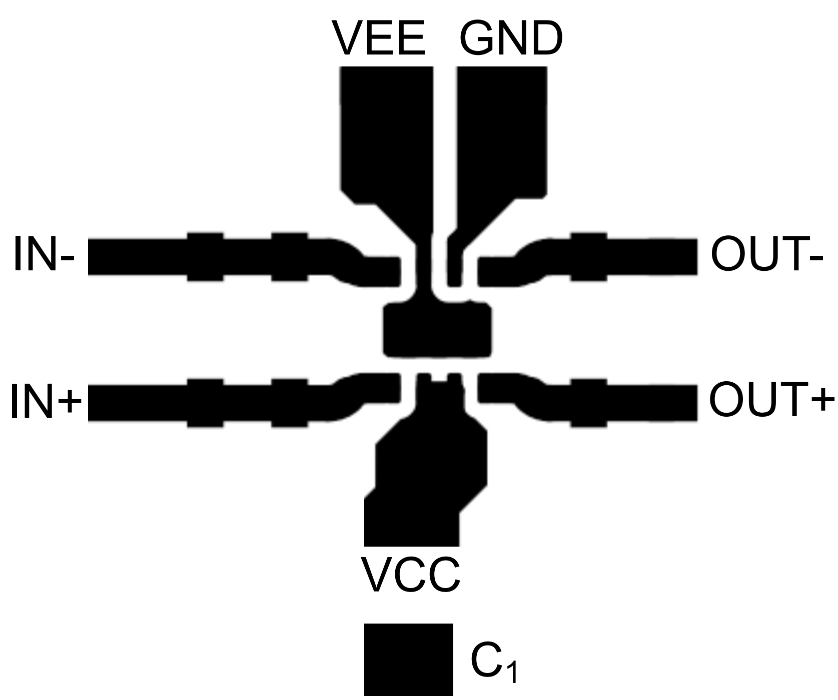


图 8-7. TLV3801EVM Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

LIDAR Pulsed Time of Flight Reference Design

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3801QDSGRQ1	ACTIVE	WSON	DSG	8	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	380Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV3801-Q1 :

- Catalog : TLV3801

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

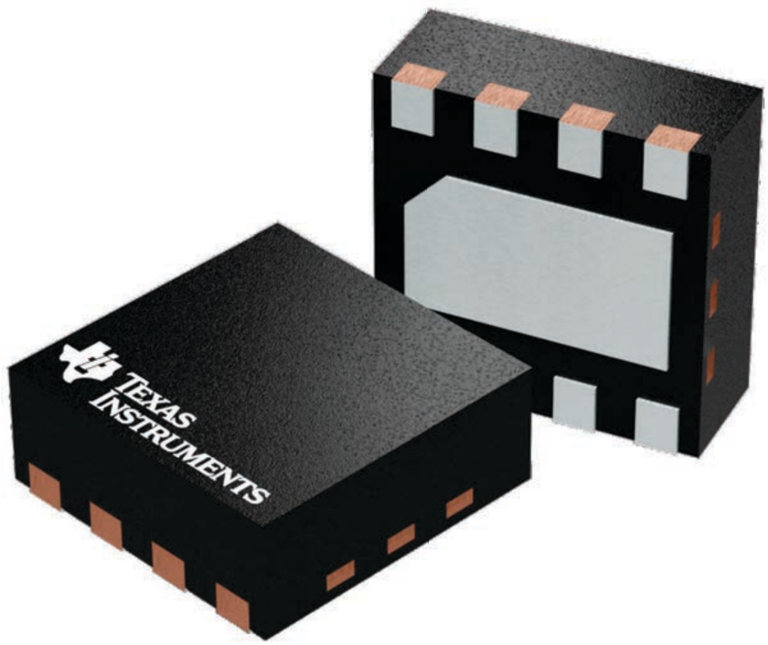
DSG 8

WSON - 0.8 mm max height

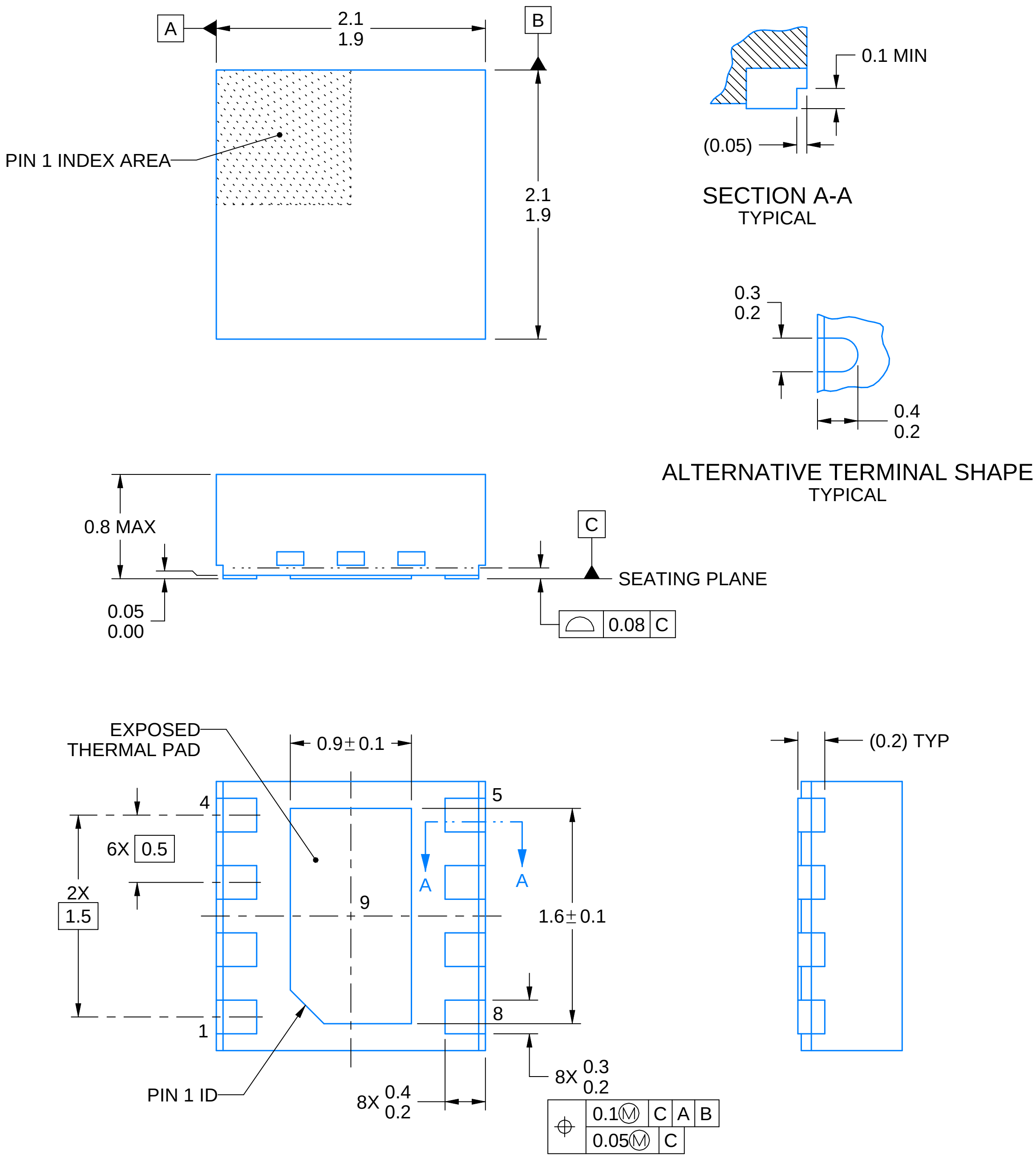
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



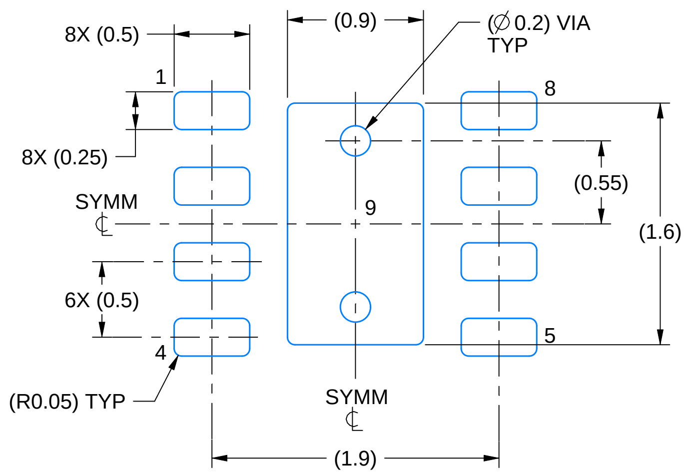
4224783/A



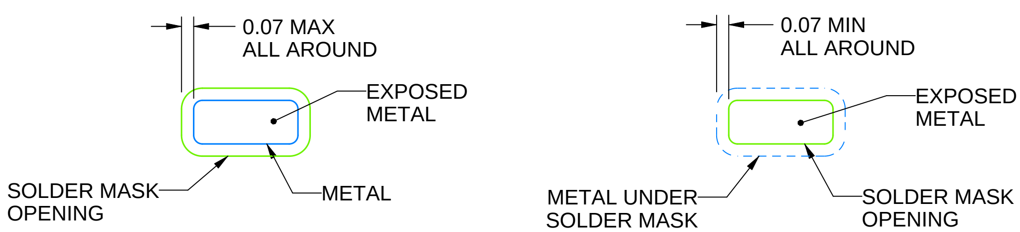
4222124/E 05/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

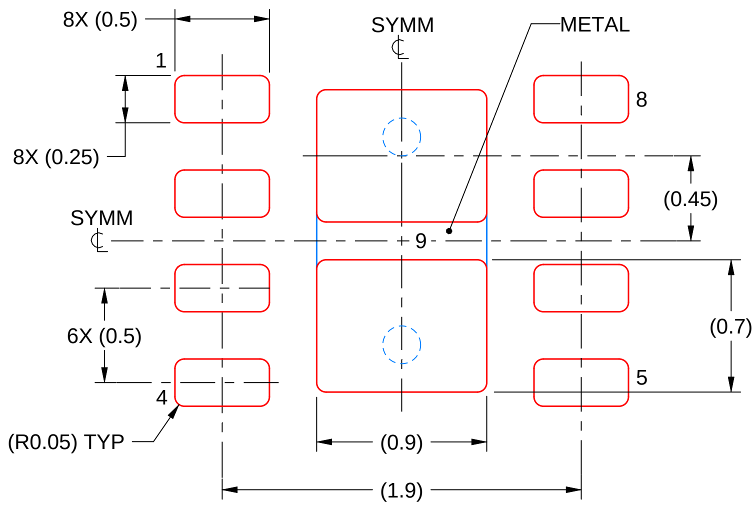
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222124/E 05/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222124/E 05/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.